# Pin Information for the Intel® Cyclone®10 10CL016 Device
## Version 2019.03.29
## Notes (1), (2)

| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | E144 (3) |
|---|---|---|---|---|---|---|
| B1 | VREFB1N0 | IO | | DATA1,ASDO | DIFFIO_L4n | 6 |
| B1 | VREFB1N0 | IO | VREFB1N0 | | | 7 |
| B1 | VREFB1N0 | IO | | FLASH_nCE,nCSO | DIFFIO_L6p | 8 |
| B1 | VREFB1N1 | nSTATUS | | nSTATUS | | 9 |
| B1 | VREFB1N1 | IO | | | | 10 |
| B1 | VREFB1N1 | IO | VREFB1N1 | | | 11 |
| B1 | VREFB1N1 | IO | | DCLK | | 12 |
| B1 | VREFB1N1 | IO | | DATA0 | | 13 |
| B1 | VREFB1N1 | nCONFIG | | nCONFIG | | 14 |
| B1 | VREFB1N1 | TDI | | TDI | | 15 |
| B1 | VREFB1N1 | TCK | | TCK | | 16 |
| B1 | VREFB1N1 | TMS | | TMS | | 18 |
| B1 | VREFB1N1 | TDO | | TDO | | 20 |
| B1 | VREFB1N1 | nCE | | nCE | | 21 |
| B1 | VREFB1N1 | CLK0 | DIFFCLK_0p | | | 22 |
| B1 | VREFB1N1 | CLK1 | DIFFCLK_0n | | | 23 |
| B2 | VREFB2N0 | CLK2 | DIFFCLK_1p | | | 24 |
| B2 | VREFB2N0 | CLK3 | DIFFCLK_1n | | | 25 |
| B2 | VREFB2N0 | IO | VREFB2N0 | | | 28 |
| B2 | VREFB2N1 | IO | VREFB2N1 | | | 31 |
| B2 | VREFB2N1 | IO | RUP1 | | | 32 |
| B2 | VREFB2N1 | IO | RDN1 | | | 33 |
| B3 | VREFB3N1 | IO | VREFB3N1 | | | 39 |
| B3 | VREFB3N1 | IO | CDPCLK2 | | | 42 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTp | | | 43 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTn | | | 44 |
| B3 | VREFB3N0 | IO | VREFB3N0 | | | 46 |
| B3 | VREFB3N0 | IO | | | | 49 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18p | 50 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18n | 51 |
| B3 | VREFB3N0 | CLK15 | DIFFCLK_6p | | | 52 |
| B3 | VREFB3N0 | CLK14 | DIFFCLK_6n | | | 53 |
| B4 | VREFB4N1 | CLK13 | DIFFCLK_7p | | | 54 |
| B4 | VREFB4N1 | CLK12 | DIFFCLK_7n | | | 55 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B21p | 58 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | E144 (3) |
|---|---|---|---|---|---|---|
| B4 | VREFB4N1 | IO | | | DIFFIO_B22p | 59 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B22n | 60 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B23p | 61 |
| B4 | VREFB4N1 | IO | VREFB4N1 | | | 65 |
| B4 | VREFB4N0 | IO | RUP2 | | | 66 |
| B4 | VREFB4N0 | IO | RDN2 | | | 67 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B29n | 68 |
| B4 | VREFB4N0 | IO | VREFB4N0 | | | 69 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTp | | | 71 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTn | | | 72 |
| B5 | VREFB5N1 | IO | RUP3 | | | 76 |
| B5 | VREFB5N1 | IO | RDN3 | | | 77 |
| B5 | VREFB5N1 | IO | VREFB5N1 | | | 80 |
| B5 | VREFB5N0 | IO | VREFB5N0 | | | 83 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R22p | 85 |
| B5 | VREFB5N0 | IO | | DEV_OE | DIFFIO_R21n | 86 |
| B5 | VREFB5N0 | IO | | DEV_CLRn | DIFFIO_R21p | 87 |
| B5 | VREFB5N0 | CLK7 | DIFFCLK_3n | | | 88 |
| B5 | VREFB5N0 | CLK6 | DIFFCLK_3p | | | 89 |
| B6 | VREFB6N1 | CLK5 | DIFFCLK_2n | | | 90 |
| B6 | VREFB6N1 | CLK4 | DIFFCLK_2p | | | 91 |
| B6 | VREFB6N1 | CONF_DONE | | CONF_DONE | | 92 |
| B6 | VREFB6N1 | MSEL0 | | MSEL0 | | 94 |
| B6 | VREFB6N1 | MSEL1 | | MSEL1 | | 96 |
| B6 | VREFB6N1 | MSEL2 | | MSEL2 | | 97 |
| B6 | VREFB6N1 | IO | | INIT_DONE | DIFFIO_R17n | 98 |
| B6 | VREFB6N1 | IO | | CRC_ERROR | DIFFIO_R17p | 99 |
| B6 | VREFB6N1 | IO | VREFB6N1 | | | 100 |
| B6 | VREFB6N1 | IO | | nCEO | DIFFIO_R16n | 101 |
| B6 | VREFB6N1 | IO | | CLKUSR | DIFFIO_R16p | 103 |
| B6 | VREFB6N0 | IO | VREFB6N0 | | | 105 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R2n | 106 |
| B7 | VREFB7N0 | IO | VREFB7N0 | | | 111 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTn | | | 112 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTp | | | 113 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | E144 (3) |
|---|---|---|---|---|---|---|
| B7 | VREFB7N0 | IO | RUP4 | | | 114 |
| B7 | VREFB7N0 | IO | RDN4 | | | 115 |
| B7 | VREFB7N1 | IO | VREFB7N1 | | | 119 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T23n | 120 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T21p | 121 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T17p | 125 |
| B7 | VREFB7N1 | CLK8 | DIFFCLK_5n | | | 126 |
| B7 | VREFB7N1 | CLK9 | DIFFCLK_5p | | | 127 |
| B8 | VREFB8N0 | CLK10 | DIFFCLK_4n | | | 128 |
| B8 | VREFB8N0 | CLK11 | DIFFCLK_4p | | | 129 |
| B8 | VREFB8N0 | IO | | DATA2 | DIFFIO_T12n | 132 |
| B8 | VREFB8N0 | IO | | DATA3 | DIFFIO_T12p | 133 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T11n | 134 |
| B8 | VREFB8N0 | IO | | DATA4 | DIFFIO_T11p | 135 |
| B8 | VREFB8N0 | IO | VREFB8N0 | | | 136 |
| B8 | VREFB8N0 | IO | | DATA5 | | 137 |
| B8 | VREFB8N1 | IO | VREFB8N1 | | | 141 |
| B8 | VREFB8N1 | IO | CDPCLK7 | | DIFFIO_T2p | 142 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTn | | | 143 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTp | | | 144 |
| | | GND | | | | 19 |
| | | GND | | | | 27 |
| | | GND | | | | 41 |
| | | GND | | | | 48 |
| | | GND | | | | 57 |
| | | GND | | | | 63 |
| | | GND | | | | 82 |
| | | GND | | | | 95 |
| | | GND | | | | 118 |
| | | GND | | | | 123 |
| | | GND | | | | 131 |
| | | GND | | | | 140 |
| | | GND | | | | 4 |
| | | GND | | | | 79 |
| | | GND | | | | 30 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | E144 (3) |
|---|---|---|---|---|---|---|
| | | GND | | | | 64 |
| | | GND | | | | 104 |
| | | GND | | | | 110 |
| | | GNDA1 | | | | 36 |
| | | GNDA2 | | | | 108 |
| | | GNDA3 | | | | 2 |
| | | GNDA4 | | | | 74 |
| | | VCCD_PLL1 | | | | 37 |
| | | VCCD_PLL2 | | | | 109 |
| | | VCCD_PLL3 | | | | 1 |
| | | VCCD_PLL4 | | | | 73 |
| | | VCCIO1 | | | | 17 |
| | | VCCIO2 | | | | 26 |
| | | VCCIO3 | | | | 40 |
| | | VCCIO3 | | | | 47 |
| | | VCCIO4 | | | | 56 |
| | | VCCIO4 | | | | 62 |
| | | VCCIO5 | | | | 81 |
| | | VCCIO6 | | | | 93 |
| | | VCCIO7 | | | | 117 |
| | | VCCIO7 | | | | 122 |
| | | VCCIO8 | | | | 130 |
| | | VCCIO8 | | | | 139 |
| | | VCCA1 | | | | 35 |
| | | VCCA2 | | | | 107 |
| | | VCCA3 | | | | 3 |
| | | VCCA4 | | | | 75 |
| | | VCCINT | | | | 5 |
| | | VCCINT | | | | 29 |
| | | VCCINT | | | | 34 |
| | | VCCINT | | | | 38 |
| | | VCCINT | | | | 45 |
| | | VCCINT | | | | 70 |
| | | VCCINT | | | | 78 |
| | | VCCINT | | | | 84 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | E144 (3) |
|---|---|---|---|---|---|---|
| | | VCCINT | | | | 102 |
| | | VCCINT | | | | 116 |
| | | VCCINT | | | | 124 |
| | | VCCINT | | | | 138 |

**Notes:**

(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.

(3) The E144 package has an exposed pad at the bottom of the package.
This exposed pad is a ground pad that must be connected to the ground plane on your PCB.
This exposed pad is used for electrical connectivity, and not for thermal purposes.


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | M164 |
|---|---|---|---|---|---|---|
| B1 | VREFB1N0 | IO | | | DIFFIO_L3p | C1 |
| B1 | VREFB1N0 | IO | | DATA1,ASDO | DIFFIO_L4n | D2 |
| B1 | VREFB1N0 | IO | VREFB1N0 | | | D1 |
| B1 | VREFB1N0 | IO | | FLASH_nCE,nCSO | DIFFIO_L6p | E1 |
| B1 | VREFB1N1 | nSTATUS | | nSTATUS | | E2 |
| B1 | VREFB1N1 | IO | VREFB1N1 | | | F1 |
| B1 | VREFB1N1 | IO | | DCLK | | F3 |
| B1 | VREFB1N1 | IO | | DATA0 | | G1 |
| B1 | VREFB1N1 | nCONFIG | | nCONFIG | | G2 |
| B1 | VREFB1N1 | TDI | | TDI | | G3 |
| B1 | VREFB1N1 | TCK | | TCK | | H2 |
| B1 | VREFB1N1 | TMS | | TMS | | H1 |
| B1 | VREFB1N1 | TDO | | TDO | | H3 |
| B1 | VREFB1N1 | nCE | | nCE | | H4 |
| B1 | VREFB1N1 | CLK0 | DIFFCLK_0p | | | J2 |
| B1 | VREFB1N1 | CLK1 | DIFFCLK_0n | | | J1 |
| B2 | VREFB2N0 | CLK2 | DIFFCLK_1p | | | K3 |
| B2 | VREFB2N0 | CLK3 | DIFFCLK_1n | | | J3 |
| B2 | VREFB2N0 | IO | VREFB2N0 | | | K1 |
| B2 | VREFB2N0 | IO | DPCLK1 | | DIFFIO_L19p | L2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L19n | K2 |
| B2 | VREFB2N1 | IO | VREFB2N1 | | | L1 |
| B2 | VREFB2N1 | IO | RUP1 | | | M1 |
| B2 | VREFB2N1 | IO | RDN1 | | | M2 |
| B3 | VREFB3N1 | IO | VREFB3N1 | | | R3 |
| B3 | VREFB3N1 | IO | CDPCLK2 | | | R4 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTp | | | P5 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTn | | | R5 |
| B3 | VREFB3N0 | IO | VREFB3N0 | | | N5 |
| B3 | VREFB3N0 | IO | | | | R6 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18p | R7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18n | P7 |
| B3 | VREFB3N0 | CLK15 | DIFFCLK_6p | | | N6 |
| B3 | VREFB3N0 | CLK14 | DIFFCLK_6n | | | N7 |
| B4 | VREFB4N1 | CLK13 | DIFFCLK_7p | | | P8 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | M164 |
|---|---|---|---|---|---|---|
| B4 | VREFB4N1 | CLK12 | DIFFCLK_7n | | | R8 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B21p | R9 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B22p | N8 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B22n | P9 |
| B4 | VREFB4N1 | IO | | | | P10 |
| B4 | VREFB4N1 | IO | VREFB4N1 | | | R10 |
| B4 | VREFB4N0 | IO | RUP2 | | | N12 |
| B4 | VREFB4N0 | IO | RDN2 | | | P12 |
| B4 | VREFB4N0 | IO | CDPCLK3 | | DIFFIO_B29n | R11 |
| B4 | VREFB4N0 | IO | VREFB4N0 | | | R12 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTp | | | R14 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTn | | | R13 |
| B5 | VREFB5N1 | IO | RUP3 | | | N15 |
| B5 | VREFB5N1 | IO | RDN3 | | | M14 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R31n | M15 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R31p | L14 |
| B5 | VREFB5N1 | IO | VREFB5N1 | | | L15 |
| B5 | VREFB5N0 | IO | VREFB5N0 | | | K13 |
| B5 | VREFB5N0 | IO | DPCLK6 | | DIFFIO_R22p | K14 |
| B5 | VREFB5N0 | IO | | DEV_OE | DIFFIO_R21n | K15 |
| B5 | VREFB5N0 | IO | | DEV_CLRn | DIFFIO_R21p | J13 |
| B5 | VREFB5N0 | CLK7 | DIFFCLK_3n | | | J15 |
| B5 | VREFB5N0 | CLK6 | DIFFCLK_3p | | | J14 |
| B6 | VREFB6N1 | CLK5 | DIFFCLK_2n | | | H15 |
| B6 | VREFB6N1 | CLK4 | DIFFCLK_2p | | | H14 |
| B6 | VREFB6N1 | CONF_DONE | | CONF_DONE | | H13 |
| B6 | VREFB6N1 | MSEL0 | | MSEL0 | | G13 |
| B6 | VREFB6N1 | MSEL1 | | MSEL1 | | G14 |
| B6 | VREFB6N1 | MSEL2 | | MSEL2 | | G15 |
| B6 | VREFB6N1 | IO | | INIT_DONE | DIFFIO_R17n | F13 |
| B6 | VREFB6N1 | IO | | CRC_ERROR | DIFFIO_R17p | F14 |
| B6 | VREFB6N1 | IO | VREFB6N1 | | | F15 |
| B6 | VREFB6N1 | IO | | nCEO | DIFFIO_R16n | E14 |
| B6 | VREFB6N1 | IO | | CLKUSR | DIFFIO_R16p | E15 |
| B6 | VREFB6N1 | IO | DPCLK7 | | DIFFIO_R15n | D14 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | M164 |
|---|---|---|---|---|---|---|
| B6 | VREFB6N0 | IO | VREFB6N0 | | | D15 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R2n | C15 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T30n | B13 |
| B7 | VREFB7N0 | IO | CDPCLK6 | | DIFFIO_T30p | A14 |
| B7 | VREFB7N0 | IO | VREFB7N0 | | | A13 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTn | | | B12 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTp | | | A12 |
| B7 | VREFB7N0 | IO | RUP4 | | | B11 |
| B7 | VREFB7N0 | IO | RDN4 | | | A11 |
| B7 | VREFB7N1 | IO | VREFB7N1 | | | B10 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T23n | A10 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T21p | C9 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T17p | A9 |
| B7 | VREFB7N1 | CLK8 | DIFFCLK_5n | | | B9 |
| B7 | VREFB7N1 | CLK9 | DIFFCLK_5p | | | A8 |
| B8 | VREFB8N0 | CLK10 | DIFFCLK_4n | | | B8 |
| B8 | VREFB8N0 | CLK11 | DIFFCLK_4p | | | A7 |
| B8 | VREFB8N0 | IO | | DATA2 | DIFFIO_T12n | C7 |
| B8 | VREFB8N0 | IO | | DATA3 | DIFFIO_T12p | B7 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T11n | B6 |
| B8 | VREFB8N0 | IO | | DATA4 | DIFFIO_T11p | A6 |
| B8 | VREFB8N0 | IO | VREFB8N0 | | | C6 |
| B8 | VREFB8N0 | IO | | DATA5 | | A5 |
| B8 | VREFB8N1 | IO | | DATA6 | DIFFIO_T6p | B4 |
| B8 | VREFB8N1 | IO | | DATA7 | | A4 |
| B8 | VREFB8N1 | IO | VREFB8N1 | | | C4 |
| B8 | VREFB8N1 | IO | CDPCLK7 | | DIFFIO_T2p | A3 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTn | | | A2 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTp | | | B3 |
| | | GND | | | | E3 |
| | | GND | | | | G12 |
| | | GND | | | | D7 |
| | | GND | | | | N14 |
| | | GND | | | | M7 |
| | | GND | | | | N1 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | M164 |
|---|---|---|---|---|---|---|
| | | GND | | | | P13 |
| | | GND | | | | P4 |
| | | GND | | | | D9 |
| | | GND | | | | M3 |
| | | GND | | | | R2 |
| | | GND | | | | J12 |
| | | GND | | | | K4 |
| | | GND | | | | N4 |
| | | GND | | | | G4 |
| | | GND | | | | D5 |
| | | GND | | | | C12 |
| | | GND | | | | D11 |
| | | GND | | | | C14 |
| | | GND | | | | M13 |
| | | GND | | | | M10 |
| | | GND | | | | C2 |
| | | GND | | | | C8 |
| | | GND | | | | E13 |
| | | GND | | | | N11 |
| | | GND | | | | P11 |
| | | GND | | | | F2 |
| | | GND | | | | P6 |
| | | GND | | | | N10 |
| | | GNDA1 | | | | P1 |
| | | GNDA2 | | | | B15 |
| | | GNDA3 | | | | B1 |
| | | GNDA4 | | | | P15 |
| | | VCCD_PLL1 | | | | P2 |
| | | VCCD_PLL2 | | | | B14 |
| | | VCCD_PLL3 | | | | B2 |
| | | VCCD_PLL4 | | | | P14 |
| | | VCCIO1 | | | | F4 |
| | | VCCIO2 | | | | J4 |
| | | VCCIO3 | | | | M5 |
| | | VCCIO3 | | | | M6 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | M164 |
|---|---|---|---|---|---|---|
| | | VCCIO4 | | | | M9 |
| | | VCCIO4 | | | | N9 |
| | | VCCIO5 | | | | L13 |
| | | VCCIO6 | | | | D13 |
| | | VCCIO7 | | | | C10 |
| | | VCCIO7 | | | | C11 |
| | | VCCIO8 | | | | B5 |
| | | VCCIO8 | | | | C5 |
| | | VCCA1 | | | | R1 |
| | | VCCA2 | | | | A15 |
| | | VCCA3 | | | | A1 |
| | | VCCA4 | | | | R15 |
| | | VCCINT | | | | D3 |
| | | VCCINT | | | | D6 |
| | | VCCINT | | | | N2 |
| | | VCCINT | | | | D10 |
| | | VCCINT | | | | F12 |
| | | VCCINT | | | | H12 |
| | | VCCINT | | | | M8 |
| | | VCCINT | | | | M11 |
| | | VCCINT | | | | D8 |
| | | VCCINT | | | | L3 |
| | | VCCINT | | | | P3 |
| | | VCCINT | | | | K12 |

**Notes:**
(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U256 |
|---|---|---|---|---|---|---|
| B1 | VREFB1N0 | IO | CDPCLK0 | | DIFFIO_L3p | B1 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L4p | C2 |
| B1 | VREFB1N0 | IO | | DATA1,ASDO | DIFFIO_L4n | C1 |
| B1 | VREFB1N0 | IO | VREFB1N0 | | | F3 |
| B1 | VREFB1N0 | IO | | FLASH_nCE,nCSO | DIFFIO_L6p | D2 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L6n | D1 |
| B1 | VREFB1N1 | nSTATUS | | nSTATUS | | F4 |
| B1 | VREFB1N1 | IO | DPCLK0 | | | G2 |
| B1 | VREFB1N1 | IO | VREFB1N1 | | | G1 |
| B1 | VREFB1N1 | IO | | DCLK | | H1 |
| B1 | VREFB1N1 | IO | | DATA0 | | H2 |
| B1 | VREFB1N1 | nCONFIG | | nCONFIG | | H5 |
| B1 | VREFB1N1 | TDI | | TDI | | H4 |
| B1 | VREFB1N1 | TCK | | TCK | | H3 |
| B1 | VREFB1N1 | TMS | | TMS | | J5 |
| B1 | VREFB1N1 | TDO | | TDO | | J4 |
| B1 | VREFB1N1 | nCE | | nCE | | J3 |
| B1 | VREFB1N1 | CLK0 | DIFFCLK_0p | | | E2 |
| B1 | VREFB1N1 | CLK1 | DIFFCLK_0n | | | E1 |
| B2 | VREFB2N0 | CLK2 | DIFFCLK_1p | | | M2 |
| B2 | VREFB2N0 | CLK3 | DIFFCLK_1n | | | M1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L14p | J2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L14n | J1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L16p | K6 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L16n | L6 |
| B2 | VREFB2N0 | IO | VREFB2N0 | | | L3 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L18n | K1 |
| B2 | VREFB2N0 | IO | DPCLK1 | | DIFFIO_L19p | L2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L19n | L1 |
| B2 | VREFB2N1 | IO | VREFB2N1 | | | K2 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L27p | N2 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L27n | N1 |
| B2 | VREFB2N1 | IO | RUP1 | | | K5 |
| B2 | VREFB2N1 | IO | RDN1 | | | L4 |
| B2 | VREFB2N1 | IO | CDPCLK1 | | | R1 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U256 |
|---|---|---|---|---|---|---|
| B2 | VREFB2N1 | IO | | | DIFFIO_L29p | P2 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L29n | P1 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B3p | N3 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B3n | P3 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B4n | R3 |
| B3 | VREFB3N1 | IO | VREFB3N1 | | | T3 |
| B3 | VREFB3N1 | IO | CDPCLK2 | | | T2 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTp | | | R4 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTn | | | T4 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B7p | N5 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B7n | N6 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B8p | M6 |
| B3 | VREFB3N0 | IO | VREFB3N0 | | | P6 |
| B3 | VREFB3N0 | IO | DPCLK2 | | | M7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B14p | R5 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B14n | T5 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B15p | R6 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B15n | T6 |
| B3 | VREFB3N0 | IO | | | | L7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B16p | R7 |
| B3 | VREFB3N0 | IO | DPCLK3 | | DIFFIO_B16n | T7 |
| B3 | VREFB3N0 | IO | | | | L8 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18p | M8 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18n | N8 |
| B3 | VREFB3N0 | IO | | | | P8 |
| B3 | VREFB3N0 | CLK15 | DIFFCLK_6p | | | R8 |
| B3 | VREFB3N0 | CLK14 | DIFFCLK_6n | | | T8 |
| B4 | VREFB4N1 | CLK13 | DIFFCLK_7p | | | R9 |
| B4 | VREFB4N1 | CLK12 | DIFFCLK_7n | | | T9 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B19p | K9 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B19n | L9 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B20p | M9 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B20n | N9 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B21p | R10 |
| B4 | VREFB4N1 | IO | DPCLK4 | | DIFFIO_B21n | T10 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U256 |
|---|---|---|---|---|---|---|
| B4 | VREFB4N1 | IO | | | DIFFIO_B22p | R11 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B22n | T11 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B23p | R12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B24p | T12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B24n | K10 |
| B4 | VREFB4N1 | IO | | | | L10 |
| B4 | VREFB4N1 | IO | DPCLK5 | | | P9 |
| B4 | VREFB4N1 | IO | VREFB4N1 | | | N12 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B26p | R13 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B26n | T13 |
| B4 | VREFB4N0 | IO | RUP2 | | | M10 |
| B4 | VREFB4N0 | IO | RDN2 | | | N11 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B29p | T14 |
| B4 | VREFB4N0 | IO | CDPCLK3 | | DIFFIO_B29n | T15 |
| B4 | VREFB4N0 | IO | VREFB4N0 | | | P11 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTp | | | P14 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTn | | | R14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B31p | L11 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B31n | M11 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R35p | K12 |
| B5 | VREFB5N1 | IO | RUP3 | | | N14 |
| B5 | VREFB5N1 | IO | RDN3 | | | P15 |
| B5 | VREFB5N1 | IO | CDPCLK4 | | DIFFIO_R34n | P16 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R34p | R16 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R31n | N16 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R31p | N15 |
| B5 | VREFB5N1 | IO | VREFB5N1 | | | L14 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R26n | L13 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R26p | L16 |
| B5 | VREFB5N0 | IO | VREFB5N0 | | | L15 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R22n | K16 |
| B5 | VREFB5N0 | IO | DPCLK6 | | DIFFIO_R22p | K15 |
| B5 | VREFB5N0 | IO | | DEV_OE | DIFFIO_R21n | J16 |
| B5 | VREFB5N0 | IO | | DEV_CLRn | DIFFIO_R21p | J15 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R19n | J14 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U256 |
|---|---|---|---|---|---|---|
| B5 | VREFB5N0 | IO | | | DIFFIO_R19p | J12 |
| B5 | VREFB5N0 | IO | | | | J13 |
| B5 | VREFB5N0 | CLK7 | DIFFCLK_3n | | | M16 |
| B5 | VREFB5N0 | CLK6 | DIFFCLK_3p | | | M15 |
| B6 | VREFB6N1 | CLK5 | DIFFCLK_2n | | | E16 |
| B6 | VREFB6N1 | CLK4 | DIFFCLK_2p | | | E15 |
| B6 | VREFB6N1 | CONF_DONE | | CONF_DONE | | H14 |
| B6 | VREFB6N1 | MSEL0 | | MSEL0 | | H13 |
| B6 | VREFB6N1 | MSEL1 | | MSEL1 | | H12 |
| B6 | VREFB6N1 | MSEL2 | | MSEL2 | | G12 |
| B6 | VREFB6N1 | IO | | INIT_DONE | DIFFIO_R17n | G16 |
| B6 | VREFB6N1 | IO | | CRC_ERROR | DIFFIO_R17p | G15 |
| B6 | VREFB6N1 | IO | VREFB6N1 | | | F13 |
| B6 | VREFB6N1 | IO | | nCEO | DIFFIO_R16n | F16 |
| B6 | VREFB6N1 | IO | | CLKUSR | DIFFIO_R16p | F15 |
| B6 | VREFB6N1 | IO | DPCLK7 | | DIFFIO_R15n | B16 |
| B6 | VREFB6N0 | IO | VREFB6N0 | | | F14 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R7n | D16 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R7p | D15 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R3p | G11 |
| B6 | VREFB6N0 | IO | CDPCLK5 | | DIFFIO_R2n | C16 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R2p | C15 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T32n | C14 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T32p | D14 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T30n | D11 |
| B7 | VREFB7N0 | IO | CDPCLK6 | | DIFFIO_T30p | D12 |
| B7 | VREFB7N0 | IO | VREFB7N0 | | | C11 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T29n | B13 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTn | | | A14 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTp | | | B14 |
| B7 | VREFB7N0 | IO | RUP4 | | | E11 |
| B7 | VREFB7N0 | IO | RDN4 | | | E10 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T27p | A12 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T26n | B12 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T25n | A11 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U256 |
|---|---|---|---|---|---|---|
| B7 | VREFB7N1 | IO | | | DIFFIO_T25p | B11 |
| B7 | VREFB7N1 | IO | VREFB7N1 | | | A13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T23n | A15 |
| B7 | VREFB7N1 | IO | DPCLK8 | | DIFFIO_T21p | F9 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T20n | A10 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T20p | B10 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T19n | C9 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T19p | D9 |
| B7 | VREFB7N1 | IO | DPCLK9 | | DIFFIO_T17p | E9 |
| B7 | VREFB7N1 | CLK8 | DIFFCLK_5n | | | A9 |
| B7 | VREFB7N1 | CLK9 | DIFFCLK_5p | | | B9 |
| B8 | VREFB8N0 | CLK10 | DIFFCLK_4n | | | A8 |
| B8 | VREFB8N0 | CLK11 | DIFFCLK_4p | | | B8 |
| B8 | VREFB8N0 | IO | DPCLK10 | | DIFFIO_T13p | C8 |
| B8 | VREFB8N0 | IO | | | | D8 |
| B8 | VREFB8N0 | IO | | DATA2 | DIFFIO_T12n | E8 |
| B8 | VREFB8N0 | IO | | DATA3 | DIFFIO_T12p | F8 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T11n | A7 |
| B8 | VREFB8N0 | IO | | DATA4 | DIFFIO_T11p | B7 |
| B8 | VREFB8N0 | IO | VREFB8N0 | | | C6 |
| B8 | VREFB8N0 | IO | DPCLK11 | | DIFFIO_T9n | A6 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T9p | B6 |
| B8 | VREFB8N0 | IO | | DATA5 | | E7 |
| B8 | VREFB8N1 | IO | | DATA6 | DIFFIO_T6p | E6 |
| B8 | VREFB8N1 | IO | | DATA7 | | A5 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T5p | B5 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T4n | D6 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T3n | A4 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T3p | B4 |
| B8 | VREFB8N1 | IO | VREFB8N1 | | | A2 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T2n | A3 |
| B8 | VREFB8N1 | IO | CDPCLK7 | | DIFFIO_T2p | B3 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTn | | | C3 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTp | | | D3 |
| | | GND | | | | H7 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U256 |
|---|---|---|---|---|---|---|
| | | GND | | | | H8 |
| | | GND | | | | H9 |
| | | GND | | | | H10 |
| | | GND | | | | J7 |
| | | GND | | | | J8 |
| | | GND | | | | J9 |
| | | GND | | | | J10 |
| | | GND | | | | F6 |
| | | GND | | | | F10 |
| | | GND | | | | J11 |
| | | GND | | | | K8 |
| | | GND | | | | B2 |
| | | GND | | | | B15 |
| | | GND | | | | C5 |
| | | GND | | | | C12 |
| | | GND | | | | D7 |
| | | GND | | | | D10 |
| | | GND | | | | E4 |
| | | GND | | | | E13 |
| | | GND | | | | G4 |
| | | GND | | | | G13 |
| | | GND | | | | K4 |
| | | GND | | | | K13 |
| | | GND | | | | M4 |
| | | GND | | | | M13 |
| | | GND | | | | N7 |
| | | GND | | | | N10 |
| | | GND | | | | P5 |
| | | GND | | | | P12 |
| | | GND | | | | R2 |
| | | GND | | | | R15 |
| | | GND | | | | H16 |
| | | GND | | | | H15 |
| | | GND | | | | D5 |
| | | GND | | | | F1 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U256 |
|---|---|---|---|---|---|---|
| | | GND | | | | F2 |
| | | GND | | | | G5 |
| | | GNDA1 | | | | M5 |
| | | GNDA2 | | | | E12 |
| | | GNDA3 | | | | E5 |
| | | GNDA4 | | | | M12 |
| | | VCCD_PLL1 | | | | N4 |
| | | VCCD_PLL2 | | | | D13 |
| | | VCCD_PLL3 | | | | D4 |
| | | VCCD_PLL4 | | | | N13 |
| | | VCCIO1 | | | | E3 |
| | | VCCIO1 | | | | G3 |
| | | VCCIO2 | | | | K3 |
| | | VCCIO2 | | | | M3 |
| | | VCCIO3 | | | | P4 |
| | | VCCIO3 | | | | P7 |
| | | VCCIO3 | | | | T1 |
| | | VCCIO4 | | | | P10 |
| | | VCCIO4 | | | | P13 |
| | | VCCIO4 | | | | T16 |
| | | VCCIO5 | | | | K14 |
| | | VCCIO5 | | | | M14 |
| | | VCCIO6 | | | | E14 |
| | | VCCIO6 | | | | G14 |
| | | VCCIO7 | | | | A16 |
| | | VCCIO7 | | | | C10 |
| | | VCCIO7 | | | | C13 |
| | | VCCIO8 | | | | A1 |
| | | VCCIO8 | | | | C4 |
| | | VCCIO8 | | | | C7 |
| | | VCCA1 | | | | L5 |
| | | VCCA2 | | | | F12 |
| | | VCCA3 | | | | F5 |
| | | VCCA4 | | | | L12 |
| | | VCCINT | | | | F7 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U256 |
|---|---|---|---|---|---|---|
| | | VCCINT | | | | F11 |
| | | VCCINT | | | | G6 |
| | | VCCINT | | | | G7 |
| | | VCCINT | | | | G8 |
| | | VCCINT | | | | G9 |
| | | VCCINT | | | | G10 |
| | | VCCINT | | | | H6 |
| | | VCCINT | | | | H11 |
| | | VCCINT | | | | J6 |
| | | VCCINT | | | | K7 |
| | | VCCINT | | | | K11 |

**Notes:**
(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.


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# Pin Information for the Intel® Cyclone®10 10CL016 Device
## Version 2019.03.29
## Notes (1), (2)

| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| B1 | VREFB1N0 | IO | | | | H5 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L1p | B2 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L1n | B1 |
| B1 | VREFB1N0 | IO | | | | G5 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L2p | E4 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L2n | E3 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L4p | D2 |
| B1 | VREFB1N0 | IO | | DATA1,ASDO | DIFFIO_L4n | D1 |
| B1 | VREFB1N0 | IO | VREFB1N0 | | | H7 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L5p | H6 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L5n | J6 |
| B1 | VREFB1N0 | IO | | FLASH_nCE,nCSO | DIFFIO_L6p | E2 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L6n | E1 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L7p | F2 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L7n | F1 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L8p | G4 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L8n | G3 |
| B1 | VREFB1N1 | nSTATUS | | nSTATUS | | K6 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L9p | L8 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L9n | K8 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L10p | J7 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L10n | K7 |
| B1 | VREFB1N1 | IO | DPCLK0 | | | J4 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L11p | H2 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L11n | H1 |
| B1 | VREFB1N1 | IO | VREFB1N1 | | | J3 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L12p | J2 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L12n | J1 |
| B1 | VREFB1N1 | IO | | DCLK | | K2 |
| B1 | VREFB1N1 | IO | | DATA0 | | K1 |
| B1 | VREFB1N1 | nCONFIG | | nCONFIG | | K5 |
| B1 | VREFB1N1 | TDI | | TDI | | L5 |
| B1 | VREFB1N1 | TCK | | TCK | | L2 |
| B1 | VREFB1N1 | TMS | | TMS | | L1 |
| B1 | VREFB1N1 | TDO | | TDO | | L4 |
| B1 | VREFB1N1 | nCE | | nCE | | L3 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| B1 | VREFB1N1 | CLK0 | DIFFCLK_0p | | | G2 |
| B1 | VREFB1N1 | CLK1 | DIFFCLK_0n | | | G1 |
| B2 | VREFB2N0 | CLK2 | DIFFCLK_1p | | | T2 |
| B2 | VREFB2N0 | CLK3 | DIFFCLK_1n | | | T1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L13p | L6 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L13n | M6 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L14p | M2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L14n | M1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L15p | M4 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L15n | M3 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L16p | N2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L16n | N1 |
| B2 | VREFB2N0 | IO | | | | L7 |
| B2 | VREFB2N0 | IO | VREFB2N0 | | | M5 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L17p | P2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L17n | P1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L18p | R2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L18n | R1 |
| B2 | VREFB2N0 | IO | | | | N5 |
| B2 | VREFB2N0 | IO | DPCLK1 | | DIFFIO_L19p | P4 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L19n | P3 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L20p | U2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L20n | U1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L21p | V2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L21n | V1 |
| B2 | VREFB2N0 | IO | | | | P5 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L22p | N6 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L22n | M7 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L23p | M8 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L23n | N8 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L24p | W2 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L24n | W1 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L25p | Y2 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L25n | Y1 |
| B2 | VREFB2N1 | IO | VREFB2N1 | | | T3 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L26p | N7 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| B2 | VREFB2N1 | IO | | | DIFFIO_L26n | P7 |
| B2 | VREFB2N1 | IO | RUP1 | | | V4 |
| B2 | VREFB2N1 | IO | RDN1 | | | V3 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L28p | P6 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L28n | R5 |
| B2 | VREFB2N1 | IO | CDPCLK1 | | | T4 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L29p | T5 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L29n | R6 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L30p | R7 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L30n | T7 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L31p | P8 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L31n | R8 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B1p | R9 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B1n | T8 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B2p | R10 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B2n | T9 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B3p | V6 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B3n | V5 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B4p | U7 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B4n | U8 |
| B3 | VREFB3N1 | IO | VREFB3N1 | | | Y4 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B5p | R11 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B5n | R12 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B6p | Y3 |
| B3 | VREFB3N1 | IO | CDPCLK2 | | | Y6 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTp | | | AA3 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTn | | | AB3 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B7p | W6 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B7n | V7 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B8p | AA4 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B8n | AB4 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B9p | AA5 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B9n | AB5 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B10p | W7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B10n | Y7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B11p | U9 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| B3 | VREFB3N0 | IO | | | DIFFIO_B11n | V8 |
| B3 | VREFB3N0 | IO | | | | W8 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B12p | AA7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B12n | AB7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B13p | Y8 |
| B3 | VREFB3N0 | IO | VREFB3N0 | | | V9 |
| B3 | VREFB3N0 | IO | DPCLK2 | | | V10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B14p | T10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B14n | U10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B15p | AA8 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B15n | AB8 |
| B3 | VREFB3N0 | IO | | | | T11 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B16p | AA9 |
| B3 | VREFB3N0 | IO | DPCLK3 | | DIFFIO_B16n | AB9 |
| B3 | VREFB3N0 | IO | | | | U11 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B17p | V11 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B17n | W10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18p | Y10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18n | AA10 |
| B3 | VREFB3N0 | IO | | | | AB10 |
| B3 | VREFB3N0 | CLK15 | DIFFCLK_6p | | | AA11 |
| B3 | VREFB3N0 | CLK14 | DIFFCLK_6n | | | AB11 |
| B4 | VREFB4N1 | CLK13 | DIFFCLK_7p | | | AA12 |
| B4 | VREFB4N1 | CLK12 | DIFFCLK_7n | | | AB12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B19p | AA13 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B19n | AB13 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B20p | AA14 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B20n | AB14 |
| B4 | VREFB4N1 | IO | | | | V12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B21p | W13 |
| B4 | VREFB4N1 | IO | DPCLK4 | | DIFFIO_B21n | Y13 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B22p | AA15 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B22n | AB15 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B23p | U12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B23n | T12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B24p | AA16 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| B4 | VREFB4N1 | IO | | | DIFFIO_B24n | AB16 |
| B4 | VREFB4N1 | IO | | | | R13 |
| B4 | VREFB4N1 | IO | DPCLK5 | | | V13 |
| B4 | VREFB4N1 | IO | VREFB4N1 | | | W14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B26p | U13 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B26n | V14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B27p | V15 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B27n | W15 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B28p | T14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B28n | T15 |
| B4 | VREFB4N0 | IO | | | | AB18 |
| B4 | VREFB4N0 | IO | | | | AA18 |
| B4 | VREFB4N0 | IO | RUP2 | | | AA19 |
| B4 | VREFB4N0 | IO | RDN2 | | | AB19 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B29p | W17 |
| B4 | VREFB4N0 | IO | CDPCLK3 | | DIFFIO_B29n | Y17 |
| B4 | VREFB4N0 | IO | VREFB4N0 | | | V16 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B30p | AA20 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B30n | AB20 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTp | | | T16 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTn | | | R16 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B31p | U15 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B31n | U14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B32p | R14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B32n | R15 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R35n | AA22 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R35p | AA21 |
| B5 | VREFB5N1 | IO | | | | P14 |
| B5 | VREFB5N1 | IO | RUP3 | | | T17 |
| B5 | VREFB5N1 | IO | RDN3 | | | T18 |
| B5 | VREFB5N1 | IO | CDPCLK4 | | DIFFIO_R34n | W20 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R34p | W19 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R33n | Y22 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R33p | Y21 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R32n | U20 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R32p | U19 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| B5 | VREFB5N1 | IO | | | | N14 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R31n | W22 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R31p | W21 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R30n | P15 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R30p | P16 |
| B5 | VREFB5N1 | IO | VREFB5N1 | | | R17 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R29n | M15 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R29p | N15 |
| B5 | VREFB5N1 | IO | | | | P17 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R28n | V22 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R28p | V21 |
| B5 | VREFB5N1 | IO | | | | R20 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R27n | U22 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R27p | U21 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R26n | R18 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R26p | R19 |
| B5 | VREFB5N0 | IO | | | | N16 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R25n | R22 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R25p | R21 |
| B5 | VREFB5N0 | IO | VREFB5N0 | | | P20 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R24n | P22 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R24p | P21 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R23n | N20 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R23p | N19 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R22n | N17 |
| B5 | VREFB5N0 | IO | DPCLK6 | | DIFFIO_R22p | N18 |
| B5 | VREFB5N0 | IO | | DEV_OE | DIFFIO_R21n | N22 |
| B5 | VREFB5N0 | IO | | DEV_CLRn | DIFFIO_R21p | N21 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R20n | M22 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R20p | M21 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R19n | M20 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R19p | M19 |
| B5 | VREFB5N0 | IO | | | | M16 |
| B5 | VREFB5N0 | CLK7 | DIFFCLK_3n | | | T22 |
| B5 | VREFB5N0 | CLK6 | DIFFCLK_3p | | | T21 |
| B6 | VREFB6N1 | CLK5 | DIFFCLK_2n | | | G22 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| B6 | VREFB6N1 | CLK4 | DIFFCLK_2p | | | G21 |
| B6 | VREFB6N1 | CONF_DONE | | CONF_DONE | | M18 |
| B6 | VREFB6N1 | MSEL0 | | MSEL0 | | M17 |
| B6 | VREFB6N1 | MSEL1 | | MSEL1 | | L18 |
| B6 | VREFB6N1 | MSEL2 | | MSEL2 | | L17 |
| B6 | VREFB6N1 | MSEL3 | | MSEL3 | | K20 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R18n | L16 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R18p | L15 |
| B6 | VREFB6N1 | IO | | INIT_DONE | DIFFIO_R17n | L22 |
| B6 | VREFB6N1 | IO | | CRC_ERROR | DIFFIO_R17p | L21 |
| B6 | VREFB6N1 | IO | | | | K15 |
| B6 | VREFB6N1 | IO | VREFB6N1 | | | K19 |
| B6 | VREFB6N1 | IO | | | | J15 |
| B6 | VREFB6N1 | IO | | nCEO | DIFFIO_R16n | K22 |
| B6 | VREFB6N1 | IO | | CLKUSR | DIFFIO_R16p | K21 |
| B6 | VREFB6N1 | IO | DPCLK7 | | DIFFIO_R15n | J22 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R15p | J21 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R14n | J16 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R14p | K16 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R13n | H22 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R13p | H21 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R12n | K17 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R12p | K18 |
| B6 | VREFB6N1 | IO | | | | J18 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R11n | F22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R11p | F21 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R10n | H20 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R10p | H19 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R9n | E22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R9p | E21 |
| B6 | VREFB6N0 | IO | VREFB6N0 | | | H18 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R8n | J17 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R8p | H16 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R7n | D22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R7p | D21 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R6n | F20 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| B6 | VREFB6N0 | IO | | | DIFFIO_R6p | F19 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R5n | G18 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R5p | H17 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R4n | C22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R4p | C21 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R3n | B22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R3p | B21 |
| B6 | VREFB6N0 | IO | CDPCLK5 | | DIFFIO_R2n | C20 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R2p | D20 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R1n | F17 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R1p | G17 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T32n | F16 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T32p | E16 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T31n | F15 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T31p | G16 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T30n | G15 |
| B7 | VREFB7N0 | IO | CDPCLK6 | | DIFFIO_T30p | F14 |
| B7 | VREFB7N0 | IO | | | | G14 |
| B7 | VREFB7N0 | IO | VREFB7N0 | | | D17 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T29n | C19 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T29p | D19 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTn | | | A20 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTp | | | B20 |
| B7 | VREFB7N0 | IO | | | | C17 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T28n | H15 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T28p | H14 |
| B7 | VREFB7N0 | IO | RUP4 | | | B19 |
| B7 | VREFB7N0 | IO | RDN4 | | | A19 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T27n | A18 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T27p | B18 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T26n | D15 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T26p | E15 |
| B7 | VREFB7N1 | IO | | | | G13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T25n | A17 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T25p | B17 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T24n | A16 |


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|---|---|---|---|---|---|---|
| B7 | VREFB7N1 | IO | | | DIFFIO_T24p | B16 |
| B7 | VREFB7N1 | IO | VREFB7N1 | | | C15 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T23n | E14 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T23p | F12 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T22n | H13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T22p | H12 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T21n | G12 |
| B7 | VREFB7N1 | IO | DPCLK8 | | DIFFIO_T21p | F13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T20n | A15 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T20p | B15 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T19n | C13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T19p | D13 |
| B7 | VREFB7N1 | IO | | | | E13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T18n | A14 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T18p | B14 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T17n | A13 |
| B7 | VREFB7N1 | IO | DPCLK9 | | DIFFIO_T17p | B13 |
| B7 | VREFB7N1 | IO | | | | E12 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T16n | E11 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T16p | F11 |
| B7 | VREFB7N1 | CLK8 | DIFFCLK_5n | | | A12 |
| B7 | VREFB7N1 | CLK9 | DIFFCLK_5p | | | B12 |
| B8 | VREFB8N0 | CLK10 | DIFFCLK_4n | | | A11 |
| B8 | VREFB8N0 | CLK11 | DIFFCLK_4p | | | B11 |
| B8 | VREFB8N0 | IO | | | | H11 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T15n | D10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T15p | E10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T14n | A10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T14p | B10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T13n | A9 |
| B8 | VREFB8N0 | IO | DPCLK10 | | DIFFIO_T13p | B9 |
| B8 | VREFB8N0 | IO | | | | C10 |
| B8 | VREFB8N0 | IO | | | | G11 |
| B8 | VREFB8N0 | IO | | DATA2 | DIFFIO_T12n | A8 |
| B8 | VREFB8N0 | IO | | DATA3 | DIFFIO_T12p | B8 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T11n | A7 |


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|---|---|---|---|---|---|---|
| B8 | VREFB8N0 | IO | | DATA4 | DIFFIO_T11p | B7 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T10n | A6 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T10p | B6 |
| B8 | VREFB8N0 | IO | VREFB8N0 | | | E9 |
| B8 | VREFB8N0 | IO | DPCLK11 | | DIFFIO_T9n | C8 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T9p | C7 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T8n | G10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T8p | G9 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T7n | H10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T7p | H9 |
| B8 | VREFB8N0 | IO | | DATA5 | | A5 |
| B8 | VREFB8N1 | IO | | | | B5 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T6n | F9 |
| B8 | VREFB8N1 | IO | | DATA6 | DIFFIO_T6p | F10 |
| B8 | VREFB8N1 | IO | | DATA7 | | C6 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T5n | A4 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T5p | B4 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T4n | F8 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T4p | G8 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T3n | A3 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T3p | B3 |
| B8 | VREFB8N1 | IO | VREFB8N1 | | | D6 |
| B8 | VREFB8N1 | IO | | | | E7 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T2n | C3 |
| B8 | VREFB8N1 | IO | CDPCLK7 | | DIFFIO_T2p | C4 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T1n | F7 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T1p | G7 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTn | | | E6 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTp | | | E5 |
| | | GND | | | | L10 |
| | | GND | | | | L11 |
| | | GND | | | | M10 |
| | | GND | | | | M11 |
| | | GND | | | | L12 |
| | | GND | | | | L13 |
| | | GND | | | | M12 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| | | GND | | | | M13 |
| | | GND | | | | N11 |
| | | GND | | | | K11 |
| | | GND | | | | N12 |
| | | GND | | | | K12 |
| | | GND | | | | K13 |
| | | GND | | | | N13 |
| | | GND | | | | N10 |
| | | GND | | | | K10 |
| | | GND | | | | J9 |
| | | GND | | | | D7 |
| | | GND | | | | J5 |
| | | GND | | | | H8 |
| | | GND | | | | A1 |
| | | GND | | | | C5 |
| | | GND | | | | C9 |
| | | GND | | | | C11 |
| | | GND | | | | C12 |
| | | GND | | | | C14 |
| | | GND | | | | C16 |
| | | GND | | | | A22 |
| | | GND | | | | E20 |
| | | GND | | | | G20 |
| | | GND | | | | L20 |
| | | GND | | | | P19 |
| | | GND | | | | V20 |
| | | GND | | | | Y20 |
| | | GND | | | | AB22 |
| | | GND | | | | Y18 |
| | | GND | | | | Y16 |
| | | GND | | | | Y12 |
| | | GND | | | | Y11 |
| | | GND | | | | Y9 |
| | | GND | | | | Y5 |
| | | GND | | | | AB1 |
| | | GND | | | | N3 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| | | GND | | | | U3 |
| | | GND | | | | W3 |
| | | GND | | | | D3 |
| | | GND | | | | F3 |
| | | GND | | | | K3 |
| | | GND | | | | AA2 |
| | | GND | | | | H3 |
| | | GND | | | | R3 |
| | | GND | | | | AB6 |
| | | GND | | | | Y15 |
| | | GND | | | | T20 |
| | | GND | | | | J19 |
| | | GND | | | | C18 |
| | | GND | | | | D8 |
| | | GND | | | | C1 |
| | | GND | | | | C2 |
| | | GND | | | | AA17 |
| | | GND | | | | AB17 |
| | | GND | | | | AA1 |
| | | GNDA1 | | | | U5 |
| | | GNDA2 | | | | E18 |
| | | GNDA3 | | | | F5 |
| | | GNDA4 | | | | V18 |
| | | VCCD_PLL1 | | | | U6 |
| | | VCCD_PLL2 | | | | E17 |
| | | VCCD_PLL3 | | | | F6 |
| | | VCCD_PLL4 | | | | V17 |
| | | VCCIO1 | | | | D4 |
| | | VCCIO1 | | | | F4 |
| | | VCCIO1 | | | | K4 |
| | | VCCIO1 | | | | H4 |
| | | VCCIO2 | | | | N4 |
| | | VCCIO2 | | | | U4 |
| | | VCCIO2 | | | | W4 |
| | | VCCIO2 | | | | R4 |
| | | VCCIO3 | | | | AB2 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| | | VCCIO3 | | | | W5 |
| | | VCCIO3 | | | | W9 |
| | | VCCIO3 | | | | W11 |
| | | VCCIO3 | | | | AA6 |
| | | VCCIO4 | | | | AB21 |
| | | VCCIO4 | | | | W12 |
| | | VCCIO4 | | | | W16 |
| | | VCCIO4 | | | | W18 |
| | | VCCIO4 | | | | Y14 |
| | | VCCIO5 | | | | P18 |
| | | VCCIO5 | | | | V19 |
| | | VCCIO5 | | | | Y19 |
| | | VCCIO5 | | | | T19 |
| | | VCCIO6 | | | | E19 |
| | | VCCIO6 | | | | G19 |
| | | VCCIO6 | | | | L19 |
| | | VCCIO6 | | | | J20 |
| | | VCCIO7 | | | | A21 |
| | | VCCIO7 | | | | D12 |
| | | VCCIO7 | | | | D14 |
| | | VCCIO7 | | | | D16 |
| | | VCCIO7 | | | | D18 |
| | | VCCIO8 | | | | A2 |
| | | VCCIO8 | | | | D5 |
| | | VCCIO8 | | | | D9 |
| | | VCCIO8 | | | | D11 |
| | | VCCIO8 | | | | E8 |
| | | VCCA1 | | | | T6 |
| | | VCCA2 | | | | F18 |
| | | VCCA3 | | | | G6 |
| | | VCCA4 | | | | U18 |
| | | VCCINT | | | | J11 |
| | | VCCINT | | | | J12 |
| | | VCCINT | | | | L14 |
| | | VCCINT | | | | M14 |
| | | VCCINT | | | | P11 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | F484 |
|---|---|---|---|---|---|---|
| | | VCCINT | | | | P12 |
| | | VCCINT | | | | L9 |
| | | VCCINT | | | | M9 |
| | | VCCINT | | | | J13 |
| | | VCCINT | | | | J14 |
| | | VCCINT | | | | K14 |
| | | VCCINT | | | | J10 |
| | | VCCINT | | | | K9 |
| | | VCCINT | | | | N9 |
| | | VCCINT | | | | P9 |
| | | VCCINT | | | | P10 |
| | | VCCINT | | | | P13 |
| | | VCCINT | | | | U16 |
| | | VCCINT | | | | U17 |
| | | VCCINT | | | | T13 |
| | | VCCINT | | | | J8 |

**Notes:**
(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
(2) For more information about pin definition and pin connection guidelines, refer to the
Cyclone 10 LP Device Family Pin Connection Guidelines.


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B1 | VREFB1N0 | IO | | | | H5 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L1p | B2 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L1n | B1 |
| B1 | VREFB1N0 | IO | | | | G5 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L2p | E4 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L2n | E3 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L4p | D2 |
| B1 | VREFB1N0 | IO | | DATA1,ASDO | DIFFIO_L4n | D1 |
| B1 | VREFB1N0 | IO | VREFB1N0 | | | H7 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L5p | H6 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L5n | J6 |
| B1 | VREFB1N0 | IO | | FLASH_nCE,nCSO | DIFFIO_L6p | E2 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L6n | E1 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L7p | F2 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L7n | F1 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L8p | G4 |
| B1 | VREFB1N0 | IO | | | DIFFIO_L8n | G3 |
| B1 | VREFB1N1 | nSTATUS | | nSTATUS | | K6 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L9p | L8 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L9n | K8 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L10p | J7 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L10n | K7 |
| B1 | VREFB1N1 | IO | DPCLK0 | | | J4 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L11p | H2 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L11n | H1 |
| B1 | VREFB1N1 | IO | VREFB1N1 | | | J3 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L12p | J2 |
| B1 | VREFB1N1 | IO | | | DIFFIO_L12n | J1 |
| B1 | VREFB1N1 | IO | | DCLK | | K2 |
| B1 | VREFB1N1 | IO | | DATA0 | | K1 |
| B1 | VREFB1N1 | nCONFIG | | nCONFIG | | K5 |
| B1 | VREFB1N1 | TDI | | TDI | | L5 |
| B1 | VREFB1N1 | TCK | | TCK | | L2 |
| B1 | VREFB1N1 | TMS | | TMS | | L1 |
| B1 | VREFB1N1 | TDO | | TDO | | L4 |
| B1 | VREFB1N1 | nCE | | nCE | | L3 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B1 | VREFB1N1 | CLK0 | DIFFCLK_0p | | | G2 |
| B1 | VREFB1N1 | CLK1 | DIFFCLK_0n | | | G1 |
| B2 | VREFB2N0 | CLK2 | DIFFCLK_1p | | | T2 |
| B2 | VREFB2N0 | CLK3 | DIFFCLK_1n | | | T1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L13p | L6 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L13n | M6 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L14p | M2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L14n | M1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L15p | M4 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L15n | M3 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L16p | N2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L16n | N1 |
| B2 | VREFB2N0 | IO | | | | L7 |
| B2 | VREFB2N0 | IO | VREFB2N0 | | | M5 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L17p | P2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L17n | P1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L18p | R2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L18n | R1 |
| B2 | VREFB2N0 | IO | | | | N5 |
| B2 | VREFB2N0 | IO | DPCLK1 | | DIFFIO_L19p | P4 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L19n | P3 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L20p | U2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L20n | U1 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L21p | V2 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L21n | V1 |
| B2 | VREFB2N0 | IO | | | | P5 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L22p | N6 |
| B2 | VREFB2N0 | IO | | | DIFFIO_L22n | M7 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L23p | M8 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L23n | N8 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L24p | W2 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L24n | W1 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L25p | Y2 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L25n | Y1 |
| B2 | VREFB2N1 | IO | VREFB2N1 | | | T3 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L26p | N7 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B2 | VREFB2N1 | IO | | | DIFFIO_L26n | P7 |
| B2 | VREFB2N1 | IO | RUP1 | | | V4 |
| B2 | VREFB2N1 | IO | RDN1 | | | V3 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L28p | P6 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L28n | R5 |
| B2 | VREFB2N1 | IO | CDPCLK1 | | | T4 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L29p | T5 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L29n | R6 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L30p | R7 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L30n | T7 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L31p | P8 |
| B2 | VREFB2N1 | IO | | | DIFFIO_L31n | R8 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B1p | R9 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B1n | T8 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B2p | R10 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B2n | T9 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B3p | V6 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B3n | V5 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B4p | U7 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B4n | U8 |
| B3 | VREFB3N1 | IO | VREFB3N1 | | | Y4 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B5p | R11 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B5n | R12 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B6p | Y3 |
| B3 | VREFB3N1 | IO | CDPCLK2 | | | Y6 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTp | | | AA3 |
| B3 | VREFB3N1 | IO | PLL1_CLKOUTn | | | AB3 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B7p | W6 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B7n | V7 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B8p | AA4 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B8n | AB4 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B9p | AA5 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B9n | AB5 |
| B3 | VREFB3N1 | IO | | | DIFFIO_B10p | W7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B10n | Y7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B11p | U9 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B3 | VREFB3N0 | IO | | | DIFFIO_B11n | V8 |
| B3 | VREFB3N0 | IO | | | | W8 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B12p | AA7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B12n | AB7 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B13p | Y8 |
| B3 | VREFB3N0 | IO | VREFB3N0 | | | V9 |
| B3 | VREFB3N0 | IO | DPCLK2 | | | V10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B14p | T10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B14n | U10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B15p | AA8 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B15n | AB8 |
| B3 | VREFB3N0 | IO | | | | T11 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B16p | AA9 |
| B3 | VREFB3N0 | IO | DPCLK3 | | DIFFIO_B16n | AB9 |
| B3 | VREFB3N0 | IO | | | | U11 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B17p | V11 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B17n | W10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18p | Y10 |
| B3 | VREFB3N0 | IO | | | DIFFIO_B18n | AA10 |
| B3 | VREFB3N0 | IO | | | | AB10 |
| B3 | VREFB3N0 | CLK15 | DIFFCLK_6p | | | AA11 |
| B3 | VREFB3N0 | CLK14 | DIFFCLK_6n | | | AB11 |
| B4 | VREFB4N1 | CLK13 | DIFFCLK_7p | | | AA12 |
| B4 | VREFB4N1 | CLK12 | DIFFCLK_7n | | | AB12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B19p | AA13 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B19n | AB13 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B20p | AA14 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B20n | AB14 |
| B4 | VREFB4N1 | IO | | | | V12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B21p | W13 |
| B4 | VREFB4N1 | IO | DPCLK4 | | DIFFIO_B21n | Y13 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B22p | AA15 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B22n | AB15 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B23p | U12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B23n | T12 |
| B4 | VREFB4N1 | IO | | | DIFFIO_B24p | AA16 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B4 | VREFB4N1 | IO | | | DIFFIO_B24n | AB16 |
| B4 | VREFB4N1 | IO | | | | R13 |
| B4 | VREFB4N1 | IO | DPCLK5 | | | V13 |
| B4 | VREFB4N1 | IO | VREFB4N1 | | | W14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B26p | U13 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B26n | V14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B27p | V15 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B27n | W15 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B28p | T14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B28n | T15 |
| B4 | VREFB4N0 | IO | | | | AB18 |
| B4 | VREFB4N0 | IO | | | | AA18 |
| B4 | VREFB4N0 | IO | RUP2 | | | AA19 |
| B4 | VREFB4N0 | IO | RDN2 | | | AB19 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B29p | W17 |
| B4 | VREFB4N0 | IO | CDPCLK3 | | DIFFIO_B29n | Y17 |
| B4 | VREFB4N0 | IO | VREFB4N0 | | | V16 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B30p | AA20 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B30n | AB20 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTp | | | T16 |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTn | | | R16 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B31p | U15 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B31n | U14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B32p | R14 |
| B4 | VREFB4N0 | IO | | | DIFFIO_B32n | R15 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R35n | AA22 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R35p | AA21 |
| B5 | VREFB5N1 | IO | | | | P14 |
| B5 | VREFB5N1 | IO | RUP3 | | | T17 |
| B5 | VREFB5N1 | IO | RDN3 | | | T18 |
| B5 | VREFB5N1 | IO | CDPCLK4 | | DIFFIO_R34n | W20 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R34p | W19 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R33n | Y22 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R33p | Y21 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R32n | U20 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R32p | U19 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B5 | VREFB5N1 | IO | | | | N14 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R31n | W22 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R31p | W21 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R30n | P15 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R30p | P16 |
| B5 | VREFB5N1 | IO | VREFB5N1 | | | R17 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R29n | M15 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R29p | N15 |
| B5 | VREFB5N1 | IO | | | | P17 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R28n | V22 |
| B5 | VREFB5N1 | IO | | | DIFFIO_R28p | V21 |
| B5 | VREFB5N1 | IO | | | | R20 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R27n | U22 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R27p | U21 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R26n | R18 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R26p | R19 |
| B5 | VREFB5N0 | IO | | | | N16 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R25n | R22 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R25p | R21 |
| B5 | VREFB5N0 | IO | VREFB5N0 | | | P20 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R24n | P22 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R24p | P21 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R23n | N20 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R23p | N19 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R22n | N17 |
| B5 | VREFB5N0 | IO | DPCLK6 | | DIFFIO_R22p | N18 |
| B5 | VREFB5N0 | IO | | DEV_OE | DIFFIO_R21n | N22 |
| B5 | VREFB5N0 | IO | | DEV_CLRn | DIFFIO_R21p | N21 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R20n | M22 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R20p | M21 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R19n | M20 |
| B5 | VREFB5N0 | IO | | | DIFFIO_R19p | M19 |
| B5 | VREFB5N0 | IO | | | | M16 |
| B5 | VREFB5N0 | CLK7 | DIFFCLK_3n | | | T22 |
| B5 | VREFB5N0 | CLK6 | DIFFCLK_3p | | | T21 |
| B6 | VREFB6N1 | CLK5 | DIFFCLK_2n | | | G22 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B6 | VREFB6N1 | CLK4 | DIFFCLK_2p | | | G21 |
| B6 | VREFB6N1 | CONF_DONE | | CONF_DONE | | M18 |
| B6 | VREFB6N1 | MSEL0 | | MSEL0 | | M17 |
| B6 | VREFB6N1 | MSEL1 | | MSEL1 | | L18 |
| B6 | VREFB6N1 | MSEL2 | | MSEL2 | | L17 |
| B6 | VREFB6N1 | MSEL3 | | MSEL3 | | K20 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R18n | L16 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R18p | L15 |
| B6 | VREFB6N1 | IO | | INIT_DONE | DIFFIO_R17n | L22 |
| B6 | VREFB6N1 | IO | | CRC_ERROR | DIFFIO_R17p | L21 |
| B6 | VREFB6N1 | IO | | | | K15 |
| B6 | VREFB6N1 | IO | VREFB6N1 | | | K19 |
| B6 | VREFB6N1 | IO | | | | J15 |
| B6 | VREFB6N1 | IO | | nCEO | DIFFIO_R16n | K22 |
| B6 | VREFB6N1 | IO | | CLKUSR | DIFFIO_R16p | K21 |
| B6 | VREFB6N1 | IO | DPCLK7 | | DIFFIO_R15n | J22 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R15p | J21 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R14n | J16 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R14p | K16 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R13n | H22 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R13p | H21 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R12n | K17 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R12p | K18 |
| B6 | VREFB6N1 | IO | | | | J18 |
| B6 | VREFB6N1 | IO | | | DIFFIO_R11n | F22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R11p | F21 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R10n | H20 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R10p | H19 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R9n | E22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R9p | E21 |
| B6 | VREFB6N0 | IO | VREFB6N0 | | | H18 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R8n | J17 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R8p | H16 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R7n | D22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R7p | D21 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R6n | F20 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B6 | VREFB6N0 | IO | | | DIFFIO_R6p | F19 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R5n | G18 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R5p | H17 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R4n | C22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R4p | C21 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R3n | B22 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R3p | B21 |
| B6 | VREFB6N0 | IO | CDPCLK5 | | DIFFIO_R2n | C20 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R2p | D20 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R1n | F17 |
| B6 | VREFB6N0 | IO | | | DIFFIO_R1p | G17 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T32n | F16 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T32p | E16 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T31n | F15 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T31p | G16 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T30n | G15 |
| B7 | VREFB7N0 | IO | CDPCLK6 | | DIFFIO_T30p | F14 |
| B7 | VREFB7N0 | IO | | | | G14 |
| B7 | VREFB7N0 | IO | VREFB7N0 | | | D17 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T29n | C19 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T29p | D19 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTn | | | A20 |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTp | | | B20 |
| B7 | VREFB7N0 | IO | | | | C17 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T28n | H15 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T28p | H14 |
| B7 | VREFB7N0 | IO | RUP4 | | | B19 |
| B7 | VREFB7N0 | IO | RDN4 | | | A19 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T27n | A18 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T27p | B18 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T26n | D15 |
| B7 | VREFB7N0 | IO | | | DIFFIO_T26p | E15 |
| B7 | VREFB7N1 | IO | | | | G13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T25n | A17 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T25p | B17 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T24n | A16 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B7 | VREFB7N1 | IO | | | DIFFIO_T24p | B16 |
| B7 | VREFB7N1 | IO | VREFB7N1 | | | C15 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T23n | E14 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T23p | F12 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T22n | H13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T22p | H12 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T21n | G12 |
| B7 | VREFB7N1 | IO | DPCLK8 | | DIFFIO_T21p | F13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T20n | A15 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T20p | B15 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T19n | C13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T19p | D13 |
| B7 | VREFB7N1 | IO | | | | E13 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T18n | A14 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T18p | B14 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T17n | A13 |
| B7 | VREFB7N1 | IO | DPCLK9 | | DIFFIO_T17p | B13 |
| B7 | VREFB7N1 | IO | | | | E12 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T16n | E11 |
| B7 | VREFB7N1 | IO | | | DIFFIO_T16p | F11 |
| B7 | VREFB7N1 | CLK8 | DIFFCLK_5n | | | A12 |
| B7 | VREFB7N1 | CLK9 | DIFFCLK_5p | | | B12 |
| B8 | VREFB8N0 | CLK10 | DIFFCLK_4n | | | A11 |
| B8 | VREFB8N0 | CLK11 | DIFFCLK_4p | | | B11 |
| B8 | VREFB8N0 | IO | | | | H11 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T15n | D10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T15p | E10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T14n | A10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T14p | B10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T13n | A9 |
| B8 | VREFB8N0 | IO | DPCLK10 | | DIFFIO_T13p | B9 |
| B8 | VREFB8N0 | IO | | | | C10 |
| B8 | VREFB8N0 | IO | | | | G11 |
| B8 | VREFB8N0 | IO | | DATA2 | DIFFIO_T12n | A8 |
| B8 | VREFB8N0 | IO | | DATA3 | DIFFIO_T12p | B8 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T11n | A7 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| B8 | VREFB8N0 | IO | | DATA4 | DIFFIO_T11p | B7 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T10n | A6 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T10p | B6 |
| B8 | VREFB8N0 | IO | VREFB8N0 | | | E9 |
| B8 | VREFB8N0 | IO | DPCLK11 | | DIFFIO_T9n | C8 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T9p | C7 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T8n | G10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T8p | G9 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T7n | H10 |
| B8 | VREFB8N0 | IO | | | DIFFIO_T7p | H9 |
| B8 | VREFB8N0 | IO | | DATA5 | | A5 |
| B8 | VREFB8N1 | IO | | | | B5 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T6n | F9 |
| B8 | VREFB8N1 | IO | | DATA6 | DIFFIO_T6p | F10 |
| B8 | VREFB8N1 | IO | | DATA7 | | C6 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T5n | A4 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T5p | B4 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T4n | F8 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T4p | G8 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T3n | A3 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T3p | B3 |
| B8 | VREFB8N1 | IO | VREFB8N1 | | | D6 |
| B8 | VREFB8N1 | IO | | | | E7 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T2n | C3 |
| B8 | VREFB8N1 | IO | CDPCLK7 | | DIFFIO_T2p | C4 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T1n | F7 |
| B8 | VREFB8N1 | IO | | | DIFFIO_T1p | G7 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTn | | | E6 |
| B8 | VREFB8N1 | IO | PLL3_CLKOUTp | | | E5 |
| | | GND | | | | L10 |
| | | GND | | | | L11 |
| | | GND | | | | M10 |
| | | GND | | | | M11 |
| | | GND | | | | L12 |
| | | GND | | | | L13 |
| | | GND | | | | M12 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| | | GND | | | | M13 |
| | | GND | | | | N11 |
| | | GND | | | | K11 |
| | | GND | | | | N12 |
| | | GND | | | | K12 |
| | | GND | | | | K13 |
| | | GND | | | | N13 |
| | | GND | | | | N10 |
| | | GND | | | | K10 |
| | | GND | | | | J9 |
| | | GND | | | | D7 |
| | | GND | | | | J5 |
| | | GND | | | | H8 |
| | | GND | | | | A1 |
| | | GND | | | | C5 |
| | | GND | | | | C9 |
| | | GND | | | | C11 |
| | | GND | | | | C12 |
| | | GND | | | | C14 |
| | | GND | | | | C16 |
| | | GND | | | | A22 |
| | | GND | | | | E20 |
| | | GND | | | | G20 |
| | | GND | | | | L20 |
| | | GND | | | | P19 |
| | | GND | | | | V20 |
| | | GND | | | | Y20 |
| | | GND | | | | AB22 |
| | | GND | | | | Y18 |
| | | GND | | | | Y16 |
| | | GND | | | | Y12 |
| | | GND | | | | Y11 |
| | | GND | | | | Y9 |
| | | GND | | | | Y5 |
| | | GND | | | | AB1 |
| | | GND | | | | N3 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| | | GND | | | | U3 |
| | | GND | | | | W3 |
| | | GND | | | | D3 |
| | | GND | | | | F3 |
| | | GND | | | | K3 |
| | | GND | | | | AA2 |
| | | GND | | | | H3 |
| | | GND | | | | R3 |
| | | GND | | | | AB6 |
| | | GND | | | | Y15 |
| | | GND | | | | T20 |
| | | GND | | | | J19 |
| | | GND | | | | C18 |
| | | GND | | | | D8 |
| | | GND | | | | C1 |
| | | GND | | | | C2 |
| | | GND | | | | AA17 |
| | | GND | | | | AB17 |
| | | GND | | | | AA1 |
| | | GNDA1 | | | | U5 |
| | | GNDA2 | | | | E18 |
| | | GNDA3 | | | | F5 |
| | | GNDA4 | | | | V18 |
| | | VCCD_PLL1 | | | | U6 |
| | | VCCD_PLL2 | | | | E17 |
| | | VCCD_PLL3 | | | | F6 |
| | | VCCD_PLL4 | | | | V17 |
| | | VCCIO1 | | | | D4 |
| | | VCCIO1 | | | | F4 |
| | | VCCIO1 | | | | K4 |
| | | VCCIO1 | | | | H4 |
| | | VCCIO2 | | | | N4 |
| | | VCCIO2 | | | | U4 |
| | | VCCIO2 | | | | W4 |
| | | VCCIO2 | | | | R4 |
| | | VCCIO3 | | | | AB2 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| | | VCCIO3 | | | | W5 |
| | | VCCIO3 | | | | W9 |
| | | VCCIO3 | | | | W11 |
| | | VCCIO3 | | | | AA6 |
| | | VCCIO4 | | | | AB21 |
| | | VCCIO4 | | | | W12 |
| | | VCCIO4 | | | | W16 |
| | | VCCIO4 | | | | W18 |
| | | VCCIO4 | | | | Y14 |
| | | VCCIO5 | | | | P18 |
| | | VCCIO5 | | | | V19 |
| | | VCCIO5 | | | | Y19 |
| | | VCCIO5 | | | | T19 |
| | | VCCIO6 | | | | E19 |
| | | VCCIO6 | | | | G19 |
| | | VCCIO6 | | | | L19 |
| | | VCCIO6 | | | | J20 |
| | | VCCIO7 | | | | A21 |
| | | VCCIO7 | | | | D12 |
| | | VCCIO7 | | | | D14 |
| | | VCCIO7 | | | | D16 |
| | | VCCIO7 | | | | D18 |
| | | VCCIO8 | | | | A2 |
| | | VCCIO8 | | | | D5 |
| | | VCCIO8 | | | | D9 |
| | | VCCIO8 | | | | D11 |
| | | VCCIO8 | | | | E8 |
| | | VCCA1 | | | | T6 |
| | | VCCA2 | | | | F18 |
| | | VCCA3 | | | | G6 |
| | | VCCA4 | | | | U18 |
| | | VCCINT | | | | J11 |
| | | VCCINT | | | | J12 |
| | | VCCINT | | | | L14 |
| | | VCCINT | | | | M14 |
| | | VCCINT | | | | P11 |


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| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Emulated LVDS Output Channel | U484 |
|---|---|---|---|---|---|---|
| | | VCCINT | | | | P12 |
| | | VCCINT | | | | L9 |
| | | VCCINT | | | | M9 |
| | | VCCINT | | | | J13 |
| | | VCCINT | | | | J14 |
| | | VCCINT | | | | K14 |
| | | VCCINT | | | | J10 |
| | | VCCINT | | | | K9 |
| | | VCCINT | | | | N9 |
| | | VCCINT | | | | P9 |
| | | VCCINT | | | | P10 |
| | | VCCINT | | | | P13 |
| | | VCCINT | | | | U16 |
| | | VCCINT | | | | U17 |
| | | VCCINT | | | | T13 |
| | | VCCINT | | | | J8 |

**Notes:**
(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.


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| Date | Version | Changes |
|---|---|---|
| February 2017 | 2017.02.13 | Initial release. |
| March 2017 | 2017.03.16 | Added Pin List U484. |
| May 2017 | 2017.05.19 | Updated description for the Configuration pins. |
| March 2019 | 2019.03.29 | Added DPCLK and CDPCLK support in optional pin function column. |


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