Pin Information for the Intel® Cyclone®10 10CL006 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	E144 (3)
B1	VREFB1N0	IO				1
B1	VREFB1N0	IO				2
B1	VREFB1N0	IO				3
B1	VREFB1N0	IO		DATA1,ASDO	DIFFIO_L1n	6
B1	VREFB1N0	IO	VREFB1N0			7
B1	VREFB1N0	IO		FLASH_nCE,nCSO	DIFFIO_L2p	8
B1	VREFB1N0	nSTATUS		nSTATUS		9
B1	VREFB1N0	IO	DPCLK0		DIFFIO_L4p	10
B1	VREFB1N0	IO			DIFFIO_L4n	11
B1	VREFB1N0	IO		DCLK		12
B1	VREFB1N0	IO		DATA0		13
B1	VREFB1N0	nCONFIG		nCONFIG		14
B1	VREFB1N0	TDI		TDI		15
B1	VREFB1N0	TCK		TCK		16
B1	VREFB1N0	TMS		TMS		18
B1	VREFB1N0	TDO		TDO		20
B1	VREFB1N0	nCE		nCE		21
B1	VREFB1N0	CLK0	DIFFCLK_0p			22
B1	VREFB1N0	CLK1	DIFFCLK_0n			23
B2	VREFB2N0	CLK2	DIFFCLK_1p			24
B2	VREFB2N0	CLK3	DIFFCLK_1n			25
B2	VREFB2N0	IO			DIFFIO_L6n	28
B2	VREFB2N0	IO	VREFB2N0			31
B2	VREFB2N0	IO	RUP1			32
B2	VREFB2N0	IO	RDN1			33
B2	VREFB2N0	IO				34
B3	VREFB3N0	IO			DIFFIO_B1p	38
B3	VREFB3N0	IO			DIFFIO_B1n	39
B3	VREFB3N0	IO	DPCLK2			42
B3	VREFB3N0	IO	PLL1_CLKOUTp			43
B3	VREFB3N0	IO	PLL1_CLKOUTn			44
B3	VREFB3N0	IO	VREFB3N0			46
B3	VREFB3N0	IO			DIFFIO_B9p	49
B3	VREFB3N0	IO			DIFFIO_B9n	50
B3	VREFB3N0	IO			DIFFIO_B10p	51

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Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	E144 (3)
B3	VREFB3N0	IO			DIFFIO_B11p	52
B3	VREFB3N0	IO			DIFFIO_B11n	53
B4	VREFB4N0	IO			DIFFIO_B12p	54
B4	VREFB4N0	IO			DIFFIO_B12n	55
B4	VREFB4N0	IO			DIFFIO_B15p	58
B4	VREFB4N0	IO			DIFFIO_B16p	59
B4	VREFB4N0	IO			DIFFIO_B16n	60
B4	VREFB4N0	IO	VREFB4N0			65
B4	VREFB4N0	IO	RUP2			66
B4	VREFB4N0	IO	RDN2			67
B4	VREFB4N0	IO	DPCLK3		DIFFIO_B20n	68
B4	VREFB4N0	IO				69
B4	VREFB4N0	IO			DIFFIO_B21p	70
B4	VREFB4N0	IO			DIFFIO_B21n	71
B4	VREFB4N0	IO			DIFFIO_B22p	72
B5	VREFB5N0	IO				73
B5	VREFB5N0	IO				74
B5	VREFB5N0	IO				75
B5	VREFB5N0	IO	RUP3			76
B5	VREFB5N0	IO	RDN3			77
B5	VREFB5N0	IO	VREFB5N0			80
B5	VREFB5N0	IO				83
B5	VREFB5N0	IO			DIFFIO_R8n	84
B5	VREFB5N0	IO	DPCLK4		DIFFIO_R8p	85
B5	VREFB5N0	IO		DEV_OE	DIFFIO_R7n	86
B5	VREFB5N0	IO		DEV_CLRn	DIFFIO_R7p	87
B5	VREFB5N0	CLK7	DIFFCLK_3n			88
B5	VREFB5N0	CLK6	DIFFCLK_3p			89
B6	VREFB6N0	CLK5	DIFFCLK_2n			90
B6	VREFB6N0	CLK4	DIFFCLK_2p			91
B6	VREFB6N0	CONF_DONE		CONF_DONE		92
B6	VREFB6N0	MSEL0		MSEL0		94
B6	VREFB6N0	MSEL1		MSEL1		96
B6	VREFB6N0	MSEL2		MSEL2		97
B6	VREFB6N0	IO		INIT_DONE	DIFFIO_R4n	98

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	E144 (3)
B6	VREFB6N0	IO		CRC_ERROR	DIFFIO_R4p	99
B6	VREFB6N0	IO				100
B6	VREFB6N0	IO		nCEO	DIFFIO_R3n	101
B6	VREFB6N0	IO		CLKUSR	DIFFIO_R3p	103
B6	VREFB6N0	IO	VREFB6N0			105
B6	VREFB6N0	IO			DIFFIO_R1n	106
B7	VREFB7N0	IO			DIFFIO_T19p	111
B7	VREFB7N0	IO	PLL2_CLKOUTn			112
B7	VREFB7N0	IO	PLL2_CLKOUTp			113
B7	VREFB7N0	IO	RUP4			114
B7	VREFB7N0	IO	RDN4			115
B7	VREFB7N0	IO	VREFB7N0			119
B7	VREFB7N0	IO			DIFFIO_T16n	120
B7	VREFB7N0	IO			DIFFIO_T16p	121
B7	VREFB7N0	IO			DIFFIO_T13p	124
B7	VREFB7N0	IO				125
B7	VREFB7N0	IO			DIFFIO_T12n	126
B7	VREFB7N0	IO			DIFFIO_T12p	127
B8	VREFB8N0	IO			DIFFIO_T11n	128
B8	VREFB8N0	IO			DIFFIO_T11p	129
B8	VREFB8N0	IO		DATA2	DIFFIO_T10n	132
B8	VREFB8N0	IO		DATA3	DIFFIO_T10p	133
B8	VREFB8N0	IO			DIFFIO_T8n	135
B8	VREFB8N0	IO	VREFB8N0			136
B8	VREFB8N0	IO		DATA5		137
B8	VREFB8N0	IO		DATA6		138
B8	VREFB8N0	IO			DIFFIO_T5p	141
B8	VREFB8N0	IO	DPCLK7		DIFFIO_T2p	142
B8	VREFB8N0	IO			DIFFIO_T1n	143
B8	VREFB8N0	IO			DIFFIO_T1p	144
		GND				19
		GND				27
		GND				41
		GND				48
		GND				57

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	E144 (3)
		GND				63
		GND				82
		GND				95
		GND				118
		GND				123
		GND				131
		GND				140
		GND				4
		GND				79
		GND				30
		GND				64
		GND				104
		GND				110
		GNDA1				36
		GNDA2				108
		VCCD_PLL1				37
		VCCD_PLL2				109
		VCCIO1				17
		VCCIO2				26
		VCCIO3				40
		VCCIO3				47
		VCCIO4				56
		VCCIO4				62
		VCCIO5				81
		VCCIO6				93
		VCCIO7				117
		VCCIO7				122
		VCCIO8				130
		VCCIO8				139
		VCCA1				35
		VCCA2				107
		VCCINT				5
		VCCINT				29
		VCCINT				45
		VCCINT				61

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	E144 (3)
		VCCINT				78
		VCCINT				102
		VCCINT				116
		VCCINT				134

Notes:

(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(2) For more information about pin definition and pin connection guidelines, refer to the Intel Cyclone 10 LP Device Family Pin Connection Guidelines.

(3) The E144 package has an exposed pad at the bottom of the package.
This exposed pad is a ground pad that must be connected to the ground plane on your PCB.
This exposed pad is used for electrical connectivity, and not for thermal purposes.

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U256
B1	VREFB1N0	IO				D4
B1	VREFB1N0	IO				E5
B1	VREFB1N0	IO				F5
B1	VREFB1N0	IO				B1
B1	VREFB1N0	IO			DIFFIO_L1p	C2
B1	VREFB1N0	IO		DATA1,ASDO	DIFFIO_L1n	C1
B1	VREFB1N0	IO	VREFB1N0			F3
B1	VREFB1N0	IO		FLASH_nCE,nCSO	DIFFIO_L2p	D2
B1	VREFB1N0	IO			DIFFIO_L2n	D1
B1	VREFB1N0	nSTATUS		nSTATUS		F4
B1	VREFB1N0	IO	DPCLK0		DIFFIO_L4p	G2
B1	VREFB1N0	IO			DIFFIO_L4n	G1
B1	VREFB1N0	IO		DCLK		H1
B1	VREFB1N0	IO		DATA0		H2
B1	VREFB1N0	nCONFIG		nCONFIG		H5
B1	VREFB1N0	TDI		TDI		H4
B1	VREFB1N0	TCK		TCK		H3
B1	VREFB1N0	TMS		TMS		J5
B1	VREFB1N0	TDO		TDO		J4
B1	VREFB1N0	nCE		nCE		J3
B1	VREFB1N0	CLK0	DIFFCLK_0p			E2
B1	VREFB1N0	CLK1	DIFFCLK_0n			E1
B2	VREFB2N0	CLK2	DIFFCLK_1p			M2
B2	VREFB2N0	CLK3	DIFFCLK_1n			M1
B2	VREFB2N0	IO			DIFFIO_L5p	J2
B2	VREFB2N0	IO			DIFFIO_L5n	J1
B2	VREFB2N0	IO				J6
B2	VREFB2N0	IO			DIFFIO_L6p	K6
B2	VREFB2N0	IO			DIFFIO_L6n	L6
B2	VREFB2N0	IO			DIFFIO_L7p	K2
B2	VREFB2N0	IO			DIFFIO_L7n	K1
B2	VREFB2N0	IO	DPCLK1		DIFFIO_L8p	L2
B2	VREFB2N0	IO			DIFFIO_L8n	L1
B2	VREFB2N0	IO	VREFB2N0			L3
B2	VREFB2N0	IO			DIFFIO_L9p	N2

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U256
B2	VREFB2N0	IO			DIFFIO_L9n	N1
B2	VREFB2N0	IO	RUP1			K5
B2	VREFB2N0	IO	RDN1			L4
B2	VREFB2N0	IO				R1
B2	VREFB2N0	IO			DIFFIO_L10p	P2
B2	VREFB2N0	IO			DIFFIO_L10n	P1
B3	VREFB3N0	IO			DIFFIO_B1p	N3
B3	VREFB3N0	IO			DIFFIO_B1n	P3
B3	VREFB3N0	IO			DIFFIO_B2p	R3
B3	VREFB3N0	IO			DIFFIO_B2n	T3
B3	VREFB3N0	IO	DPCLK2			T2
B3	VREFB3N0	IO	PLL1_CLKOUTp			R4
B3	VREFB3N0	IO	PLL1_CLKOUTn			T4
B3	VREFB3N0	IO			DIFFIO_B4p	N5
B3	VREFB3N0	IO			DIFFIO_B4n	N6
B3	VREFB3N0	IO				M6
B3	VREFB3N0	IO	VREFB3N0			P6
B3	VREFB3N0	IO			DIFFIO_B5p	M7
B3	VREFB3N0	IO			DIFFIO_B5n	K8
B3	VREFB3N0	IO			DIFFIO_B6p	R5
B3	VREFB3N0	IO			DIFFIO_B6n	T5
B3	VREFB3N0	IO			DIFFIO_B7p	R6
B3	VREFB3N0	IO			DIFFIO_B7n	T6
B3	VREFB3N0	IO				L7
B3	VREFB3N0	IO			DIFFIO_B8p	R7
B3	VREFB3N0	IO			DIFFIO_B8n	T7
B3	VREFB3N0	IO			DIFFIO_B9p	L8
B3	VREFB3N0	IO			DIFFIO_B9n	M8
B3	VREFB3N0	IO			DIFFIO_B10p	N8
B3	VREFB3N0	IO			DIFFIO_B10n	P8
B3	VREFB3N0	IO			DIFFIO_B11p	R8
B3	VREFB3N0	IO			DIFFIO_B11n	T8
B4	VREFB4N0	IO			DIFFIO_B12p	R9
B4	VREFB4N0	IO			DIFFIO_B12n	T9
B4	VREFB4N0	IO			DIFFIO_B13p	K9

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U256
B4	VREFB4N0	IO			DIFFIO_B13n	L9
B4	VREFB4N0	IO			DIFFIO_B14p	M9
B4	VREFB4N0	IO			DIFFIO_B14n	N9
B4	VREFB4N0	IO			DIFFIO_B15p	R10
B4	VREFB4N0	IO			DIFFIO_B15n	T10
B4	VREFB4N0	IO			DIFFIO_B16p	R11
B4	VREFB4N0	IO			DIFFIO_B16n	T11
B4	VREFB4N0	IO			DIFFIO_B17p	R12
B4	VREFB4N0	IO			DIFFIO_B17n	T12
B4	VREFB4N0	IO			DIFFIO_B18p	K10
B4	VREFB4N0	IO			DIFFIO_B18n	L10
B4	VREFB4N0	IO				P9
B4	VREFB4N0	IO	VREFB4N0			P11
B4	VREFB4N0	IO			DIFFIO_B19p	R13
B4	VREFB4N0	IO			DIFFIO_B19n	T13
B4	VREFB4N0	IO	RUP2			M10
B4	VREFB4N0	IO	RDN2			N11
B4	VREFB4N0	IO			DIFFIO_B20p	T14
B4	VREFB4N0	IO	DPCLK3		DIFFIO_B20n	T15
B4	VREFB4N0	IO				R14
B4	VREFB4N0	IO			DIFFIO_B21p	P14
B4	VREFB4N0	IO			DIFFIO_B21n	L11
B4	VREFB4N0	IO			DIFFIO_B22p	M11
B4	VREFB4N0	IO			DIFFIO_B22n	N12
B5	VREFB5N0	IO				N13
B5	VREFB5N0	IO				M12
B5	VREFB5N0	IO				L12
B5	VREFB5N0	IO				K12
B5	VREFB5N0	IO	RUP3			N14
B5	VREFB5N0	IO	RDN3			P15
B5	VREFB5N0	IO			DIFFIO_R11n	P16
B5	VREFB5N0	IO			DIFFIO_R11p	R16
B5	VREFB5N0	IO				K11
B5	VREFB5N0	IO			DIFFIO_R10n	N16
B5	VREFB5N0	IO			DIFFIO_R10p	N15

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U256
B5	VREFB5N0	IO	VREFB5N0			L14
B5	VREFB5N0	IO				L13
B5	VREFB5N0	IO			DIFFIO_R9n	L16
B5	VREFB5N0	IO			DIFFIO_R9p	L15
B5	VREFB5N0	IO				J11
B5	VREFB5N0	IO			DIFFIO_R8n	K16
B5	VREFB5N0	IO	DPCLK4		DIFFIO_R8p	K15
B5	VREFB5N0	IO		DEV_OE	DIFFIO_R7n	J16
B5	VREFB5N0	IO		DEV_CLRn	DIFFIO_R7p	J15
B5	VREFB5N0	IO			DIFFIO_R6n	J14
B5	VREFB5N0	IO			DIFFIO_R6p	J12
B5	VREFB5N0	IO				J13
B5	VREFB5N0	CLK7	DIFFCLK_3n			M16
B5	VREFB5N0	CLK6	DIFFCLK_3p			M15
B6	VREFB6N0	CLK5	DIFFCLK_2n			E16
B6	VREFB6N0	CLK4	DIFFCLK_2p			E15
B6	VREFB6N0	CONF_DONE		CONF_DONE		H14
B6	VREFB6N0	MSEL0		MSEL0		H13
B6	VREFB6N0	MSEL1		MSEL1		H12
B6	VREFB6N0	MSEL2		MSEL2		G12
B6	VREFB6N0	IO		INIT_DONE	DIFFIO_R4n	G16
B6	VREFB6N0	IO		CRC_ERROR	DIFFIO_R4p	G15
B6	VREFB6N0	IO				F13
B6	VREFB6N0	IO		nCEO	DIFFIO_R3n	F16
B6	VREFB6N0	IO		CLKUSR	DIFFIO_R3p	F15
B6	VREFB6N0	IO	DPCLK5			B16
B6	VREFB6N0	IO	VREFB6N0			F14
B6	VREFB6N0	IO			DIFFIO_R2n	D16
B6	VREFB6N0	IO			DIFFIO_R2p	D15
B6	VREFB6N0	IO				G11
B6	VREFB6N0	IO			DIFFIO_R1n	C16
B6	VREFB6N0	IO			DIFFIO_R1p	C15
B7	VREFB7N0	IO			DIFFIO_T21n	C14
B7	VREFB7N0	IO			DIFFIO_T21p	D14
B7	VREFB7N0	IO			DIFFIO_T20n	D11

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U256
B7	VREFB7N0	IO	DPCLK6		DIFFIO_T20p	D12
B7	VREFB7N0	IO			DIFFIO_T19n	A13
B7	VREFB7N0	IO			DIFFIO_T19p	B13
B7	VREFB7N0	IO	PLL2_CLKOUTn			A14
B7	VREFB7N0	IO	PLL2_CLKOUTp			B14
B7	VREFB7N0	IO	RUP4			E11
B7	VREFB7N0	IO	RDN4			E10
B7	VREFB7N0	IO			DIFFIO_T18n	A12
B7	VREFB7N0	IO			DIFFIO_T18p	B12
B7	VREFB7N0	IO			DIFFIO_T17n	A11
B7	VREFB7N0	IO			DIFFIO_T17p	B11
B7	VREFB7N0	IO	VREFB7N0			C11
B7	VREFB7N0	IO			DIFFIO_T16n	F10
B7	VREFB7N0	IO			DIFFIO_T16p	F9
B7	VREFB7N0	IO			DIFFIO_T15n	F11
B7	VREFB7N0	IO			DIFFIO_T15p	A15
B7	VREFB7N0	IO			DIFFIO_T14n	A10
B7	VREFB7N0	IO			DIFFIO_T14p	B10
B7	VREFB7N0	IO			DIFFIO_T13n	C9
B7	VREFB7N0	IO			DIFFIO_T13p	D9
B7	VREFB7N0	IO				E9
B7	VREFB7N0	IO			DIFFIO_T12n	A9
B7	VREFB7N0	IO			DIFFIO_T12p	B9
B8	VREFB8N0	IO			DIFFIO_T11n	A8
B8	VREFB8N0	IO			DIFFIO_T11p	B8
B8	VREFB8N0	IO				C8
B8	VREFB8N0	IO				D8
B8	VREFB8N0	IO		DATA2	DIFFIO_T10n	E8
B8	VREFB8N0	IO		DATA3	DIFFIO_T10p	F8
B8	VREFB8N0	IO			DIFFIO_T9n	A7
B8	VREFB8N0	IO		DATA4	DIFFIO_T9p	B7
B8	VREFB8N0	IO			DIFFIO_T8n	F6
B8	VREFB8N0	IO			DIFFIO_T8p	F7
B8	VREFB8N0	IO	VREFB8N0			C6
B8	VREFB8N0	IO			DIFFIO_T7n	A6

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U256
B8	VREFB8N0	IO			DIFFIO_T7p	B6
B8	VREFB8N0	IO		DATA5		E7
B8	VREFB8N0	IO		DATA6		E6
B8	VREFB8N0	IO		DATA7	DIFFIO_T6n	A5
B8	VREFB8N0	IO			DIFFIO_T5n	A2
B8	VREFB8N0	IO			DIFFIO_T5p	B5
B8	VREFB8N0	IO			DIFFIO_T4n	A4
B8	VREFB8N0	IO			DIFFIO_T4p	B4
B8	VREFB8N0	IO			DIFFIO_T3p	D6
B8	VREFB8N0	IO			DIFFIO_T2n	A3
B8	VREFB8N0	IO	DPCLK7		DIFFIO_T2p	B3
B8	VREFB8N0	IO			DIFFIO_T1n	C3
B8	VREFB8N0	IO			DIFFIO_T1p	D3
		GND				H7
		GND				H8
		GND				H9
		GND				H10
		GND				J7
		GND				J8
		GND				J9
		GND				J10
		GND				B2
		GND				B15
		GND				C5
		GND				C12
		GND				D7
		GND				D10
		GND				E4
		GND				E13
		GND				G4
		GND				G13
		GND				K4
		GND				K13
		GND				M4
		GND				M13

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U256
		GND				N7
		GND				N10
		GND				P5
		GND				P12
		GND				R2
		GND				R15
		GND				H16
		GND				H15
		GND				D5
		GND				F1
		GND				F2
		GND				G5
		GNDA1				M5
		GNDA2				E12
		VCCD_PLL1				N4
		VCCD_PLL2				D13
		VCCIO1				E3
		VCCIO1				G3
		VCCIO2				K3
		VCCIO2				M3
		VCCIO3				P4
		VCCIO3				P7
		VCCIO3				T1
		VCCIO4				P10
		VCCIO4				P13
		VCCIO4				T16
		VCCIO5				K14
		VCCIO5				M14
		VCCIO6				E14
		VCCIO6				G14
		VCCIO7				A16
		VCCIO7				C10
		VCCIO7				C13
		VCCIO8				A1
		VCCIO8				C4

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U256
		VCCIO8				C7
		VCCA1				L5
		VCCA2				F12
		VCCINT				G6
		VCCINT				G7
		VCCINT				G8
		VCCINT				G9
		VCCINT				G10
		VCCINT				H6
		VCCINT				H11
		VCCINT				K7

Notes:
(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
(2) For more information about pin definition and pin connection guidelines, refer to the Intel Cyclone 10 LP Device Family Pin Connection Guidelines.

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Date	Version	Changes
February 2017	2017.02.13	Initial release.
May 2017	2017.05.19	Updated description for the Configuration pins.
March 2019	2019.03.29	Added DPCLK and CDPCLK support in optional pin function column.

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