



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	FB96 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					A123									
		GND					A126									
		GND					A15									
		GND					A16									
		GND					B1									
		GND					B2									
		GND					B23									
		GND					B26									
		GND					B29									
		GND					B5									
		GND					B8									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E5									
		GND					E8									
		GND					G12									
		GND					G14									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H5									
		GND					H8									
		GND					K11									
		GND					K14									
		GND					L17									
		GND					L2									
		GND					L20									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L5									
		GND					L8									
		GND					N10									
		GND					N14									
		GND					P11									
		GND					P17									
		GND					P16									
		GND					P2									
		GND					P20									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P5									
		GND					P8									
		GND					R18									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T20									
		GND					U11									
		GND					U15									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U7									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V18									
		GND					V20									
		GND					V14									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					X10									
		GND					Y12									
		GND					Y18									
		GND					Y20									

Notes:
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).
 (2) GAB, REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
 (3) Pins with * contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.
 (4) Pins with ~ are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).
 (5) RESET pin is only applicable for DDR3 device.



Pin Information for the Arria® V SASXMB5 Device
Version 1.3
Note (1)

Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X3	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS(3,6)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNV					A89									
		REF_TL					B8									
		REFCLKMn					U32									
		REFCLKMn					U31									
		GXB_TX_L17n					C30									
		GXB_TX_L17p					G37									
		GXB_RX_L17n:GXB_REFCLK_L17p					D39									
		GXB_RX_L17n:GXB_REFCLK_L17n					D38									
		GXB_TX_L16n					E36									
		GXB_TX_L16p					E37									
		GXB_RX_L16n:GXB_REFCLK_L16p					F39									
		GXB_RX_L16n:GXB_REFCLK_L16n					F38									
		GXB_TX_L15n					G36									
		GXB_TX_L15p					G37									
		GXB_RX_L15n:GXB_REFCLK_L15p					H39									
		GXB_RX_L15n:GXB_REFCLK_L15n					H38									
		GXB_TX_L14n					J36									
		GXB_TX_L14p					J37									
		GXB_RX_L14n:GXB_REFCLK_L14p					K39									
		GXB_RX_L14n:GXB_REFCLK_L14n					K38									
		GXB_TX_L13n					L36									
		GXB_TX_L13p					L37									
		GXB_RX_L13n:GXB_REFCLK_L13p					M39									
		GXB_RX_L13n:GXB_REFCLK_L13n					M38									
		GXB_TX_L12n					N36									
		GXB_TX_L12p					N37									
		GXB_RX_L12n:GXB_REFCLK_L12p					P39									
		GXB_RX_L12n:GXB_REFCLK_L12n					P38									
		REFCLKMn					W32									
		REFCLKMn					W31									
		REFCLKMn					A32									
		REFCLKMn					A31									
		GXB_TX_L11n					R36									
		GXB_TX_L11p					R37									
		GXB_RX_L11n:GXB_REFCLK_L11p					T39									
		GXB_RX_L11n:GXB_REFCLK_L11n					T38									
		GXB_TX_L10n					U36									
		GXB_TX_L10p					U37									
		GXB_RX_L10n:GXB_REFCLK_L10p					V39									
		GXB_RX_L10n:GXB_REFCLK_L10n					V38									
		GXB_TX_L9n					W36									
		GXB_TX_L9p					W37									
		GXB_RX_L9n:GXB_REFCLK_L9p					Y39									
		GXB_RX_L9n:GXB_REFCLK_L9n					Y38									
		GXB_TX_L8n					AA36									
		GXB_TX_L8p					AA37									
		GXB_RX_L8n:GXB_REFCLK_L8p					AB39									
		GXB_RX_L8n:GXB_REFCLK_L8n					AB38									
		GXB_TX_L7n					AC36									
		GXB_TX_L7p					AC37									
		GXB_RX_L7n:GXB_REFCLK_L7p					AD39									
		GXB_RX_L7n:GXB_REFCLK_L7n					AD38									
		GXB_TX_L6n					AE36									
		GXB_TX_L6p					AE37									
		GXB_RX_L6n:GXB_REFCLK_L6p					AF39									
		GXB_RX_L6n:GXB_REFCLK_L6n					AF38									
		REFCLKMn					AG32									
		REFCLKMn					AG31									
		REFCLKMn					AE32									
		REFCLKMn					AE31									
		GXB_TX_L5n					AG36									
		GXB_TX_L5p					AG37									
		GXB_RX_L5n:GXB_REFCLK_L5p					AH39									
		GXB_RX_L5n:GXB_REFCLK_L5n					AH38									
		GXB_TX_L4n					AI36									
		GXB_TX_L4p					AI37									
		GXB_RX_L4n:GXB_REFCLK_L4p					AK39									
		GXB_RX_L4n:GXB_REFCLK_L4n					AK38									
		GXB_TX_L3n					AL36									
		GXB_TX_L3p					AL37									
		GXB_RX_L3n:GXB_REFCLK_L3p					AM39									
		GXB_RX_L3n:GXB_REFCLK_L3n					AM38									
		GXB_TX_L2n					AM36									
		GXB_TX_L2p					AM37									
		GXB_RX_L2n:GXB_REFCLK_L2p					AP39									
		GXB_RX_L2n:GXB_REFCLK_L2n					AP38									
		GXB_TX_L1n					AP36									
		GXB_TX_L1p					AP37									
		GXB_RX_L1n:GXB_REFCLK_L1p					AT39									
		GXB_RX_L1n:GXB_REFCLK_L1n					AT38									
		GXB_TX_L0n					AU36									
		GXB_TX_L0p					AU37									
		GXB_RX_L0n:GXB_REFCLK_L0p					AV39									
		GXB_RX_L0n:GXB_REFCLK_L0n					AV38									
		REFCLKMn					AG32									
		REFCLKMn					AG31									
3A		DNV					AK41									
3A		TDO			TDO		AT34									
3A		TMS			TMS		AM35									
3A		TCX			TCX		AV34									
3A		TDI			TDI		AT33									
3A		DCLK			DCLK		AV33									
3A		AS0			AS0		AM34									
3A		AS_DATA3			DATA3		AU34									
3A		AS_DATA2			DATA2		AV33									
3A		AS_DATA1			DATA1		AV33									
3A		AS_DATA0AS0			DATA0		AV33									
3A	VREFBAND	IO	R20_0				DIFF0_TX_81n	DIFFOUT_81n	AM33							
3A	VREFBAND	IO					DIFF0_TX_81p	DIFFOUT_81p	AP33	DO1B						
3A	VREFBAND	IO	CLK0n				DIFF0_RX_80n	DIFFOUT_80n	AM34	DO1B						
3A	VREFBAND	IO	CLK0p				DIFF0_RX_80p	DIFFOUT_80p	AP34	DO1B						
3A	VREFBAND	IO					DIFF0_TX_80n	DIFFOUT_80n	AM32							
3A	VREFBAND	IO					DIFF0_TX_80p	DIFFOUT_80p	AP32	DO1B						
3A	VREFBAND	IO	CLK1n				DIFF0_RX_84n	DIFFOUT_84n	AM34	DO2B/DO20B						
3A	VREFBAND	IO	CLK1p				DIFF0_RX_84p	DIFFOUT_84p	AP34	DO2B/DO20B/DO21B/DO21n						
3A	VREFBAND	IO					DIFF0_TX_85n	DIFFOUT_85n	AM34							
3A	VREFBAND	IO	FPLL_B0_CLKOUT1:FPLL_B0_CLKOUTn				DIFF0_TX_86n	DIFFOUT_86n	AM34	DO1B						
3A	VREFBAND	IO	FPLL_B0_CLKOUT2:FPLL_B0_CLKOUTp:FPLL_B0_FBD				DIFF0_RX_86n	DIFFOUT_86n	AP34	DO1B						
3A	VREFBAND	IO	FPLL_B0_CLKOUT3:FPLL_B0_FBD				DIFF0_RX_86p	DIFFOUT_86p	AP33	DO1B						
3A	VREFBAND	IO	FPLL_B1_CLKOUT7:FPLL_B1_FBD:FPLL_B1_FBI				DIFF0_RX_86p	DIFFOUT_86p	AK33	DO1B						
3A	VREFBAND	IO	VREFBAND						AV31							



Bank Number	REF	PinName/Function (1), (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X3	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (6)	HMC pin assignment for FPDQS (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
1A	VREFBAND0	I0			DIFFIO_TX_B16n	DIFFOUT_B16n	AU31	DQ3B	DQ3B		A_3A_11					
1A	VREFBAND0	I0			DIFFIO_TX_B16p	DIFFOUT_B16p	AV31	DQ3B	DQ3B		A_3A_12					
1A	VREFBAND0	Q0			DIFFIO_RX_B17p	DIFFOUT_B17p	AV31	DD3B	DD1B		A_3A_9	CA_3A_9				
1A	VREFBAND0	I0			DIFFIO_TX_B18n	DIFFOUT_B18n	AA3B				A_3A_7	CA_3A_7				
1A	VREFBAND0	I0			DIFFIO_TX_B18p	DIFFOUT_B18p	AL3B	DQ3B	DQ1B		A_3A_6	CA_3A_6				
1A	VREFBAND0	I0			DIFFIO_RX_B18n	DIFFOUT_B18n	AP3B	DQ5B/QK3B	DQ5B/QK1B		A_3A_5	CA_3A_5				
1A	VREFBAND0	I0			DIFFIO_RX_B17p	DIFFOUT_B17p	AT3B	DQ5B/CQ3B/CQ3B/CQ3B	DQ5B/CQ3B/CQ3B/CQ3B		A_3A_4	CA_3A_4				
1A	VREFBAND0	I0			DIFFIO_TX_B20n	DIFFOUT_B20n	AU30				A_3A_3	CA_3A_3				
1A	VREFBAND0	I0			DIFFIO_TX_B20p	DIFFOUT_B20p	AV30	DQ3B	DQ1B		A_3A_2	CA_3A_2				
1A	VREFBAND0	I0			DIFFIO_RX_B21n	DIFFOUT_B21n	AT19	DQ3B	DQ1B		A_3A_1	CA_3A_1				
1A	VREFBAND0	I0			DIFFIO_RX_B21p	DIFFOUT_B21p	AU19	DQ3B	DQ1B		A_3A_0	CA_3A_0				
1A	VREFBAND0	I0			DIFFIO_TX_B22n	DIFFOUT_B22n	AA30				C0A_3A_1	C0A_3A_1				
1A	VREFBAND0	I0			DIFFIO_TX_B22p	DIFFOUT_B22p	AV30	DQ3B	DQ1B		C0A_3A_0	C0A_3A_0				
1A	VREFBAND0	Q0			DIFFIO_RX_B23n	DIFFOUT_B23n	AA29	DQ3B	DQ1B		CPA_3A	CPA_3A				
1A	VREFBAND0	I0			DIFFIO_RX_B23p	DIFFOUT_B23p	AV29	DQ3B	DQ1B		CK_3A	CK_3A				
1B	VREFBAND0	I0			DIFFIO_TX_B24n	DIFFOUT_B24n	AA28				RESETS_3A					
1B	VREFBAND0	I0			DIFFIO_TX_B24p	DIFFOUT_B24p	AV28	DQ4B	DQ2B		DQ1_3B_8	DQ1_3B_8				
1B	VREFBAND0	I0			DIFFIO_RX_B25n	DIFFOUT_B25n	AA28	DQ4B	DQ2B		DQ1_3B_7	DQ1_3B_7				
1B	VREFBAND0	I0			DIFFIO_RX_B25p	DIFFOUT_B25p	AV28	DQ4B	DQ2B		DQ1_3B_6	DQ1_3B_6				
1B	VREFBAND0	I0			DIFFIO_TX_B26n	DIFFOUT_B26n	AA29				DQ2B					
1B	VREFBAND0	I0			DIFFIO_RX_B26p	DIFFOUT_B26p	AV29	DQ4B	DQ2B		DQ1_3B	DQ1_3B				
1B	VREFBAND0	I0			DIFFIO_RX_B27n	DIFFOUT_B27n	AA28	DQ5B/QK4B	DQ5B/QK2B		DQ1_3B	DQ1_3B				
1B	VREFBAND0	I0			DIFFIO_RX_B27p	DIFFOUT_B27p	AV28	DQ5B/CQ4B/CQ4B/CQ4B	DQ5B/QK2B		DQ0B1_3B	DQ0B1_3B				
1B	VREFBAND0	I0			DIFFIO_TX_B28n	DIFFOUT_B28n	AA29				DQ2B					
1B	VREFBAND0	I0			DIFFIO_TX_B28p	DIFFOUT_B28p	AV29	DQ4B	DQ2B		DQ1_3B_5	DQ1_3B_5				
1B	VREFBAND0	I0			DIFFIO_RX_B29n	DIFFOUT_B29n	AA27	DQ4B	DQ2B		DQ1_3B_4	DQ1_3B_4				
1B	VREFBAND0	I0			DIFFIO_RX_B29p	DIFFOUT_B29p	AV27	DQ4B	DQ2B		DQ1_3B_3	DQ1_3B_3				
1B	VREFBAND0	I0	VREFBAND0				AL28									
1B	VREFBAND0	I0			DIFFIO_RX_B30n	DIFFOUT_B30n	AA28	DQ4B	DQ2B		DQ1_3B_2	DQ1_3B_2				
1B	VREFBAND0	I0			DIFFIO_RX_B30p	DIFFOUT_B30p	AV27	DQ4B	DQ2B		DQ1_3B_1	DQ1_3B_1				
1B	VREFBAND0	I0			DIFFIO_TX_B31n	DIFFOUT_B31n	AA29				DQ1_3B_0	DQ1_3B_0				
1B	VREFBAND0	I0			DIFFIO_TX_B31p	DIFFOUT_B31p	AA28	DQ5B	DQ3B		DQ2_3B_8	DQ2_3B_8				
1B	VREFBAND0	I0			DIFFIO_RX_B32n	DIFFOUT_B32n	AA28	DQ5B	DQ3B		DQ2_3B_7	DQ2_3B_7				
1B	VREFBAND0	I0			DIFFIO_RX_B32p	DIFFOUT_B32p	AV28	DQ5B	DQ3B		DQ2_3B_6	DQ2_3B_6				
1B	VREFBAND0	I0			DIFFIO_TX_B33n	DIFFOUT_B33n	AA27									
1B	VREFBAND0	I0			DIFFIO_TX_B33p	DIFFOUT_B33p	AV27	DQ5B	DQ3B		DMG_3B	DMG_3B				
1B	VREFBAND0	I0			DIFFIO_RX_B34n	DIFFOUT_B34n	AV29	DQ5B/CQ5B	DQ5B/CQ3B		DQ5B_3B	DQ5B_3B				
1B	VREFBAND0	I0			DIFFIO_RX_B34p	DIFFOUT_B34p	AV28	DQ5B/CQ5B/CQ5B/CQ5B	DQ5B/CQ3B/CQ3B/CQ3B		DQ5B_3B	DQ5B_3B				
1B	VREFBAND0	I0			DIFFIO_TX_B35n	DIFFOUT_B35n	AA27									
1B	VREFBAND0	I0			DIFFIO_TX_B35p	DIFFOUT_B35p	AA27	DQ6B	DQ4B		DQ2_3B_5	DQ2_3B_5				
1B	VREFBAND0	I0			DIFFIO_RX_B36n	DIFFOUT_B36n	AA27	DQ6B	DQ4B		DQ2_3B_4	DQ2_3B_4				
1B	VREFBAND0	I0			DIFFIO_RX_B36p	DIFFOUT_B36p	AV27	DQ6B	DQ4B		DQ2_3B_3	DQ2_3B_3				
1B	VREFBAND0	I0			DIFFIO_TX_B37n	DIFFOUT_B37n	AA27									
1B	VREFBAND0	I0			DIFFIO_TX_B37p	DIFFOUT_B37p	AA27	DQ6B	DQ4B		DQ2_3B_2	DQ2_3B_2				
1B	VREFBAND0	I0			DIFFIO_RX_B38n	DIFFOUT_B38n	AA27	DQ6B	DQ4B		DQ2_3B_1	DQ2_3B_1				
1B	VREFBAND0	I0			DIFFIO_RX_B38p	DIFFOUT_B38p	AV27	DQ6B	DQ4B		DQ2_3B_0	DQ2_3B_0				
1C	VREFBAND0	I0			DIFFIO_TX_B39n	DIFFOUT_B39n	AA27									
1C	VREFBAND0	I0			DIFFIO_TX_B39p	DIFFOUT_B39p	AA27	DQ6B	DQ4B		DQ3_3C_8	DQ3_3C_8				
1C	VREFBAND0	I0			DIFFIO_RX_B40n	DIFFOUT_B40n	AA25	DQ6B	DQ4B		DQ3_3C_7	DQ3_3C_7				
1C	VREFBAND0	I0			DIFFIO_RX_B40p	DIFFOUT_B40p	AA25	DQ6B	DQ4B		DQ3_3C_6	DQ3_3C_6				
1C	VREFBAND0	I0			DIFFIO_TX_B41n	DIFFOUT_B41n	AA27									
1C	VREFBAND0	I0			DIFFIO_TX_B41p	DIFFOUT_B41p	AA27	DQ6B	DQ4B		DMG_3C	DMG_3C				
1C	VREFBAND0	I0			DIFFIO_RX_B42n	DIFFOUT_B42n	AA25	DQ5B/CQ6B	DQ5B/CQ4B		DQ5B_3C	DQ5B_3C				
1C	VREFBAND0	I0			DIFFIO_RX_B42p	DIFFOUT_B42p	AA25	DQ5B/CQ6B/CQ6B/CQ6B	DQ5B		DQ5B_3C	DQ5B_3C				
1C	VREFBAND0	I0			DIFFIO_TX_B43n	DIFFOUT_B43n	AA26				DQ3_3C_5	DQ3_3C_5				
1C	VREFBAND0	I0			DIFFIO_TX_B43p	DIFFOUT_B43p	AA25	DQ6B	DQ4B		DQ3_3C_4	DQ3_3C_4				
1C	VREFBAND0	I0			DIFFIO_RX_B44n	DIFFOUT_B44n	AA26	DQ6B	DQ4B		DQ3_3C_3	DQ3_3C_3				
1C	VREFBAND0	I0			DIFFIO_RX_B44p	DIFFOUT_B44p	AA26	DQ6B	DQ4B		DQ3_3C_2	DQ3_3C_2				
1C	VREFBAND0	I0			DIFFIO_RX_B45n	DIFFOUT_B45n	AA26	DQ6B	DQ4B		DQ3_3C_1	DQ3_3C_1				
1C	VREFBAND0	I0			DIFFIO_RX_B45p	DIFFOUT_B45p	AA26	DQ6B	DQ4B		DQ3_3C_0	DQ3_3C_0				
1C	VREFBAND0	I0			DIFFIO_TX_B46n	DIFFOUT_B46n	AA27									
1C	VREFBAND0	I0			DIFFIO_RX_B46p	DIFFOUT_B46p	AA26	DQ6B	DQ4B		DQ4_3C_7	DQ4_3C_7				
1C	VREFBAND0	I0			DIFFIO_TX_B47n	DIFFOUT_B47n	AA26				DQ4_3C_6	DQ4_3C_6				
1C	VREFBAND0	I0			DIFFIO_RX_B47p	DIFFOUT_B47p	AA25	DQ7B	DQ5B		DQ4_3C_5	DQ4_3C_5				
1C	VREFBAND0	I0			DIFFIO_TX_B48n	DIFFOUT_B48n	AA25									
1C	VREFBAND0	I0			DIFFIO_TX_B48p	DIFFOUT_B48p	AA25	DQ7B	DQ5B		DMG_3C	DMG_3C				
1C	VREFBAND0	I0			DIFFIO_RX_B49n	DIFFOUT_B49n	AA25	DQ7B	DQ5B		DQ5B_3C	DQ5B_3C				
1C	VREFBAND0	I0			DIFFIO_RX_B49p	DIFFOUT_B49p	AA25	DQ7B	DQ5B		DQ5B_3C	DQ5B_3C				
1C	VREFBAND0	I0			DIFFIO_TX_B50n	DIFFOUT_B50n	AT26	DQ6B/QK3B	DQ6B/QK1B		DQ4_3C	DQ4_3C				
1C	VREFBAND0	I0			DIFFIO_RX_B50p	DIFFOUT_B50p	AV26	DQ6B/CQ7B/CQ7B/CQ7B	DQ6B/CQ3B/CQ3B/CQ3B		DQ4_3C	DQ4_3C				
1C	VREFBAND0	I0			DIFFIO_TX_B51n	DIFFOUT_B51n	AA25				DQ4_3C	DQ4_3C				
1C	VREFBAND0	I0			DIFFIO_TX_B51p	DIFFOUT_B51p	AA25				DQ4_3C	DQ4_3C				
1C	VREFBAND0	I0			DIFFIO_RX_B52n	DIFFOUT_B52n	AT26	DQ7B	DQ5B		DQ4_3C_5	DQ4_3C_5				
1C	VREFBAND0	I0			DIFFIO_RX_B52p	DIFFOUT_B52p	AV26	DQ7B	DQ5B		DQ4_3C_4	DQ4_3C_4				
1C	VREFBAND0	I0			DIFFIO_RX_B53n	DIFFOUT_B53n	AA26				DQ4_3C_3	DQ4_3C_3				
1C	VREFBAND0	I0			DIFFIO_RX_B53p	DIFFOUT_B53p	AV26	DQ7B	DQ5B		DQ4_3C_2	DQ4_3C_2				
1C	VREFBAND0	I0			DIFFIO_TX_B54n	DIFFOUT_B54n	AA24				DQ4_3C_1	DQ4_3C_1				
1C	VREFBAND0	I0			DIFFIO_TX_B54p	DIFFOUT_B54p	AA24	DQ8B	DQ6B		DQ4_3C_0	DQ4_3C_0				
1C	VREFBAND0	I0			DIFFIO_RX_B55n	DIFFOUT_B55n	AA24	DQ8B	DQ6B		DQ5_3C_8	DQ5_3C_8				
1C	VREFBAND0	I0			DIFFIO_RX_B55p	DIFFOUT_B55p	AA24	DQ8B	DQ6B		DQ5_3C_7	DQ5_3C_7				
1C	VREFBAND0	I0			DIFFIO_RX_B56n	DIFFOUT_B56n	AA24	DQ8B	DQ6B		DQ5_3C_6	DQ5_3C_6				
1C	VREFBAND0	I0			DIFFIO_TX_B56p	DIFFOUT_B56p	AA24	DQ8B	DQ6B		DMG_3C	DMG_3C				
1C	VREFBAND0	I0			DIFFIO_RX_B57n	DIFFOUT_B57n	AA24	DQ8B	DQ6B		DQ5B_3C	DQ5B_3C				
1C	VREFBAND0	I0			DIFFIO_RX_B57p	DIFFOUT_B57p	AA24	DQ8B/CQ8B/CQ8B/CQ8B	DQ4B		DQ5B_3C	DQ5B_3C				
1C	VREFBAND0	I0			DIFFIO_TX_B58n	DIFFOUT_B58n	AA24									
1C	VREFBAND0	I0			DIFFIO_TX_B58p	DIFFOUT_B58p	AA24	DQ8B	DQ6B		DQ5_3C_5	DQ5_3C_5				
1C	VREFBAND0	I0			DIFFIO_RX_B59n	DIFFOUT_B59n	AA23	DQ8B	DQ6B		DQ5_3C_4	DQ5_3C_4				
1C	VREFBAND0	I0			DIFFIO_RX_B59p	DIFFOUT_B59p	AA23	DQ8B	DQ6B		DQ5_3C_3	DQ5_3C_3				
1C	VREFBAND0	I0			DIFFIO_TX_B60n	DIFFOUT_B60n	AA24									
1C	VREFBAND0	I0			DIFFIO_RX_B60p	DIFFOUT_B60p	AA24	DQ8B	DQ6B		DQ5_3C_2	DQ5_3C_2				
1C	VREFBAND0	I0			DIFFIO_RX_B61n	DIFFOUT_B61n	AT23	DQ8B	DQ6B		DQ5_3C_1	DQ5_3C_1				
1C	VREFBAND0	I0			DIFFIO_RX_B61p	DIFFOUT_B61p	AT23	DQ8B	DQ6B		DQ5_3C_0	DQ5_3C_0				
1D	VREFBAND0	I0			DIFFIO_TX_B62n	DIFFOUT_B62n	AA23									
1D	VREFBAND0	I0			DIFFIO_TX_B62p	DIFFOUT_B62p	AA23	DQ8B	DQ6B							
1D	VREFBAND0	I0			DIFFIO_RX_B63n	DIFFOUT_B63n	AA22	DQ8B	DQ6B							
1D	VREFBAND0	I0			DIFFIO_RX_B63p	DIFFOUT_B63p	AA23	DQ8B	DQ6B							
1D	VREFBAND0	I0			DIFFIO_TX_B64n	DIFFOUT_B64n	AA23									
1D	VREFBAND0	I0			DIFFIO_TX_B64p	DIFFOUT_B64p	AA23	DQ9B	DQ7B							
1D	VREFBAND0	I0			DIFFIO_RX_B65n	DIFFOUT_B65n	AA22	DQ8								



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DS0 for X8/X9	DS0 for X16/X18	DS0 for X32/X36	HMC pin assignment for DS03 (6)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
EB	UNREFBAND_HPS	HPS_D0R					L1				HPS_DD_35	HPS_DD_35				
EB	UNREFBAND_HPS	HPS_D0R					F1				HPS_DD_31	HPS_DD_31				
EB	UNREFBAND_HPS	HPS_D0R					K3				HPS_DD_21	HPS_DD_21				
EB	UNREFBAND_HPS	HPS_D0R					G1				HPS_DD_33	HPS_DD_33				
EB	UNREFBAND_HPS	HPS_GPI2					K3				HPS_DD_34	HPS_DD_34				
EB	UNREFBAND_HPS	HPS_GPI1					J2				HPS_DD_32	HPS_DD_32				
EB	UNREFBAND_HPS	HPS_D0R					D1				HPS_DM_3	HPS_DM_3				
EB	UNREFBAND_HPS	HPS_GPI0					K2									
EB	UNREFBAND_HPS	HPS_D0R					E1				HPS_DD_31	HPS_DD_31				
EB	UNREFBAND_HPS	HPS_D0R					F2				HPS_DD_29	HPS_DD_29				
EB	UNREFBAND_HPS	HPS_D0R					M3				HPS_DD_30	HPS_DD_30				
EB	UNREFBAND_HPS	HPS_D0R					G2				HPS_DD_28	HPS_DD_28				
EB	UNREFBAND_HPS	UNREFBAND_HPS					M2									
EB	UNREFBAND_HPS	HPS_D0R					G2				HPS_D03_3	HPS_D03_3				
EB	UNREFBAND_HPS	HPS_GPI9					B1				HPS_D03_3	HPS_D03_3				
EB	UNREFBAND_HPS	HPS_D0R					D0				HPS_D03_3	HPS_D03_3				
EB	UNREFBAND_HPS	HPS_D0R					C1				HPS_D03_3	HPS_D03_3				
EB	UNREFBAND_HPS	HPS_D0R					A3				HPS_DD_25	HPS_DD_25				
EB	UNREFBAND_HPS	HPS_D0R					F7				HPS_DD_26	HPS_DD_26				
EB	UNREFBAND_HPS	HPS_D0R					A2				HPS_DD_24	HPS_DD_24				
EB	UNREFBAND_HPS	HPS_GPI8					N5									
EB	UNREFBAND_HPS	HPS_D0R					K3									
EB	UNREFBAND_HPS	HPS_D0R					D3				HPS_DM_2	HPS_DM_2				
EB	UNREFBAND_HPS	HPS_GPI8					K4									
EB	UNREFBAND_HPS	HPS_D0R					C3				HPS_DD_23	HPS_DD_23				
EB	UNREFBAND_HPS	HPS_D0R					J4				HPS_DD_21	HPS_DD_21				
EB	UNREFBAND_HPS	HPS_D0R					M4				HPS_DD_22	HPS_DD_22				
EB	UNREFBAND_HPS	HPS_D0R					L5				HPS_DD_22	HPS_DD_22				
EB	UNREFBAND_HPS	HPS_GPI5					G4				HPS_DD_20	HPS_DD_20				
EB	UNREFBAND_HPS	HPS_D0R					E3				HPS_D03_2	HPS_D03_2				
EB	UNREFBAND_HPS	HPS_D0R					H4				HPS_RESET#	HPS_RESET#				
EB	UNREFBAND_HPS	HPS_D0R					H4				HPS_D03_2	HPS_D03_2				
EB	UNREFBAND_HPS	HPS_D0R					F3				HPS_DD_19	HPS_DD_19				
EB	UNREFBAND_HPS	HPS_D0R					K5				HPS_DD_17	HPS_DD_17				
EB	UNREFBAND_HPS	HPS_D0R					N7				HPS_DD_18	HPS_DD_18				
EB	UNREFBAND_HPS	HPS_D0R					J2				HPS_DD_16	HPS_DD_16				
EB	UNREFBAND_HPS	HPS_GPI4					M6									
EA	UNREFBAND_HPS	HPS_GPI3					C4				HPS_DM_1	HPS_DM_1				
EA	UNREFBAND_HPS	HPS_D0R					E4									
EA	UNREFBAND_HPS	HPS_GPI2					B4				HPS_DD_15	HPS_DD_15				
EA	UNREFBAND_HPS	HPS_D0R					F4				HPS_DD_13	HPS_DD_13				
EA	UNREFBAND_HPS	HPS_D0R					A5				HPS_DD_13	HPS_DD_13				
EA	UNREFBAND_HPS	HPS_D0R					R9				HPS_DD_14	HPS_DD_14				
EA	UNREFBAND_HPS	HPS_D0R					A4				HPS_DD_12	HPS_DD_12				
EA	UNREFBAND_HPS	HPS_D0R					R8				HPS_CK6_0	HPS_CK6_0				
EA	UNREFBAND_HPS	HPS_D0R					D5				HPS_D0S_1	HPS_D0S_1				
EA	UNREFBAND_HPS	HPS_D0R					F5				HPS_CK6_1	HPS_CK6_1				
EA	UNREFBAND_HPS	HPS_D0R					E8				HPS_D03_1	HPS_D03_1				
EA	UNREFBAND_HPS	HPS_D0R					G5				HPS_D03_1	HPS_D03_1				
EA	UNREFBAND_HPS	HPS_D0R					G6				HPS_DD_9	HPS_DD_9				
EA	UNREFBAND_HPS	HPS_D0R					N8				HPS_DD_10	HPS_DD_10				
EA	UNREFBAND_HPS	HPS_D0R					M9				HPS_DD_9	HPS_DD_9				
EA	UNREFBAND_HPS	HPS_GPI1					W4				HPS_DD_8	HPS_DD_8				
EA	UNREFBAND_HPS	HPS_GPI0					B6									
EA	UNREFBAND_HPS	HPS_D0R					C8				HPS_DM_0	HPS_DM_0				
EA	UNREFBAND_HPS	HPS_D0R					D8				HPS_DD_7	HPS_DD_7				
EA	UNREFBAND_HPS	HPS_D0R					A7				HPS_DD_5	HPS_DD_5				
EA	UNREFBAND_HPS	HPS_D0R					L6				HPS_DD_6	HPS_DD_6				
EA	UNREFBAND_HPS	HPS_D0R					A6				HPS_DD_4	HPS_DD_4				
EA	UNREFBAND_HPS	HPS_D0R					K6				HPS_ODT_1	HPS_ODT_1				
EA	UNREFBAND_HPS	HPS_D0R					F7				HPS_D0S_0	HPS_D0S_0				
EA	UNREFBAND_HPS	HPS_D0R					H7				HPS_ODT_0	HPS_ODT_0				
EA	UNREFBAND_HPS	HPS_D0R					E7				HPS_D03_0	HPS_D03_0				
EA	UNREFBAND_HPS	HPS_D0R					E5				HPS_DD_3	HPS_DD_3				
EA	UNREFBAND_HPS	HPS_D0R					C7				HPS_DD_1	HPS_DD_1				
EA	UNREFBAND_HPS	HPS_D0R					F10				HPS_DD_2	HPS_DD_2				
EA	UNREFBAND_HPS	HPS_D0R					D7				HPS_DD_0	HPS_DD_0				
EA	UNREFBAND_HPS	UNREFBAND_HPS					F10									
EA	UNREFBAND_HPS	HPS_D0R					N5				HPS_CA_0	HPS_CA_0				
EA	UNREFBAND_HPS	HPS_D0R					M9				HPS_A_1	HPS_A_1				
EA	UNREFBAND_HPS	HPS_D0R					AP				HPS_A_4	HPS_A_4				
EA	UNREFBAND_HPS	HPS_D0R					N10				HPS_A_2	HPS_A_2				
EA	UNREFBAND_HPS	HPS_D0R					B7				HPS_A_5	HPS_A_5				
EA	UNREFBAND_HPS	HPS_D0R					M10				HPS_A_3	HPS_A_3				
EA	UNREFBAND_HPS	HPS_D0R					A11				HPS_CK	HPS_CK				
EA	UNREFBAND_HPS	HPS_D0R					B9				HPS_A_6	HPS_A_6				
EA	UNREFBAND_HPS	HPS_D0R					C10				HPS_CK6	HPS_CK6				
EA	UNREFBAND_HPS	HPS_D0R					M9				HPS_CK6	HPS_CK6				
EA	UNREFBAND_HPS	HPS_D0R					L7				HPS_BA_1	HPS_BA_1				
EA	UNREFBAND_HPS	HPS_D0R					C9				HPS_BA_0	HPS_BA_0				
EA	UNREFBAND_HPS	HPS_D0R					D8				HPS_BA_2	HPS_BA_2				
EA	UNREFBAND_HPS	HPS_D0R					G9				HPS_CAS#	HPS_CAS#				
EA	UNREFBAND_HPS	HPS_D0R					G8				HPS_RAS#	HPS_RAS#				
EA	UNREFBAND_HPS	HPS_D0R					K9				HPS_CA_8	HPS_CA_8				
EA	UNREFBAND_HPS	HPS_D0R					D9				HPS_A_10	HPS_A_10				
EA	UNREFBAND_HPS	HPS_D0R					C10				HPS_A_9	HPS_A_9				
EA	UNREFBAND_HPS	HPS_D0R					J7				HPS_A_11	HPS_A_11				
EA	UNREFBAND_HPS	HPS_D0R					F9				HPS_CSB_0	HPS_CSB_0				
EA	UNREFBAND_HPS	HPS_D0R					J9				HPS_A_17	HPS_A_17				
EA	UNREFBAND_HPS	HPS_D0R					E9				HPS_CSB_1	HPS_CSB_1				
EA	UNREFBAND_HPS	HPS_D0R					H9				HPS_A_13	HPS_A_13				
EA	UNREFBAND_HPS	HPS_D0R					D11				HPS_A_14	HPS_A_14				
EA	UNREFBAND_HPS	HPS_D0R					J8				HPS_W#	HPS_W#				
EA	UNREFBAND_HPS	HPS_D0R					D10				HPS_A_15	HPS_A_15				
EA	UNREFBAND_HPS	HPS_D0R					B12									
EA	UNREFBAND_HPS	HPS_D0R					C11									
EA	UNREFBAND_HPS	HPS_D0R					A12									
EA	UNREFBAND_HPS	HPS_D0R					F10									
EA	UNREFBAND_HPS	HPS_D0R					K10									
EA	UNREFBAND_HPS	HPS_D0R					I11									
EA	UNREFBAND_HPS	HPS_D0R					F10									
EA	UNREFBAND_HPS	HPS_D0R					G10									
EA	UNREFBAND_HPS	HPS_D0R					F11									
EA	UNREFBAND_HPS	HPS_D0R					H10									
EA	UNREFBAND_HPS	HPS_D0R					M11									
EA	UNREFBAND_HPS	HPS_D0R					C12									
EA	UNREFBAND_HPS	HPS_D0R					N11									
EA	UNREFBAND_HPS	HPS_D0R					D12									
EA	UNREFBAND_HPS	HPS_D0R					F11				TRACE_CLK	TRACE_CLK				
EA	UNREFBAND_HPS	HPS_D0R					K12				TRACE_DD	TRACE_DD	SPIS0_CLK	UART0_RX		HPS_GPI048
EA	UNREFBAND_HPS	HPS_D0R					X11				TRACE_D1	TRACE_D1	SPIS0_MISO	UART0_TX		HPS_GPI049
EA	UNREFBAND_HPS	HPS_D0R					F12				TRACE_D2	TRACE_D2	SPIS0_MISO	DCI_SDA		HPS_GPI050
EA	UNREFBAND_HPS	HPS_D0R					H12				TRACE_D3	TRACE_D3	SPIS0_SSD	DCI_SCL		HPS_GPI050
EA	UNREFBAND_HPS	HPS_D0R					F12				TRACE_D4	TRACE_D4	SPIS1_CLK	TRACE_D4		HPS_GPI053
EA	UNREFBAND_HPS	HPS_D0R					G11				TRACE_D5	TRACE_D5	SPIS1_MISO	HPS_GPI054		
EA	UNREFBAND_HPS	HPS_D0R					F12				TRACE_D6	TRACE_D6	SPIS1_SSD	DCI_SDA		HPS_GPI056
EA	UNREFBAND_HPS	HPS_D0R					A13				TRACE_D7	TRACE_D7	SPIS1_MISO	DCI_SCL		HPS_GPI056
EA	UNREFBAND_HPS	HPS_D0R					F12				SPIM0_CLK	SPIM0_CLK	DCI_SDA	UART0_CTS		HPS_GPI057
EA	UNREFBAND_HPS	HPS_D0R					A14				SPIM0_MOSI	SPIM0_MOSI	DCI_SCL	UART0_RTS		HPS_GPI058
EA	UNREFBAND_HPS	HPS_D0R					N12				SPIM0_MISO	SPIM0_MISO	DCI_CTS	UART1_CTS		



Pin Information for the Arria® V SASXMB5 Device

Version 1.3

Note (1)

Table with columns: Bank Number, VREF, PinName/Function (Z), Optional Function(s), Configuration Function, Dedicated Tx/Rx Channel, Emulated LVDS Output Channel, F1517 (4), DQS for X8/X4, DQS for X16/X8, DQS for X32/X16, HMC pin assignment for DQS3 (2), HMC pin assignment for LPDDR2, HPS Pin Mux Select 3, HPS Pin Mux Select 2, HPS Pin Mux Select 1, HPS Pin Mux Select 0. Rows include various pins like SPB1_MOSI, SPB1_MISO, SPB1_SS0, etc.



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQES1 (6)	HMC pin assignment for FPODE2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BA	VREFBAND	IO			DIFFIO_TX_T112n	DIFFIO_TX_T112n	G32									
BA	VREFBAND	IO	CLK200p		DIFFIO_RX_T113p	DIFFIO_TX_T113p	G34	DD11T								
BA	VREFBAND	IO	CLK200p		DIFFIO_RX_T113p	DIFFIO_TX_T113p	G34	DD11T								
BA	VREFBAND	IO			DIFFIO_TX_T114p	DIFFIO_TX_T114p	E33	DD11T								
BA	VREFBAND	IO	R3D_6		DIFFIO_TX_T114n	DIFFIO_TX_T114n	F33									
BA		MSEL0		MSEL0			H36									
BA		MSEL1		MSEL1			A34									
BA		MSEL2		MSEL2			D35									
BA		MSEL3		MSEL3			A37									
BA		MSEL4		MSEL4			P34									
BA		CONF_DONE		CONF_DONE			K35									
BA		STATUS		STATUS			F36									
BA		NCI		NCI			M35									
BA		KCONFG		KCONFG			A36									
BA		GND					P35									
BA		VCC_NIPS					V16									
BA		GND					W16									
BA		GND					AA33									
BA		GND					AA35									
BA		GND					AA38									
BA		GND					AA39									
BA		GND					AB11									
BA		GND					AB32									
BA		GND					AB44									
BA		GND					AB36									
BA		GND					AB37									
BA		GND					AC33									
BA		GND					AC38									
BA		GND					AC39									
BA		GND					AD32									
BA		GND					AD36									
BA		GND					AD37									
BA		GND					AE33									
BA		GND					AE35									
BA		GND					AE38									
BA		GND					AE39									
BA		GND					AF31									
BA		GND					AF32									
BA		GND					AF34									
BA		GND					AF36									
BA		GND					AF37									
BA		GND					AG36									
BA		GND					AG39									
BA		GND					AH33									
BA		GND					AH33									
BA		GND					AH34									
BA		GND					AH35									
BA		GND					AH36									
BA		GND					AH37									
BA		GND					AI35									
BA		GND					AI38									
BA		GND					AI39									
BA		GND					AM36									
BA		GND					AM37									
BA		GND					AM35									
BA		GND					AN38									
BA		GND					AN39									
BA		GND					AP39									
BA		GND					AP35									
BA		GND					AP38									
BA		GND					AR39									
BA		GND					AT36									
BA		GND					AT37									
BA		GND					AU25									
BA		GND					AU38									
BA		GND					AU39									
BA		GND					AV35									
BA		GND					AV38									
BA		GND					AV37									
BA		GND					AV38									
BA		GND					AV39									
BA		GND					AV35									
BA		GND					AV38									
BA		GND					BA36									
BA		GND					B37									
BA		GND					C35									
BA		GND					C38									
BA		GND					C39									
BA		GND					D36									
BA		GND					D37									
BA		GND					E35									
BA		GND					E38									
BA		GND					E39									
BA		GND					F36									
BA		GND					F37									
BA		GND					G35									
BA		GND					G38									
BA		GND					G38									
BA		GND					H36									
BA		GND					H37									
BA		GND					J35									
BA		GND					J38									
BA		GND					J39									
BA		GND					K36									
BA		GND					K37									
BA		GND					L36									
BA		GND					L38									
BA		GND					L39									
BA		GND					M36									
BA		GND					M37									
BA		GND					N35									
BA		GND					N38									
BA		GND					N39									
BA		GND					P39									
BA		GND					PF37									
BA		GND					R34									
BA		GND					R38									
BA		GND					R39									
BA		GND					T32									
BA		GND					T38									
BA		GND					T37									
BA		GND					U33									
BA		GND					U36									
BA		GND					U38									
BA		GND					U39									
BA		GND					V32									
BA		GND					V34									
BA		GND					V36									
BA		GND					V37									
BA		GND					W33									
BA		GND					W38									
BA		GND					W39									
BA		GND					Y31									
BA		GND					Y32									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					B02									
		GND					B5									
		GND					E11									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E32									
		GND					E5									
		GND					E8									
		GND					F14									
		GND					H11									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					I14									
		GND					K20									
		GND					L11									
		GND					L17									
		GND					L2									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L32									
		GND					L5									
		GND					L8									
		GND					N14									
		GND					N17									
		GND					N20									
		GND					P11									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P22									
		GND					P25									
		GND					W21									
		GND					T12									
		GND					T15									
		GND					T16									
		GND					T18									
		GND					T20									
		GND					T9									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U23									
		GND					U26									
		GND					U27									
		GND					U30									
		GND					U7									
		GND					V14									
		GND					V9									
		GND					V18									
		GND					V21									
		GND					V24									
		GND					V26									
		GND					V28									
		GND					V30									
		GND					V8									
		GND					W17									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W23									
		GND					W25									
		GND					W29									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V15									
		GND					V18									
		GND					V20									
		GND					V22									
		GND					V24									
		GND					V26									
		GND					V28									

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).
(2) GND_AREFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) Pins with * contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.
(4) Pins with # are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices](#) chapter.
(5) RESET pin is only applicable for DDR3 device.



**Pin Information for the Arria® V 5ASXMB5 Device
Version 1.3**

Version Number	Date	Changes Made
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.