



Table with columns: Bank Number, REF, PinName/Function (2, 3), Optional Function(s), Configuration Function, Dedicated Tx/Rx Channel, Emulated LVDS Output Channel, F1152 (#), DQS for X8/X9, DQS for X16/X18, DQS for X32/X36, HMC pin assignment for DDR3 (0), HMC pin assignment for LPDDR2, HPS Pin Mux Select 3, HPS Pin Mux Select 2, HPS Pin Mux Select 1, HPS Pin Mux Select 0.



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AB27									
		GND					AB28									
		GND					AB30									
		GND					AB31									
		GND					AB32									
		GND					AC30									
		GND					AC33									
		GND					AC34									
		GND					AD31									
		GND					AD32									
		GND					AE30									
		GND					AE33									
		GND					AE34									
		GND					AF31									
		GND					AF32									
		GND					AG30									
		GND					AG33									
		GND					AG34									
		GND					AH31									
		GND					AH32									
		GND					AJ30									
		GND					AJ33									
		GND					AJ34									
		GND					AK31									
		GND					AK32									
		GND					AL33									
		GND					AL34									
		GND					E34									
		GND					F31									
		GND					F32									
		GND					G30									
		GND					G33									
		GND					G34									
		GND					H31									
		GND					H32									
		GND					J30									
		GND					J33									
		GND					J34									
		GND					K31									
		GND					K32									
		GND					L30									
		GND					L33									
		GND					L34									
		GND					M30									
		GND					M31									
		GND					M32									
		GND					N28									
		GND					N29									
		GND					N33									
		GND					N34									
		GND					P27									
		GND					P31									
		GND					P32									
		GND					R28									
		GND					R30									
		GND					R33									
		GND					R34									
		GND					T27									
		GND					T29									
		GND					T31									
		GND					T32									
		GND					U28									
		GND					U33									
		GND					U34									
		GND					V27									
		GND					V31									
		GND					V32									
		GND					W28									
		GND					W30									
		GND					W33									
		GND					W34									
		GND					Y27									
		GND					Y29									
		GND					Y31									
		GND					Y32									
		GND					AA1									
		GND					AA2									
		GND					AB3									
		GND					AB4									
		GND					AC1									
		GND					AC2									
		GND					AC5									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE5									
		GND					AF3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG5									
		GND					AH3									
		GND					AH4									
		GND					AJ1									
		GND					AJ2									
		GND					AJ5									
		GND					AK3									
		GND					AK4									
		GND					AL1									
		GND					AL2									
		GND					AL3									
		GND					AN1									
		GND					V3									
		GND					V4									
		GND					V7									
		GND					W1									
		GND					W2									
		GND					W6									
		GND					Y3									
		GND					Y4									
		GND					Y8									
		GND					Y8									
		VCCP					R18									
		VCCP					T21									
		VCCP					U6									
		VCCP					W10									
		VCCP					Y10									
		VCCP					Y12									
		VCCP					Y22									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCP					Y24									
		VCCP					Y25									
		VCCA_FPLL					V26									
		VCCA_FPLL					V9									
		VCCA_FPLL					T26									
		VCCPLL_HPS					M9									
		VCCBATT					M27									
		VCC_AUX					AA24									
		VCC_AUX					F11									
		VCC_AUX					E24									
		VCC_AUX_SHARED					R12									
		VCCD_FPLL					Y26									
		VCCD_FPLL					V9									
		VCCD_FPLL					P26									
		VCCA_GXBLO					V28									
		VCCA_GXBRO					V7									
		VCCA_GXBL1					T28									
		VCCCH_GXBLO					V28									
		VCCCH_GXBRO					V16									
		VCCCH_GXBL1					P28									
		VCCCL_GXBLO					V29									
		VCCCL_GXBRO					V30									
		VCCCL_GXBRO					V5									
		VCCCL_GXBL1					Y5									
		VCCCL_GXBL1					P29									
		VCCCL_GXBL1					P30									
		VCCCR_GXBL					AA30									
		VCCCR_GXBL					AB29									
		VCCCR_GXBL					N30									
		VCCCR_GXBL					R29									
		VCCCR_GXBR					AA5									
		VCCCR_GXBR					AB6									
		VCCCR_GXBR					AB6									
		VCCCT_GXBLO					T30									
		VCCCT_GXBRO					U29									
		VCCCT_GXBLO					U30									
		VCCCT_GXBR0					W6									
		VCCCT_GXBR0					A8									
		VCCCT_GXBL1					W29									
		VCCCT_GXBL1					V30									
		VCC					AA30									
		VCC					T19									
		VCC					T23									
		VCC					T26									
		VCC					V24									
		VCC					U18									
		VCC					U20									
		VCC					U22									
		VCC					U24									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V20									
		VCC					V21									
		VCC					V22									
		VCC					V23									
		VCC					W16									
		VCC					W14									
		VCC					W20									
		VCC					W22									
		VCC					W24									
		VCC					Y13									
		VCC					Y14									
		VCC					Y15									
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y21									
		VCC					Y23									
		VCC					W18									
		VCC_HPS					T11									
		VCC_HPS					U10									
		VCC_HPS					U12									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V12									
		VCC_HPS					V13									
		VCC_HPS					W12									
		VCC_HPS					W27									
		VCC00A					AF30									
		VCC00A					AH30									
		VCC00A					AJ29									
		VCC00A					AK30									
		VCC00A					AN29									
		VCC00B					AF25									
		VCC00B					AK24									
		VCC00B					AN24									
		VCC00C					AD21									
		VCC00C					AF21									
		VCC00C					AJ21									
		VCC00C					AM21									
		VCC00D					AE18									
		VCC00D					AH18									
		VCC00D					AL18									
		VCC00A					AD5									
		VCC00A					AEB									
		VCC00A					AF5									
		VCC00A					AH5									
		VCC00A					AK5									
		VCC00A					AD11									
		VCC00A					AF10									
		VCC00A					AJ10									
		VCC00A					AM10									
		VCC00C					AE13									
		VCC00C					AH12									
		VCC00C					AL12									
		VCC00D					AF16									
		VCC00D					AJ16									
		VCC00D					AM15									
		VCC00D					AN17									
		VCC00A_HPS					B3									
		VCC00A_HPS					CB									
		VCC00A_HPS					DB									
		VCC00A_HPS					EB									
		VCC00A_HPS					FB									
		VCC00A_HPS					H5									
		VCC00A_HPS					H7									
		VCC00A_HPS					M7									
		VCC00B_HPS					L4									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					D30									
		GND					E14									
		GND					E25									
		GND					E28									
		GND					E8									
		GND					F19									
		GND					F22									
		GND					F5									
		GND					G11									
		GND					G2									
		GND					H25									
		GND					H28									
		GND					H8									
		GND					J13									
		GND					J19									
		GND					J22									
		GND					J5									
		GND					K16									
		GND					K2									
		GND					L25									
		GND					L28									
		GND					L8									
		GND					M18									
		GND					M22									
		GND					M5									
		GND					N11									
		GND					N15									
		GND					N2									
		GND					N24									
		GND					P13									
		GND					P18									
		GND					P8									
		GND					V18									
		GND					V14									
		GND					V16									
		GND					V8									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					W23									
		GND					W28									
		GND					W9									
		GND					Y18									
		GND					Z20									
		GND					R17									
		GND					R19									
		GND					R21									
		GND					R23									
		GND					R25									
		GND					R5									
		GND					R8									
		GND					T10									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T2									
		GND					T20									
		GND					T22									
		GND					T24									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U23									
		GND					U25									
		GND					U6									
		GND					U9									
		GND					V10									

Notes:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Altera V Device Family Pin Connection Guidelines](#).
- (2) GND, REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
- (3) Pins with * contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.
- (4) Pins with * are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).
- (5) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					B32									
		GND					B5									
		GND					B6									
		GND					E11									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E32									
		GND					E5									
		GND					E8									
		GND					F14									
		GND					H11									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					H21									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					K14									
		GND					K20									
		GND					L1									
		GND					L17									
		GND					L2									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L32									
		GND					L5									
		GND					L8									
		GND					N14									
		GND					N17									
		GND					N20									
		GND					P11									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P32									
		GND					P5									
		GND					W21									
		GND					T12									
		GND					T15									
		GND					T16									
		GND					T18									
		GND					T20									
		GND					T9									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U23									
		GND					U26									
		GND					U27									
		GND					U30									
		GND					U7									
		GND					V14									
		GND					V8									
		GND					V18									
		GND					V21									
		GND					V24									
		GND					V26									
		GND					V28									
		GND					V30									
		GND					V8									
		GND					W27									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W23									
		GND					W25									
		GND					W29									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V16									
		GND					V18									
		GND					V20									
		GND					V22									
		GND					V24									
		GND					V26									
		GND					V28									

Notes:
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).
 (2) QDR, REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
 (3) Pins with * contains similar name with other pins in the same column. For the selection of the "HPS Pin Mux Select x" columns.
 (4) Pins with # are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).
 (5) RESET pin is only applicable for DDR3 device.



**Pin Information for the Arria® V 5ASXFB5 Device
Version 1.3**

Version Number	Date	Changes Made
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.