



Bank Number	REF	PinName/Function (3, 2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F866 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		DNU					R29										
		DNU					T29										
		RRREF_TL					T30										
GXB_L1		REFCLK2n					W23										
GXB_L1		REFCLK2p					W24										
GXB_L1		GXB_TX_L11n					U27										
GXB_L1		GXB_TX_L11p					U28										
GXB_L1		GXB_RX_L11n	GXB_REFCLK_L11n				V29										
GXB_L1		GXB_RX_L11p	GXB_REFCLK_L11p				V29										
GXB_L1		GXB_TX_L10n					W27										
GXB_L1		GXB_TX_L10p					W28										
GXB_L1		GXB_RX_L10n	GXB_REFCLK_L10n				Y30										
GXB_L1		GXB_RX_L10p	GXB_REFCLK_L10p				Y30										
GXB_L1		GXB_TX_L8n					AA27										
GXB_L1		GXB_TX_L8p					AA28										
GXB_L1		GXB_RX_L8n	GXB_REFCLK_L8n				AB30										
GXB_L1		GXB_RX_L8p	GXB_REFCLK_L8p				AB29										
GXB_L1		GXB_TX_L6n					AC27										
GXB_L1		GXB_TX_L6p					AC28										
GXB_L1		GXB_RX_L6n	GXB_REFCLK_L6n				AD30										
GXB_L1		GXB_RX_L6p	GXB_REFCLK_L6p				AD29										
GXB_L1		GXB_TX_L7n					AE27										
GXB_L1		GXB_TX_L7p					AE28										
GXB_L1		GXB_RX_L7n	GXB_REFCLK_L7n				AF29										
GXB_L1		GXB_RX_L7p	GXB_REFCLK_L7p				AF29										
GXB_L1		GXB_TX_L6m					AG27										
GXB_L1		GXB_TX_L6p					AG28										
GXB_L1		GXB_RX_L6n	GXB_REFCLK_L6n				AH29										
GXB_L1		GXB_RX_L6p	GXB_REFCLK_L6p				AH29										
GXB_L1		REFCLK2ln					AA23										
GXB_L1		REFCLK2lp					AA22										
		DNU					AJ28										
JA		TD0		TD0			AF25										
JA		TD1		TD1			AK28										
JA		TKC		TKC			AH25										
JA		TDI		TDI			AG25										
JA		DCLK		DCLK			AK27										
JA		AS0		DATA4			AJ27										
JA		AS_DATA3		DATA3			AK28										
JA		AS_DATA2		DATA2			AE25										
JA		AS_DATA1		DATA1			AC25										
JA		AS_DATA0		DATA0			AK28										
JA	VREFBAND	IO	RZD_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AD25										
JA	VREFBAND	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AE24										
JA	VREFBAND	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AE24										
JA	VREFBAND	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AJ25										
JA	VREFBAND	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AK25										
JA	VREFBAND	IO	FPLL_B0	FPLL_B0_CLKOUT0_FPLL_B0_CLKOUT0	DIFFIO_TX_B5n	DIFFOUT_B5n	AD23										
JA	VREFBAND	IO	FPLL_B1	FPLL_B1_CLKOUT0_FPLL_B1_CLKOUT0	DIFFIO_TX_B5p	DIFFOUT_B5p	AE23										
JA	VREFBAND	IO	FPLL_B2	FPLL_B2_CLKOUT0_FPLL_B2_CLKOUT0	DIFFIO_RX_B6n	DIFFOUT_B6n	AG24										
JA	VREFBAND	IO	FPLL_B3	FPLL_B3_CLKOUT0_FPLL_B3_CLKOUT0	DIFFIO_RX_B6p	DIFFOUT_B6p	AH24										
JA	VREFBAND	IO	FPLL_B4	FPLL_B4_CLKOUT0_FPLL_B4_CLKOUT0	DIFFIO_RX_B7n	DIFFOUT_B7n	AJ24										
JA	VREFBAND	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AJ24										
JA	VREFBAND	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AK24										
JA	VREFBAND	IO	CLK3n		DIFFIO_TX_B8n	DIFFOUT_B8n	AC22										
JA	VREFBAND	IO	CLK3p		DIFFIO_TX_B8p	DIFFOUT_B8p	AC21	DG18									
JA	VREFBAND	IO	CLK3n		DIFFIO_RX_B8n	DIFFOUT_B8n	AG23	DG18									
JA	VREFBAND	IO	CLK3p		DIFFIO_RX_B8p	DIFFOUT_B8p	AH23	DG18									
JA	VREFBAND	IO	CLK4n		DIFFIO_TX_B10n	DIFFOUT_B10n	AE21	DG18									
JA	VREFBAND	IO	CLK4p		DIFFIO_TX_B10p	DIFFOUT_B10p	AD22	DG18									
JA	VREFBAND	IO	Q0n		DIFFIO_RX_B11n	DIFFOUT_B11n	AK23	DQ0n1B/QK1B									
JA	VREFBAND	IO	Q0p		DIFFIO_RX_B11p	DIFFOUT_B11p	AK22	DQ0p1B/QK1p1B									
JA	VREFBAND	IO	Q1n		DIFFIO_TX_B12n	DIFFOUT_B12n	AJ22	DG18									
JA	VREFBAND	IO	Q1p		DIFFIO_TX_B12p	DIFFOUT_B12p	AJ21	DG18									
JA	VREFBAND	IO	Q2n		DIFFIO_RX_B13n	DIFFOUT_B13n	AG22	DG18									
JA	VREFBAND	IO	Q2p		DIFFIO_RX_B13p	DIFFOUT_B13p	AG22	DG18									
JA	VREFBAND	IO	Q3n		DIFFIO_TX_B14n	DIFFOUT_B14n	AE18	DG18									
JA	VREFBAND	IO	Q3p		DIFFIO_TX_B14p	DIFFOUT_B14p	AF18	DG18									
JA	VREFBAND	IO	Q4n		DIFFIO_RX_B15n	DIFFOUT_B15n	AK21	DG18									
JA	VREFBAND	IO	Q4p		DIFFIO_RX_B15p	DIFFOUT_B15p	AK20	DG18									
JA	VREFBAND	IO	Q5n		DIFFIO_TX_B16n	DIFFOUT_B16n	AH21	DG18									
JA	VREFBAND	IO	Q5p		DIFFIO_TX_B16p	DIFFOUT_B16p	AH20	DG28									
JA	VREFBAND	IO	Q6n		DIFFIO_RX_B17n	DIFFOUT_B17n	AF21	DG28									
JA	VREFBAND	IO	Q6p		DIFFIO_RX_B17p	DIFFOUT_B17p	AK21	DG28									
JA	VREFBAND	IO	Q7n		DIFFIO_TX_B18n	DIFFOUT_B18n	AD21	DG28									
JA	VREFBAND	IO	Q7p		DIFFIO_TX_B18p	DIFFOUT_B18p	AD20	DG28									
JA	VREFBAND	IO	Q8n		DIFFIO_RX_B19n	DIFFOUT_B19n	AH19	DQS2B/QK2B	DQS1B/QK1B								
JA	VREFBAND	IO	Q8p		DIFFIO_RX_B19p	DIFFOUT_B19p	AK19	DQS2B/QK2B	DQS1B/QK1B								
JA	VREFBAND	IO	Q9n		DIFFIO_TX_B20n	DIFFOUT_B20n	AG20	DQS2B/QK2B	DQS1B/QK1B								
JA	VREFBAND	IO	Q9p		DIFFIO_TX_B20p	DIFFOUT_B20p	AG19	DG28									
JA	VREFBAND	IO	Q10n		DIFFIO_RX_B21n	DIFFOUT_B21n	AG18	DQ28									
JA	VREFBAND	IO	Q10p		DIFFIO_RX_B21p	DIFFOUT_B21p	AH18	DQ28									
JA	VREFBAND	IO	Q11n		DIFFIO_TX_B22n	DIFFOUT_B22n	AD19	DQ28									
JA	VREFBAND	IO	Q11p		DIFFIO_TX_B22p	DIFFOUT_B22p	AD18	DQ28									
JA	VREFBAND	IO	Q12n		DIFFIO_RX_B23n	DIFFOUT_B23n	AF19	DQ28									
JA	VREFBAND	IO	Q12p		DIFFIO_RX_B23p	DIFFOUT_B23p	AE20	DQ28									
JB	VREFBAND	IO	Q13n		DIFFIO_TX_B24n	DIFFOUT_B24n	AE15	DQ28									
JB	VREFBAND	IO	Q13p		DIFFIO_TX_B24p	DIFFOUT_B24p	AE14	DQ38									
JB	VREFBAND	IO	Q14n		DIFFIO_RX_B25n	DIFFOUT_B25n	AH18	DQ38									
JB	VREFBAND	IO	Q14p		DIFFIO_RX_B25p	DIFFOUT_B25p	AK18	DQ38									
JB	VREFBAND	IO	Q15n		DIFFIO_TX_B26n	DIFFOUT_B26n	AK15	DQ38									
JB	VREFBAND	IO	Q15p		DIFFIO_TX_B26p	DIFFOUT_B26p	AK14	DQ38									
JB	VREFBAND	IO	Q16n		DIFFIO_RX_B27n	DIFFOUT_B27n	AK17	DQS3B/QK3B	DQS2B/QK2B								
JB	VREFBAND	IO	Q16p		DIFFIO_RX_B27p	DIFFOUT_B27p	AK16	DQS3B/QK3B	DQS2B/QK2B								
JB	VREFBAND	IO	Q17n		DIFFIO_TX_B28n	DIFFOUT_B28n	AC16	DQ38									
JB	VREFBAND	IO	Q17p		DIFFIO_TX_B28p	DIFFOUT_B28p	AD15	DQ38									
JB	VREFBAND	IO	Q18n		DIFFIO_RX_B29n	DIFFOUT_B29n	AH16	DQ38									
JB	VREFBAND	IO	Q18p		DIFFIO_RX_B29p	DIFFOUT_B29p	AH15	DQ38									
JB	VREFBAND	IO	Q19n		DIFFIO_TX_B30n	DIFFOUT_B30n	AD16	DQ38									
JB	VREFBAND	IO	Q19p		DIFFIO_TX_B30p	DIFFOUT_B30p	AH16	DQ38									
JB	VREFBAND	IO	Q20n		DIFFIO_RX_B31n	DIFFOUT_B31n	AG17	DQ48									
JB	VREFBAND	IO	Q20p		DIFFIO_RX_B31p	DIFFOUT_B31p	AG14	DQ48									
JB	VREFBAND	IO	Q21n		DIFFIO_RX_B32n	DIFFOUT_B32n	AH14	DQ48									
JB	VREFBAND	IO	Q21p		DIFFIO_RX_B32p	DIFFOUT_B32p	AH14	DQ48									
JB	VREFBAND	IO	Q22n		DIFFIO_TX_B33n	DIFFOUT_B33n	AE17	DQ48									
JB	VREFBAND	IO	Q22p		DIFFIO_TX_B33p	DIFFOUT_B33p	AE17	DQ48									
JB	VREFBAND	IO	Q23n		DIFFIO_RX_B34n	DIFFOUT_B34n	AF16	DQS4B/QK4B	DQS3B/QK3B								
JB	VREFBAND	IO	Q23p		DIFFIO_RX_B34p	DIFFOUT_B34p	AG16	DQS4B/QK4B	DQS3B/QK3B								
JB	VREFBAND	IO	Q24n		DIFFIO_TX_B35n	DIFFOUT_B35n	AD14	DQ48									
JB	VREFBAND	IO	Q24p		DIFFIO_TX_B35p	DIFFOUT_B35p	AF15	DQ48									
JB	VREFBAND	IO	Q25n		DIFFIO_RX_B36n	DIFFOUT_B36n	AG15	DQ48									
JB	VREFBAND	IO	Q25p		DIFFIO_RX_B36p	DIFFOUT_B36p	AD13	DQ48									
JB	VREFBAND	IO	Q26n		DIFFIO_TX_B37n	DIFFOUT_B37n	AD13	DQ48									
JB	VREFBAND	IO	Q26p		DIFFIO_TX_B37p	DIFFOUT_B37p	AD13	DQ48									
JB	VREFBAND	IO	Q27n		DIFFIO_RX_B38n	DIFFOUT_B38n	AB13	DQ48									
JB	VREFBAND	IO	Q27p		DIFFIO_RX_B38p	DIFFOUT_B38p	AC13	DQ48									
JD	VREFBAND	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AJ13										
JD	VREFBAND	IO	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AK										



Pin Information for the Arria<sup>®</sup> V 5ASXBB5 Device  
Version 1.3  
Note (1)

Bank Number	VREF	PinName/Function (3, 2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DORS (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3D	VREFB3ND0	IO		CLK5n	DIFFIO_RX_B78n	DIFFOUT_B78n	AH12									
3D	VREFB3ND0	IO		CLK5p	DIFFIO_RX_B78p	DIFFOUT_B78p	AJ12									
3D	VREFB3ND0	IO			DIFFIO_TX_B79n	DIFFOUT_B79n	AB12									
3D	VREFB3ND0	IO			DIFFIO_TX_B79p	DIFFOUT_B79p	AC12									
3D	VREFB3ND0	IO			DIFFIO_RX_B80n	DIFFOUT_B80n	AH13									
3D	VREFB3ND0	IO			DIFFIO_RX_B80p	DIFFOUT_B80p	AG12									
3D	VREFB3ND0	IO		CLK6n	DIFFIO_RX_B82n	DIFFOUT_B82n	AF13									
3D	VREFB3ND0	IO		CLK6p	DIFFIO_RX_B82p	DIFFOUT_B82p	AE12									
3D	VREFB3ND0	IO		CLK7n	DIFFIO_RX_B84n	DIFFOUT_B84n	AD12									
3D	VREFB3ND0	IO		CLK7p	DIFFIO_RX_B84p	DIFFOUT_B84p	AD11									
		VCC2_FPLL					AB15									
		VCCA_FPLL					AB16									
		DNJ					AC16									
4A	VREFB4ND0	IO		DATA10	DIFFIO_TX_B140p	DIFFOUT_B140p	AC10	DQ58								
4A	VREFB4ND0	IO		DATA11	DIFFIO_RX_B147n	DIFFOUT_B147n	AE10	DQ58								
4A	VREFB4ND0	IO		DATA5	DIFFIO_RX_B147p	DIFFOUT_B147p	AF10	DQ58								
4A	VREFB4ND0	IO		DATA6	DIFFIO_TX_B148p	DIFFOUT_B148p	AD10	DQ58								
4A	VREFB4ND0	IO		DATA12	DIFFIO_TX_B149n	DIFFOUT_B149n	AH11	DQS0B/CQ0B/Q0x0B								
4A	VREFB4ND0	IO		DATA13	DIFFIO_RX_B149p	DIFFOUT_B149p	AH11	DQS0B/CQ0B/Q0x0B								
4A	VREFB4ND0	IO		DATA7	DIFFIO_TX_B150n	DIFFOUT_B150n	AK12	DQ58								
4A	VREFB4ND0	IO		DATA8	DIFFIO_TX_B150p	DIFFOUT_B150p	AK11	DQ58								
4A	VREFB4ND0	IO		DATA14	DIFFIO_RX_B151n	DIFFOUT_B151n	AG10	DQ58								
4A	VREFB4ND0	IO		DATA15	DIFFIO_RX_B151p	DIFFOUT_B151p	AH10	DQ58								
4A	VREFB4ND0	IO		DATA9	DIFFIO_TX_B152n	DIFFOUT_B152n	A89	DQ58								
4A	VREFB4ND0	IO		CLKUSR	DIFFIO_TX_B152p	DIFFOUT_B152p	A99	DQ58								
4A	VREFB4ND0	IO			DIFFIO_RX_B153n	DIFFOUT_B153n	AK10	DQ58								
4A	VREFB4ND0	IO			DIFFIO_RX_B153p	DIFFOUT_B153p	A99	DQ58								
4A	VREFB4ND0	IO		PR_ERROR	DIFFIO_TX_B154n	DIFFOUT_B154n	AJ10	DQ58								
4A	VREFB4ND0	IO		PR_READY	DIFFIO_TX_B154p	DIFFOUT_B154p	AJ9	DQ58								
4A	VREFB4ND0	IO		PR_DONE	DIFFIO_RX_B155n	DIFFOUT_B155n	AG9	DQ58								
4A	VREFB4ND0	IO		PR_REQUEST	DIFFIO_RX_B155p	DIFFOUT_B155p	AH9	DQ58								
4A	VREFB4ND0	IO			DIFFIO_TX_B156n	DIFFOUT_B156n	AD9	DQ58								
4A	VREFB4ND0	IO			DIFFIO_TX_B156p	DIFFOUT_B156p	AC8	DQ58								
4A	VREFB4ND0	IO		CLP_CONF_DONE	DIFFIO_RX_B157n	DIFFOUT_B157n	AK8	DQS0B/CQ0B								
4A	VREFB4ND0	IO		CRC_ERROR	DIFFIO_TX_B157p	DIFFOUT_B157p	AK7	DQS0B/CQ0B/Q0x0B								
4A	VREFB4ND0	IO		DEV_DE	DIFFIO_TX_B158n	DIFFOUT_B158n	AK6	DQ58								
4A	VREFB4ND0	IO		DEV_CLRn	DIFFIO_TX_B158p	DIFFOUT_B158p	AK5	DQ58								
4A	VREFB4ND0	IO		INT_DONE	DIFFIO_RX_B159n	DIFFOUT_B159n	AG8	DQ58								
4A	VREFB4ND0	IO		ICE0	DIFFIO_RX_B159p	DIFFOUT_B159p	AH8	DQ58								
4A	VREFB4ND0	IO		VREFB4ND0			AC9	DQ58								
4A	VREFB4ND0	IO					AE8	DQ58								
4A	VREFB4ND0	IO		CLK11n	DIFFIO_RX_B160n	DIFFOUT_B160n	AJ4	DQ58								
4A	VREFB4ND0	IO		CLK11p	DIFFIO_RX_B160p	DIFFOUT_B160p	AK4	DQ58								
4A	VREFB4ND0	IO			DIFFIO_TX_B161n	DIFFOUT_B161n	AJ7	DQ58								
4A	VREFB4ND0	IO			DIFFIO_TX_B161p	DIFFOUT_B161p	AJ6	DQ58								
4A	VREFB4ND0	IO			DIFFIO_RX_B162n	DIFFOUT_B162n	AG6	DQ58								
4A	VREFB4ND0	IO			DIFFIO_RX_B162p	DIFFOUT_B162p	AH6	DQ58								
4A	VREFB4ND0	IO		CLK10n	DIFFIO_RX_B164n	DIFFOUT_B164n	AJ7	DQ58								
4A	VREFB4ND0	IO		CLK10p	DIFFIO_RX_B164p	DIFFOUT_B164p	AG7	DQ58								
4A	VREFB4ND0	IO		CLK9n	DIFFIO_RX_B166n	DIFFOUT_B166n	AE6	DQ58								
4A	VREFB4ND0	IO		CLK9p	DIFFIO_RX_B166p	DIFFOUT_B166p	AF6	DQ58								
4A	VREFB4ND0	IO			DIFFIO_TX_B167n	DIFFOUT_B167n	AC7	DQ58								
4A	VREFB4ND0	IO		RZQ_1	DIFFIO_TX_B167p	DIFFOUT_B167p	AD7	DQ58								
4A	VREFB4ND0	IO		CLK8n	DIFFIO_RX_B168n	DIFFOUT_B168n	AC6	DQ58								
4A	VREFB4ND0	IO		CLK8p	DIFFIO_RX_B168p	DIFFOUT_B168p	AD6	DQ58								
		RREF_BR					AK2									
		DNJ					AJ3									
		DNJ					AK3									
GXB_R0		REFCLK0Rn					AA8									
GXB_R0		REFCLK0Rp					AA8									
GXB_R0		GXB_RX_R0nGXB_REFCLK_R0n					AH2									
GXB_R0		GXB_RX_R0pGXB_REFCLK_R0p					AH1									
GXB_R0		GXB_TX_R0n					AG3									
GXB_R0		GXB_TX_R0p					AJ4									
GXB_R0		GXB_RX_R1nGXB_REFCLK_R1n					AF2									
GXB_R0		GXB_RX_R1pGXB_REFCLK_R1p					AF1									
GXB_R0		GXB_TX_R1n					AE3									
GXB_R0		GXB_TX_R1p					AE4									
GXB_R0		GXB_RX_R2nGXB_REFCLK_R2n					AD2									
GXB_R0		GXB_RX_R2pGXB_REFCLK_R2p					AD1									
GXB_R0		GXB_TX_R2n					AC3									
GXB_R0		GXB_TX_R2p					AC4									
		GND					AB2									
		GND					AB1									
		DNJ					AK3									
		DNJ					AA4									
		GND					Y2									
		GND					V1									
		DNJ					W3									
		DNJ					W4									
		GND					V2									
		GND					V1									
		DNJ					U3									
		DNJ					U4									
		GND					W9									
		GND					W8									
BB	VREFB8ND0_HPS	HPS_D0R					R4				HPS_DM_4	HPS_DM_4				
BB	VREFB8ND0_HPS	HPS_D0R					R5				HPS_DQ_39	HPS_DQ_39				
BB	VREFB8ND0_HPS	HPS_D0R					P7				HPS_DQ_37	HPS_DQ_37				
BB	VREFB8ND0_HPS	HPS_D0R					N7				HPS_DQ_38	HPS_DQ_38				
BB	VREFB8ND0_HPS	HPS_D0R					R7				HPS_DQ_38	HPS_DQ_38				
BB	VREFB8ND0_HPS	HPS_D0R					R3				HPS_DQS_4	HPS_DQS_4				
BB	VREFB8ND0_HPS	HPS_GPI13					T7									
BB	VREFB8ND0_HPS	HPS_D0R					R2				HPS_DQS#_4	HPS_DQS#_4				
BB	VREFB8ND0_HPS	HPS_D0R					T8				HPS_DQ_35	HPS_DQ_35				
BB	VREFB8ND0_HPS	HPS_D0R					R1				HPS_DQ_33	HPS_DQ_33				
BB	VREFB8ND0_HPS	HPS_D0R					M6				HPS_DQ_34	HPS_DQ_34				
BB	VREFB8ND0_HPS	HPS_D0R					T1				HPS_DQ_32	HPS_DQ_32				
BB	VREFB8ND0_HPS	HPS_GPI12					N6									
BB	VREFB8ND0_HPS	HPS_GPI11					N3									
BB	VREFB8ND0_HPS	HPS_D0R					R4				HPS_DM_3	HPS_DM_3				
BB	VREFB8ND0_HPS	HPS_GPI10					P3									
BB	VREFB8ND0_HPS	HPS_D0R					N5				HPS_DQ_31	HPS_DQ_31				
BB	VREFB8ND0_HPS	HPS_D0R					A2				HPS_DQ_29	HPS_DQ_29				
BB	VREFB8ND0_HPS	HPS_D0R					R6				HPS_DQ_30	HPS_DQ_30				
BB	VREFB8ND0_HPS	HPS_D0R					P1				HPS_DQ_28	HPS_DQ_28				
BB	VREFB8ND0_HPS	VREFB8ND0_HPS					T6									
BB	VREFB8ND0_HPS	HPS_D0R					M2				HPS_DQS_3	HPS_DQS_3				
BB	VREFB8ND0_HPS	HPS_GPI9					L1									
BB	VREFB8ND0_HPS	HPS_D0R					M3				HPS_DQS#_3	HPS_DQS#_3				
BB	VREFB8ND0_HPS	HPS_D0R					L1				HPS_DQ_27	HPS_DQ_27				
BB	VREFB8ND0_HPS	HPS_D0R					L4				HPS_DQ_25	HPS_DQ_25				
BB	VREFB8ND0_HPS	HPS_D0R					L9				HPS_DQ_26	HPS_DQ_26				
BB	VREFB8ND0_HPS	HPS_D0R					M4				HPS_DQ_24	HPS_DQ_24				
BB	VREFB8ND0_HPS	HPS_GPI8					T9									
BB	VREFB8ND0_HPS	HPS_GPI7					K1									
BB	VREFB8ND0_HPS	HPS_D0R					L3				HPS_DM_2	HPS_DM_2				

Bank Number	VREF	PinName/Function (3, (2))	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DORS (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GB	VREFBAND0_HPS	HPS_GP#6					J1									
GB	VREFBAND0_HPS	HPS_DDR					K3									
GB	VREFBAND0_HPS	HPS_DDR					M4				HPS_DO_23	HPS_DO_23				
GB	VREFBAND0_HPS	HPS_DDR					J8				HPS_DO_21	HPS_DO_21				
GB	VREFBAND0_HPS	HPS_DDR					M5				HPS_DO_22	HPS_DO_22				
GB	VREFBAND0_HPS	HPS_DDR					K8				HPS_DO_20	HPS_DO_20				
GB	VREFBAND0_HPS	HPS_DDR					G8				HPS_DQS_2	HPS_DQS_2				
GB	VREFBAND0_HPS	HPS_DDR					J2				HPS_RESET#	HPS_RESET#				
GB	VREFBAND0_HPS	HPS_DDR					F8				HPS_DQS#_2	HPS_DQS#_2				
GB	VREFBAND0_HPS	HPS_DDR					K2				HPS_DO_19	HPS_DO_19				
GB	VREFBAND0_HPS	HPS_DDR					J4				HPS_DO_17	HPS_DO_17				
GB	VREFBAND0_HPS	HPS_DDR					R9				HPS_DO_18	HPS_DO_18				
GB	VREFBAND0_HPS	HPS_DDR					J3				HPS_DO_16	HPS_DO_16				
GB	VREFBAND0_HPS	HPS_GPI4					P9									
GA	VREFBAND0_HPS	HPS_GPI3					D1									
GA	VREFBAND0_HPS	HPS_DDR					E3				HPS_DM_1	HPS_DM_1				
GA	VREFBAND0_HPS	HPS_GPI2					C1									
GA	VREFBAND0_HPS	HPS_DDR					F3				HPS_DO_15	HPS_DO_15				
GA	VREFBAND0_HPS	HPS_DDR					F1				HPS_DO_13	HPS_DO_13				
GA	VREFBAND0_HPS	HPS_DDR					M7				HPS_DO_14	HPS_DO_14				
GA	VREFBAND0_HPS	HPS_DDR					G1				HPS_DO_12	HPS_DO_12				
GA	VREFBAND0_HPS	HPS_DDR					L7				HPS_CKE_0	HPS_CKE_0				
GA	VREFBAND0_HPS	HPS_DDR					D2				HPS_DQS_1	HPS_DQS_1				
GA	VREFBAND0_HPS	HPS_DDR					A2				HPS_CAE_1	HPS_CAE_1				
GA	VREFBAND0_HPS	HPS_DDR					E1				HPS_DQS#_1	HPS_DQS#_1				
GA	VREFBAND0_HPS	HPS_DDR					B1				HPS_DO_11	HPS_DO_11				
GA	VREFBAND0_HPS	HPS_DDR					A3				HPS_DO_9	HPS_DO_9				
GA	VREFBAND0_HPS	HPS_DDR					G2				HPS_DO_10	HPS_DO_10				
GA	VREFBAND0_HPS	HPS_DDR					B3				HPS_DO_8	HPS_DO_8				
GA	VREFBAND0_HPS	HPS_GPI1					H3									
GA	VREFBAND0_HPS	HPS_GPI0					A4									
GA	VREFBAND0_HPS	HPS_DDR					K5				HPS_DM_0	HPS_DM_0				
GA	VREFBAND0_HPS	HPS_DDR					K6				HPS_DO_7	HPS_DO_7				
GA	VREFBAND0_HPS	HPS_DDR					G3				HPS_DO_5	HPS_DO_5				
GA	VREFBAND0_HPS	HPS_DDR					A4				HPS_DO_6	HPS_DO_6				
GA	VREFBAND0_HPS	HPS_DDR					C3				HPS_DO_4	HPS_DO_4				
GA	VREFBAND0_HPS	HPS_DDR					B4				HPS_ODT_1	HPS_ODT_1				
GA	VREFBAND0_HPS	HPS_DDR					A5				HPS_DQS_0	HPS_DQS_0				
GA	VREFBAND0_HPS	HPS_DDR					G3				HPS_ODT_0	HPS_ODT_0				
GA	VREFBAND0_HPS	HPS_DDR					B6				HPS_DQS#_0	HPS_DQS#_0				
GA	VREFBAND0_HPS	HPS_DDR					G4				HPS_DO_3	HPS_DO_3				
GA	VREFBAND0_HPS	HPS_DDR					C4				HPS_DO_1	HPS_DO_1				
GA	VREFBAND0_HPS	HPS_DDR					E7				HPS_DO_2	HPS_DO_2				
GA	VREFBAND0_HPS	HPS_DDR					G4				HPS_DO_0	HPS_DO_0				
GA	VREFBAND0_HPS	VREFBAND0_HPS					K7									
GA	VREFBAND0_HPS	HPS_DDR					F5				HPS_A_0	HPS_CA_0				
GA	VREFBAND0_HPS	HPS_DDR					E4				HPS_A_1	HPS_CA_1				
GA	VREFBAND0_HPS	HPS_DDR					B7				HPS_A_4	HPS_CA_4				
GA	VREFBAND0_HPS	HPS_DDR					G5				HPS_A_2	HPS_CA_2				
GA	VREFBAND0_HPS	HPS_DDR					A6				HPS_A_5	HPS_CA_5				
GA	VREFBAND0_HPS	HPS_DDR					H6				HPS_A_3	HPS_CA_3				
GA	VREFBAND0_HPS	HPS_DDR					G6				HPS_CK	HPS_CK				
GA	VREFBAND0_HPS	HPS_DDR					A8				HPS_A_6	HPS_CA_6				
GA	VREFBAND0_HPS	HPS_DDR					G7				HPS_CKE	HPS_CKE				
GA	VREFBAND0_HPS	HPS_DDR					A7				HPS_CLV_7	HPS_CLV_7				
GA	VREFBAND0_HPS	HPS_DDR					A10				HPS_BA_1					
GA	VREFBAND0_HPS	HPS_DDR					H7				HPS_BA_0					
GA	VREFBAND0_HPS	HPS_DDR					A8				HPS_BA_2					
GA	VREFBAND0_HPS	HPS_DDR					E6				HPS_CAS#					
GA	VREFBAND0_HPS	HPS_DDR					D5				HPS_RAS#					
GA	VREFBAND0_HPS	HPS_DDR					D6				HPS_A_8	HPS_CA_8				
GA	VREFBAND0_HPS	HPS_DDR					J6				HPS_A_10					
GA	VREFBAND0_HPS	HPS_DDR					C6				HPS_A_9	HPS_CA_9				
GA	VREFBAND0_HPS	HPS_DDR					J7				HPS_A_11					
GA	VREFBAND0_HPS	HPS_DDR					C9				HPS_CSN_0	HPS_CSN_0				
GA	VREFBAND0_HPS	HPS_DDR					D7				HPS_A_12					
GA	VREFBAND0_HPS	HPS_DDR					C10				HPS_CSN_1	HPS_CSN_1				
GA	VREFBAND0_HPS	HPS_DDR					C7				HPS_A_13					
GA	VREFBAND0_HPS	HPS_DDR					D9				HPS_A_14					
GA	VREFBAND0_HPS	HPS_DDR					B9				HPS_WE#					
GA	VREFBAND0_HPS	HPS_DDR					D8				HPS_A_15					
GA	VREFBAND0_HPS	HPS_RZQ_0					B10									
	DNU						F7									
	GND						P9									
	GND						F10									
ZA	HPS_nRST						M8									
ZA	HPS_nPOR						H10									
ZA	HPS_TDO						H9									
ZA	VDDRSTCLK_HPS						L9									
ZA	HPS_TMS						L9									
ZA	HPS_TXC						J11									
ZA	HPS_TRST						K9									
ZA	HPS_TDI						J11									
	GND						A19									
ZA	HPS_PORSEL						A13									
ZA	HPS_CLK1						A11									
ZA	HPS_CLK2						A14									
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_CLK					A15						TRACE_CLK			HPS_GPI048
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_D0					K10						TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPI049
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_D1					A16						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPI050
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_D2					L10						TRACE_D2	SPIS0_MISO	IC21_SDA	HPS_GPI051
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_D3					A18						TRACE_D3	SPIS0_SS0	IC21_SCL	HPS_GPI052
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_D4					L11						TRACE_D4	SPIS1_CLK		HPS_GPI053
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_D6					A17						TRACE_D6	SPIS1_MOSI		HPS_GPI054
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_D6					M11						TRACE_D6	SPIS1_SS0	IC20_SDA	HPS_GPI055
ZA	VREFB7A78/C7D7EN0_HPS	TRACE_D7					B15						TRACE_D7	SPIS1_MISO	IC20_SCL	HPS_GPI056
ZA	VREFB7A78/C7D7EN0_HPS	SPIM0_CLK					A20						SPIM0_CLK	IC21_SDA	UART0_CTS	HPS_GPI057
ZA	VREFB7A78/C7D7EN0_HPS	SPIM0_MOSI					B16						SPIM0_MOSI	IC21_SCL	UART0_RTS	HPS_GPI058
ZA	VREFB7A78/C7D7EN0_HPS	SPIM0_MISO					A19						SPIM0_MISO	UART1_CTS		HPS_GPI059
ZA	VREFB7A78/C7D7EN0_HPS	SPIM0_SS0					B13						SPIM0_SS0	UART1_RTS		HPS_GPI060
ZA	VREFB7A78/C7D7EN0_HPS	UART0_RX					A12						UART0_RX		SPIM0_SS1	HPS_GPI061
ZA	VREFB7A78/C7D7EN0_HPS	UART0_TX					B12						UART0_TX		SPIM1_SS1	HPS_GPI062
ZA	VREFB7A78/C7D7EN0_HPS	IC20_SDA					B12						IC20_SDA	UART1_RX	SPIM1_CLK	HPS_GPI063
ZA	VREFB7A78/C7D7EN0_HPS	IC20_SCL					B18						IC20_SCL	UART1_TX	SPIM1_MISO	HPS_GPI064
ZA	VREFB7A78/C7D7EN0_HPS	UART0_RX*					C11						UART0_RX		SPIM1_MISO	HPS_GPI065
ZA	VREFB7A78/C7D7EN0_HPS	UART0_TX*					B19						UART0_TX		SPIM1_SS0	HPS_GPI066
ZA	VREFB7A78/C7D7EN0_HPS	SPIS1_CLK					D10						SPIS1_CLK	SPIM1_CLK		HPS_GPI067
ZA	VREFB7A78/C7D7EN0_HPS	SPIS1_MOSI					F11						SPIS1_MOSI	SPIM1_MOSI		HPS_GPI068
ZA	VREFB7A78/C7D7EN0_HPS	SPIS1_MISO					J10						SPIS1_MISO	SPIM1_MISO		HPS_GPI069
ZA	VREFB7A78/C7D7EN0_HPS	SPIS1_SS0					G11						SPIS1_SS0	SPIM1_SS0		HPS_GPI070
ZA	VREFB7A78/C7D7EN0_HPS	UART1_RX					B						UART1_RX	SPIM1_SS1		HPS_GPI071
ZA	VREFB7A78/C7D7EN0_HPS	UART1_TX					A21						UART1_TX	SPIM0_CLK		HPS_GPI072
ZA	VREFB7A78/C7D7EN0_HPS	IC21_SDA					F10						IC21_SDA	SPIM0_MOSI		HPS_GPI073
ZA	VREFB7A78/C7D7EN0_HPS	IC21_SCL					A22						IC21_SCL	SPIM0_MISO		HPS_GPI074
ZA	VREFB7A78/C7D7EN0_HPS	SPIM0_SS0					E9						SPIM0_SS0			HPS_GPI075
ZA	VREFB7A78/C7D7EN0_HPS	SPIS0_CLK					D11						SPIS0_CLK	SPIM0_SS1		HPS_GPI076
ZA	VREFB7A78/C7D7EN0_HPS	SPIS0_MOSI					P12						SPIS0_MOSI			HPS_GPI077



Bank Number	VFREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	FB96 (4)	DO5 for X8/X9	DO5 for X16/X18	DO5 for X32/X36	HMC pin assignment for DOR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7A	VREFB7A7B7C7D7E7F	SPISO_MISO					E11						SPISO_MISO			HPS_GPIO69
7A	VREFB7A7B7C7D7E7F	SPISO_SS0					P13						SPISO_SS0			HPS_GPIO70
7B	VREFB7A7B7C7D7E7F	NAND_ALE					A23						NAND_ALE	RGMII_TX_CLK	QSPI_SS3	HPS_GPIO14
7B	VREFB7A7B7C7D7E7F	NAND_CE					E22						NAND_CE	RGMII_TXD0	USB1_D9	HPS_GPIO15
7B	VREFB7A7B7C7D7E7F	NAND_GLE					B22						NAND_GLE	RGMII_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A7B7C7D7E7F	NAND_RE					D21						NAND_RE	RGMII_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A7B7C7D7E7F	NAND_RB					A24						NAND_RB	RGMII_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A7B7C7D7E7F	NAND_DQ0					C12						NAND_DQ0	RGMII_RXD0		HPS_GPIO19
7B	VREFB7A7B7C7D7E7F	NAND_DQ1					B24						NAND_DQ1	RGMII_RXD0	ZC2_SDA	HPS_GPIO20
7B	VREFB7A7B7C7D7E7F	NAND_DQ2					D12						NAND_DQ2	RGMII_RXD1	ZC2_SCL	HPS_GPIO21
7B	VREFB7A7B7C7D7E7F	NAND_DQ3					C16						NAND_DQ3	RGMII_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A7B7C7D7E7F	NAND_DQ4					C14						NAND_DQ4	RGMII_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A7B7C7D7E7F	NAND_DQ5					C16						NAND_DQ5	RGMII_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A7B7C7D7E7F	NAND_DQ6					C13						NAND_DQ6	RGMII_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A7B7C7D7E7F	NAND_DQ7					E18						NAND_DQ7	RGMII_RXD2		HPS_GPIO26
7B	VREFB7A7B7C7D7E7F	NAND_WP					K12						NAND_WP	RGMII_RXD3	QSPI_SS2	HPS_GPIO27
7B	VREFB7A7B7C7D7E7F	NAND_WE					C17						NAND_WE	QSPI_SS1		HPS_GPIO28
7B	VREFB7A7B7C7D7E7F	QSPI_D0					H12						QSPI_D0		USB1_CLK	HPS_GPIO29
7B	VREFB7A7B7C7D7E7F	QSPI_I01					B21						QSPI_I01		USB1_STP	HPS_GPIO30
7B	VREFB7A7B7C7D7E7F	QSPI_I02					C20						QSPI_I02		USB1_DR	HPS_GPIO31
7B	VREFB7A7B7C7D7E7F	QSPI_I03					C21						QSPI_I03		USB1_NXT	HPS_GPIO32
7B	VREFB7A7B7C7D7E7F	QSPI_SS0					C19						QSPI_SS0			HPS_GPIO33
7B	VREFB7A7B7C7D7E7F	QSPI_CLK					A26						QSPI_CLK			HPS_GPIO34
7B	VREFB7A7B7C7D7E7F	QSPI_SS1					B26						QSPI_SS1			HPS_GPIO35
7C	VREFB7A7B7C7D7E7F	SDMMC_CMD					D13						SDMMC_CMD	USBD_D0		HPS_GPIO36
7C	VREFB7A7B7C7D7E7F	SDMMC_PWREN					K13						SDMMC_PWREN	USBD_D1		HPS_GPIO37
7C	VREFB7A7B7C7D7E7F	SDMMC_D0					D14						SDMMC_D0	USBD_D2		HPS_GPIO38
7C	VREFB7A7B7C7D7E7F	SDMMC_D1					L13						SDMMC_D1	USBD_D3		HPS_GPIO39
7C	VREFB7A7B7C7D7E7F	SDMMC_D4					E13						SDMMC_D4	USBD_D4		HPS_GPIO40
7C	VREFB7A7B7C7D7E7F	SDMMC_D6					N13						SDMMC_D6	USBD_D6		HPS_GPIO41
7C	VREFB7A7B7C7D7E7F	SDMMC_D8					F13						SDMMC_D8	USBD_D8		HPS_GPIO42
7C	VREFB7A7B7C7D7E7F	SDMMC_D7					P14						SDMMC_D7	USBD_D7		HPS_GPIO43
7C	VREFB7A7B7C7D7E7F	HPS_GPIO44					G13						USBD_CLK			HPS_GPIO44
7C	VREFB7A7B7C7D7E7F	SDMMC_CLK_OUT					J13						SDMMC_CLK_OUT	USBD_STP		HPS_GPIO45
7C	VREFB7A7B7C7D7E7F	SDMMC_D2					H13						SDMMC_D2	USBD_DIR		HPS_GPIO46
7C	VREFB7A7B7C7D7E7F	SDMMC_D5					H12						SDMMC_D5	USBD_NXT		HPS_GPIO47
7D	VREFB7A7B7C7D7E7F	RGMII_TX_CLK					L15						RGMII_TX_CLK			HPS_GPIO1
7D	VREFB7A7B7C7D7E7F	RGMII_TXD0					N15						RGMII_TXD0	USBD_D0		HPS_GPIO1
7D	VREFB7A7B7C7D7E7F	RGMII_TXD1					K15						RGMII_TXD1	USBD_D1		HPS_GPIO2
7D	VREFB7A7B7C7D7E7F	RGMII_TXD2					P16						RGMII_TXD2	USBD_D2		HPS_GPIO3
7D	VREFB7A7B7C7D7E7F	RGMII_TXD3					D16						RGMII_TXD3	USBD_D3		HPS_GPIO4
7D	VREFB7A7B7C7D7E7F	RGMII_RXD0					M15						RGMII_RXD0	USBD_D4		HPS_GPIO5
7D	VREFB7A7B7C7D7E7F	RGMII_MDIO					E15						RGMII_MDIO	USBD_D6	ZC2_SDA	HPS_GPIO6
7D	VREFB7A7B7C7D7E7F	RGMII_MDC					M16						RGMII_MDC	USBD_D8	ZC2_SCL	HPS_GPIO7
7D	VREFB7A7B7C7D7E7F	RGMII_RX_CTL					D17						RGMII_RX_CTL	USBD_D7		HPS_GPIO8
7D	VREFB7A7B7C7D7E7F	RGMII_TX_CTL					M14						RGMII_TX_CTL			HPS_GPIO9
7D	VREFB7A7B7C7D7E7F	RGMII_RX_CLK					D16						RGMII_RX_CLK	USBD_CLK		HPS_GPIO10
7D	VREFB7A7B7C7D7E7F	RGMII_RXD1					L14						RGMII_RXD1	USBD_STP		HPS_GPIO11
7D	VREFB7A7B7C7D7E7F	RGMII_RXD2					F15						RGMII_RXD2	USBD_DIR		HPS_GPIO12
7D	VREFB7A7B7C7D7E7F	RGMII_RXD3					D19						RGMII_RXD3	USBD_NXT		HPS_GPIO13
7D	VREFB7A7B7C7D7E7F	RGMII_TX_CLK					E16						RGMII_TX_CLK			HPS_GPIO14
7D	VREFB7A7B7C7D7E7F	RGMII_TXD0					D18						RGMII_TXD0			HPS_GPIO14
7D	VREFB7A7B7C7D7E7F	RGMII_TXD1					E19						RGMII_TXD1			HPS_GPIO15
7D	VREFB7A7B7C7D7E7F	RGMII_TX_CTL					H15						RGMII_TX_CTL			HPS_GPIO16
7D	VREFB7A7B7C7D7E7F	RGMII_RXD0					D20						RGMII_RXD0			HPS_GPIO17
7D	VREFB7A7B7C7D7E7F	RGMII_RXD1					H14						RGMII_RXD1			HPS_GPIO18
7E	VREFB7A7B7C7D7E7F	RGMII_MDIO					F16						RGMII_MDIO	SPIM0_CLK	SPIS0_CLK	HPS_GPIO4
7E	VREFB7A7B7C7D7E7F	RGMII_MDC					H16						RGMII_MDC	SPIM0_MOSI	SPIS0_MOSI	HPS_GPIO5
7E	VREFB7A7B7C7D7E7F	RGMII_TXD0					F17						RGMII_TXD0	SPIM0_MISO	SPIS0_MISO	HPS_GPIO6
7E	VREFB7A7B7C7D7E7F	RGMII_TXD1					H17						RGMII_TXD1	SPIM0_SS0	SPIS0_SS0	HPS_GPIO7
7E	VREFB7A7B7C7D7E7F	RGMII_RX_CLK					E16	DO5nTQ0K1T					RGMII_RX_CLK	SPIM1_CLK	SPIM1_CLK	HPS_GPIO8
7E	VREFB7A7B7C7D7E7F	RGMII_RX_CTL					R16						RGMII_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	HPS_GPIO9
7E	VREFB7A7B7C7D7E7F	RGMII_RXD2					K16						RGMII_RXD2	SPIS1_MISO	SPM1_MISO	HPS_GPIO10
7E	VREFB7A7B7C7D7E7F	RGMII_RXD3					F16						RGMII_RXD3	SPIS1_SS0	SPM1_SS0	HPS_GPIO11
		VOCA_FPLL					F16									
		VCCD_FPLL					T15									
		INU					G19									
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T31b	DIFFOUT_T31b	M17									DOIT
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T31a	DIFFOUT_T31a	N17									DOIT
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T33p	DIFFOUT_T33p	F18									DOIT
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T33a	DIFFOUT_T33a	G18									DOIT
8D	VREFB8D0	IO	FPLL_TC_CLKOUT2_FPLL_TC_Fb0_FPLL_TC_FB1		DIFFIO_RX_T35p	DIFFOUT_T35p	F19									DOIT
8D	VREFB8D0	IO	FPLL_TC_CLKOUT3_FPLL_TC_FBn		DIFFIO_RX_T35a	DIFFOUT_T35a	G19									DOIT
8D	VREFB8D0	IO	FPLL_TC_CLKOUT3_FPLL_TC_CLKOUT4_FPLL_TC_FB0		DIFFIO_TX_T39p	DIFFOUT_T39p	J17									DOIT
8D	VREFB8D0	IO	FPLL_TC_CLKOUT3_FPLL_TC_CLKOUT5		DIFFIO_TX_T39a	DIFFOUT_T39a	H18									DOIT
8D	VREFB8D0	IO	CLK17p		DIFFIO_RX_T37p	DIFFOUT_T37p	H18									DOIT
8D	VREFB8D0	IO	CLK17n		DIFFIO_RX_T37n	DIFFOUT_T37n	H19									DOIT
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T39p	DIFFOUT_T39p	F20									DOIT
8D	VREFB8D0	IO	CLK19n		DIFFIO_RX_T39a	DIFFOUT_T39a	G20									DOIT
8C	VREFB8C0	IO	VREFB8D0		DIFFIO_RX_T54p	DIFFOUT_T54p	G17									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T54a	DIFFOUT_T54a	K20									DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T55p	DIFFOUT_T55p	P19									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	J20									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	H21									DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	N18									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	D22	DO5nTQ0K1T								DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T56a	DIFFOUT_T56a	E22	DO5nTQ0K1T								DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	M18									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T60p	DIFFOUT_T60p	A29									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T60a	DIFFOUT_T60a	B30									DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T61p	DIFFOUT_T61p	L18									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T62p	DIFFOUT_T62p	C23									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T62a	DIFFOUT_T62a	G23									DOIT
8C	VREFB8C0	IO					K18									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	A28									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T63a	DIFFOUT_T63a	B29									DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	M19									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T65p	DIFFOUT_T65p	D24	DO5nTQ0K1T								DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T65a	DIFFOUT_T65a	E24	DO5nTQ0K1T								DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T66p	DIFFOUT_T66p	N19									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T67p	DIFFOUT_T67p	B27									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T67a	DIFFOUT_T67a	E27									DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	A28									DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T68a	DIFFOUT_T68a	A27									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T69p	DIFFOUT_T69p	F21									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T69a	DIFFOUT_T69a	G21									DOIT
8C	VREFB8C0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	M20									DOIT
8C	VREFB8C0	IO			DIFFIO_RX_T71p	DIFFOUT_T71										



Bank Number	VREF	PinName/Function (3, 2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	#B66 (4)	QDS for X8/X9	QDS for X16/ X18	QDS for X32/ X36	HMC pin assignment for DORS (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
0C	VREFBAND	IO			DIFFIO_TX_176a	DIFFOUT_176a	K21	DQ0T								
0B	VREFBAND	IO			DIFFIO_RX_177a	DIFFOUT_177a	K22	DQ4T	DQ1T							
0B	VREFBAND	IO			DIFFIO_RX_177a	DIFFOUT_177a	J22	DQ4T		DQ1T						
0B	VREFBAND	IO			DIFFIO_TX_178a	DIFFOUT_178a	G23	DQ4T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_178a	DIFFOUT_178a	M23	DQ4T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_179a	DIFFOUT_179a	L22	DQ4T		DQ2T						
0B	VREFBAND	IO			DIFFIO_TX_180a	DIFFOUT_180a	J23	DQ4T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_181a	DIFFOUT_181a	E23	DQS4T/CQ4T/CQ4+T/DQ4+T	DQS8T/CQ2T/CQ2+T/DQ2+T							
0B	VREFBAND	IO			DIFFIO_RX_181a	DIFFOUT_181a	F24	DQS4T/DQ4T	DQS8+T/DQ4+T							
0B	VREFBAND	IO			DIFFIO_TX_182a	DIFFOUT_182a	H24	DQ4T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_183a	DIFFOUT_183a	K21	DQ4T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_183a	DIFFOUT_183a	M21	DQ4T		DQ2T						
0B	VREFBAND	IO			DIFFIO_TX_184a	DIFFOUT_184a	K24	DQ4T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_185a	DIFFOUT_185a	F26	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_185a	DIFFOUT_185a	F27	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_185a	DIFFOUT_185a	J24	DQ6T		DQ2T						
0B	VREFBAND	IO	VREFBAND0		DIFFIO_RX_186a	DIFFOUT_186a	H27	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_186a	DIFFOUT_186a	D28	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_TX_187a	DIFFOUT_187a	K25	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_TX_187a	DIFFOUT_187a	L24	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_188a	DIFFOUT_188a	C28	DQS8T/CQ8T/CQ8+T/DQ8+T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_188a	DIFFOUT_188a	C29	DQS8+T/DQ8+T		DQ2T						
0B	VREFBAND	IO			DIFFIO_TX_189a	DIFFOUT_189a	G24	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_TX_189a	DIFFOUT_189a	G25	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_190a	DIFFOUT_190a	P21	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_RX_190a	DIFFOUT_190a	N22	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_TX_191a	DIFFOUT_191a	C30	DQ6T		DQ2T						
0B	VREFBAND	IO			DIFFIO_TX_191a	DIFFOUT_191a	C30	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_192a	DIFFOUT_192a	E28	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_192a	DIFFOUT_192a	D29	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_TX_193a	DIFFOUT_193a	G26	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_TX_193a	DIFFOUT_193a	G27	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_194a	DIFFOUT_194a	F30	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_194a	DIFFOUT_194a	E30	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_TX_195a	DIFFOUT_195a	G29	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_TX_195a	DIFFOUT_195a	G29	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_196a	DIFFOUT_196a	G30	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_196a	DIFFOUT_196a	G28	DQS8T/CQ8T/CQ8+T/DQ8+T	DQS8T/CQ2T/CQ2+T/DQ2+T							
0A	VREFBAND	IO			DIFFIO_RX_196a	DIFFOUT_196a	F28	DQS8+T/DQ8+T	DQS8+T/DQ8+T							
0A	VREFBAND	IO			DIFFIO_TX_197a	DIFFOUT_197a	H27	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_TX_197a	DIFFOUT_197a	H28	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_198a	DIFFOUT_198a	J30	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_198a	DIFFOUT_198a	H30	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_TX_199a	DIFFOUT_199a	K28	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_TX_199a	DIFFOUT_199a	L28	DQ6T		DQ2T						
0A	VREFBAND	IO			DIFFIO_RX_1100a	DIFFOUT_1100a	L30	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1100a	DIFFOUT_1100a	K30	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_TX_1101a	DIFFOUT_1101a	M27	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_TX_1101a	DIFFOUT_1101a	L27	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1102a	DIFFOUT_1102a	L26	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1102a	DIFFOUT_1102a	K29	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_TX_1103a	DIFFOUT_1103a	N30	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_TX_1103a	DIFFOUT_1103a	M30	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1104a	DIFFOUT_1104a	F24	DQS8T/CQ8T/CQ8+T/DQ8+T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1104a	DIFFOUT_1104a	F23	DQS8+T/DQ8+T		DQ3T						
0A	VREFBAND	IO			DIFFIO_TX_1105a	DIFFOUT_1105a	K26	DQ7T		DQ3T						
0A	VREFBAND	IO	CLK23a		DIFFIO_TX_1105a	DIFFOUT_1105a	K27	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1106a	DIFFOUT_1106a	P30	DQ7T		DQ3T						
0A	VREFBAND	IO	CLK33a		DIFFIO_RX_1106a	DIFFOUT_1106a	N29	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_TX_1107a	DIFFOUT_1107a	R22	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_TX_1107a	DIFFOUT_1107a	K23	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1108a	DIFFOUT_1108a	K28	DQ7T		DQ3T						
0A	VREFBAND	IO	CLK22a		DIFFIO_RX_1108a	DIFFOUT_1108a	P28	DQ7T		DQ3T						
0A	VREFBAND	IO		VREFBAND	DIFFIO_RX_1109a	DIFFOUT_1109a	J28	DQ7T		DQ3T						
0A	VREFBAND	IO		FP4L_TL_CLKOUT2_FPLL_TL_FB0_FPLL_TL_FB1	DIFFIO_RX_1109a	DIFFOUT_1109a	M28	DQ7T		DQ3T						
0A	VREFBAND	IO		FP4L_TL_CLKOUT3_FPLL_TL_FB0_FPLL_TL_FB1	DIFFIO_RX_1109a	DIFFOUT_1109a	M28	DQ7T		DQ3T						
0A	VREFBAND	IO		FP4L_TL_CLKOUT0_FPLL_TL_CLKOUT0_FPLL_TL_FB0	DIFFIO_TX_1110a	DIFFOUT_1110a	T25	DQ7T		DQ3T						
0A	VREFBAND	IO		FP4L_TL_CLKOUT0_FPLL_TL_CLKOUT0_FPLL_TL_FB0	DIFFIO_TX_1110a	DIFFOUT_1110a	T26	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1111a	DIFFOUT_1111a	R27	DQ7T		DQ3T						
0A	VREFBAND	IO	CLK21a		DIFFIO_RX_1111a	DIFFOUT_1111a	P27	DQ7T		DQ3T						
0A	VREFBAND	IO	CLK32a		DIFFIO_RX_1112a	DIFFOUT_1112a	P25	DQ7T		DQ3T						
0A	VREFBAND	IO			DIFFIO_RX_1113a	DIFFOUT_1113a	R25	DQ7T		DQ3T						
0A	VREFBAND	IO	RZD_6		DIFFIO_TX_1114a	DIFFOUT_1114a	J25	DQ7T		DQ3T						
0A	MSEL0		MSEL0				F24									
0A	MSEL1		MSEL1				K26									
0A	MSEL2		MSEL2				M25									
0A	MSEL3		MSEL3				L25									
0A	MSEL4		MSEL4				K20									
0A	CONF_DONE		CONF_DONE				N05									
0A	HSTATUS		HSTATUS				M26									
0A	HCE		HCE				M24									
0A	HCONFIG		HCONFIG				M23									
GND							T26									
U0C_HPS							W11									
GND							W10									
GND							AA24									
GND							AA29									
GND							AA30									
GND							AB22									
GND							AB23									
GND							AB24									
GND							AB25									
GND							AB26									
GND							AB27									
GND							AB28									
GND							AC26									
GND							AC29									
GND							AC30									
GND							AD27									
GND							AD28									
GND							AE26									
GND							AE29									
GND							AE30									
GND							AF27									
GND							AF28									
GND							AG26									
GND							AG29									
GND							AG30									
GND							AH27									
GND							AH28									
GND							AJ26									
GND							AJ30									
GND							R30									
GND							T27									
GND							T28									
GND							U22									
GND							U23									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	R896 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U24									
		GND					U25									
		GND					U26									
		GND					U29									
		GND					U30									
		GND					V23									
		GND					V27									
		GND					V28									
		GND					W24									
		GND					W29									
		GND					W35									
		GND					Y23									
		GND					Y25									
		GND					Y26									
		GND					Y27									
		GND					Y28									
		GND					AA1									
		GND					AA2									
		GND					AA7									
		GND					AB3									
		GND					AB4									
		GND					AB5									
		GND					AB6									
		GND					AC1									
		GND					AC2									
		GND					AC5									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE5									
		GND					AF3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG5									
		GND					AH3									
		GND					AH4									
		GND					AI1									
		GND					AJ2									
		GND					TI									
		GND					T4									
		GND					I1									
		GND					I2									
		GND					U5									
		GND					U6									
		GND					V3									
		GND					V4									
		GND					V8									
		GND					W1									
		GND					W2									
		GND					W5									
		GND					W7									
		GND					Y3									
		GND					Y4									
		GND					Y6									
		GND					Y8									
		VCCP					AB10									
		VCCP					AB14									
		VCCP					AB17									
		VCCP					AB20									
		VCCP					AC19									
		VCCP					P10									
		VCCP					RI7									
		VCCP					R21									
		VCCP					T10									
		VCCA_FPLL					V9									
		VCCA_FPLL					V22									
		VCCPLL_HPS					LI0									
		VCCBAT					H25									
		VCC_AUX					AB11									
		VCC_AUX					AB18									
		VCC_AUX					R20									
		VCC_AUX_SHARED					R13									
		VCCD_FPLL					V9									
		VCCD_FPLL					Y22									
		VCCA_GXBR0					W6									
		VCCA_GXBL1					W29									
		VCCD_GXBR0					V7									
		VCCD_GXBL1					V24									
		VCCD_GXBR0					V5									
		VCCD_GXBL1					V6									
		VCCD_GXBL1					V25									
		VCCD_GXBL1					V26									
		VCCR_GXBL					AA25									
		VCCR_GXBL					AA26									
		VCCR_GXBL					AA5									
		VCCR_GXBR					AA6									
		VCCD_GXBR0					V5									
		VCCD_GXBL1					V7									
		VCCD_GXBL1					W25									
		VCCD_GXBL1					V24									
		VCC					AA10									
		VCC					AA13									
		VCC					AA14									
		VCC					AA16									
		VCC					AA18									
		VCC					AA19									
		VCC					AA20									
		VCC					T17									
		VCC					T19									
		VCC					T21									
		VCC					T22									
		VCC					U16									
		VCC					U18									
		VCC					U20									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V21									
		VCC					W12									
		VCC					W14									
		VCC					W18									
		VCC					W20									
		VCC					Y11									
		VCC					Y13									
		VCC					Y15									



Bank Number	VREF	PinName/Function (3), (9)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	R966 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y21									
		VCC					W16									
		VCC_HPS					R12									
		VCC_HPS					T11									
		VCC_HPS					T13									
		VCC_HPS					U12									
		VCC_HPS					U13									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V13									
		VCCD0A					AE19									
		VCCD0A					AE22									
		VCCD0A					AF26									
		VCCD0A					AH19									
		VCCD0A					AH22									
		VCCD0A					AH26									
		VCCD0B					AE13									
		VCCD0B					AE16									
		VCCD0B					AH15									
		VCCD0B					AE11									
		VCCD0B					AC19									
		VCCD0A					AD5									
		VCCD0A					AE7									
		VCCD0A					AP5									
		VCCD0A					AM5									
		VCCD0A					AH7									
		VCCD0A_HPS					C2									
		VCCD0A_HPS					C5									
		VCCD0A_HPS					C8									
		VCCD0A_HPS					F2									
		VCCD0A_HPS					F4									
		VCCD0A_HPS					F6									
		VCCD0A_HPS					H1									
		VCCD0A_HPS					J5									
		VCCD0B_HPS					L4									
		VCCD0B_HPS					M4									
		VCCD0B_HPS					N1									
		VCCD0B_HPS					N6									
		VCCD0B_HPS					T2									
		VCCD0B_HPS					T5									
		VCCD0A_HPS					B14									
		VCCD0A_HPS					B17									
		VCCD0A_HPS					G10									
		VCCD0A_HPS					M10									
		VCCD0B_HPS					R20									
		VCCD0B_HPS					E12									
		VCCD0C_HPS					E14									
		VCCD0D_HPS					E18									
		VCCD0D_HPS					J14									
		VCCD0E_HPS					G15									
		VCCD0A					F29									
		VCCD0A					J27									
		VCCD0A					J29									
		VCCD0A					M29									
		VCCD0A					N24									
		VCCD0A					N27									
		VCCD0B					E27									
		VCCD0B					F25									
		VCCD0B					K23									
		VCCD0C					D25									
		VCCD0C					F29									
		VCCD0C					J1									
		VCCD0C					L19									
		VCCD0D					E21									
		VCCD0D					K17									
		VCCPD3					AB21									
		VCCPD3					AC18									
		VCCPD3					AC24									
		VCCPD4A					AB7									
		VCCPD6A6B_HPS					MB									
		VCCPD6A6B_HPS					MB									
		VCCPD6A6B_HPS					OB									
		VCCPD6A6B_HPS					UB									
		VCCPD7A_HPS					N11									
		VCCPD7B_HPS					L12									
		VCCPD7C_HPS					M13									
		VCCPD7D_HPS					M16									
		VCCPD7E_HPS					J15									
		VCCPD8					P18									
		VCCPD9					P22									
		VCCD9B					R19									
		VCCD9B					R24									
		VCCPGM					F12									
		VCCPGM					AD26									
		VCCRSTCLK_HPS					C9									
		VCC_HPS					R10									
		VCC_HPS					R11									
		VCC_HPS					R14									
		VCC_HPS					R15									
		VREFB7A/B/C/D/E/N0_HPS	VREFB7A/B/C/D/E/N0_HPS				F14									
		GND					AA41									
		GND					AA13									
		GND					AA15									
		GND					AA17									
		GND					AA21									
		GND					AB19									
		GND					AB9									
		GND					AB9									
		GND					AC11									
		GND					AC14									
		GND					AC17									
		GND					AC20									
		GND					AC23									
		GND					AD8									
		GND					AF1									
		GND					AF14									
		GND					AF17									
		GND					AF20									
		GND					AF23									
		GND					AF9									
		GND					AJ14									
		GND					AJ14									
		GND					AJ17									
		GND					AJ20									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	FB96 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					A123									
		GND					A126									
		GND					A15									
		GND					A16									
		GND					B1									
		GND					B2									
		GND					B23									
		GND					B26									
		GND					B29									
		GND					B5									
		GND					B8									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E5									
		GND					E8									
		GND					G12									
		GND					G14									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H5									
		GND					H8									
		GND					K11									
		GND					K14									
		GND					L17									
		GND					L2									
		GND					L20									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L5									
		GND					L8									
		GND					N10									
		GND					N14									
		GND					P11									
		GND					P17									
		GND					P16									
		GND					P2									
		GND					P20									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P5									
		GND					P8									
		GND					R18									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T20									
		GND					U11									
		GND					U15									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U7									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V18									
		GND					V20									
		GND					V14									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					X10									
		GND					Y12									
		GND					Y18									
		GND					Y20									

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).  
 (2) GAB, REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.  
 (3) Pins with \* contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.  
 (4) Pins with ~ are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).  
 (5) RESET pin is only applicable for DDR3 device.





Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					E33									
		DNU					F33									
		RREF_IL					F34									
		GND					R27									
		GND					R28									
		DNU					G31									
		DNU					G32									
		GND					H34									
		GND					H33									
		DNU					L31									
		DNU					J32									
		GND					K34									
		GND					K33									
		DNU					L31									
		DNU					L32									
		GND					M34									
		GND					M33									
		GXB TX L8n					N31									
		GXB TX L8p					N32									
		GXB RX L8p_GXB_REFCLK_L8p					P34									
		GXB RX L8n_GXB_REFCLK_L8n					P33									
		GXB TX L7n					R31									
		GXB TX L7p					R32									
		GXB RX L7p_GXB_REFCLK_L7p					T34									
		GXB RX L7n_GXB_REFCLK_L7n					T33									
		GXB TX L6n					U31									
		GXB TX L6p					U32									
		GXB RX L6p_GXB_REFCLK_L6p					V34									
		GXB RX L6n_GXB_REFCLK_L6n					V33									
		REFCLK0Lp					W27									
		REFCLK0Lp					W26									
		REFCLK0Lp					W27									
		REFCLK0Lp					W26									
		GXB TX L5n					W31									
		GXB TX L5p					W32									
		GXB RX L5p_GXB_REFCLK_L5p					Y34									
		GXB RX L5n_GXB_REFCLK_L5n					Y33									
		GXB TX L4n					AA31									
		GXB TX L4p					AA32									
		GXB RX L4p_GXB_REFCLK_L4p					AB34									
		GXB RX L4n_GXB_REFCLK_L4n					AB33									
		GXB TX L3n					AC31									
		GXB TX L3p					AC32									
		GXB RX L3p_GXB_REFCLK_L3p					AD34									
		GXB RX L3n_GXB_REFCLK_L3n					AD33									
		GXB TX L2n					AE31									
		GXB TX L2p					AE32									
		GXB RX L2p_GXB_REFCLK_L2p					AF34									
		GXB RX L2n_GXB_REFCLK_L2n					AF33									
		GXB TX L1n					AG31									
		GXB TX L1p					AG32									
		GXB RX L1p_GXB_REFCLK_L1p					AH34									
		GXB RX L1n_GXB_REFCLK_L1n					AH33									
		GXB TX L0n					AJ31									
		GXB TX L0p					AJ32									
		GXB RX L0p_GXB_REFCLK_L0p					AK34									
		GXB RX L0n_GXB_REFCLK_L0n					AK33									
		REFCLK0Ln					AA38									
		REFCLK0Lp					AA27									
		DNU					AL32									
		TDO		TDO			AM33									
		TMS		TMS			AD30									
		TDK		TDK			AM34									
		TDI		TDI			AN34									
		DCCLK		DCCLK			AP33									
		ASDO		ASDO			AC06									
		AS_DATA3		AS_DATA3			AL31									
		AS_DATA2		AS_DATA2			AM32									
		AS_DATA1		AS_DATA1			AN33									
		AS_DATA0_ASDO		AS_DATA0			AL30									
	VREFB3A0	I0	RZ0_0		DIFF0_TX_B1n	DIFF0UT_B1n	AM30									
	VREFB3A0	I0	CLK0n		DIFF0_RX_B2n	DIFF0UT_B2n	AP29									
	VREFB3A0	I0	CLK0p		DIFF0_TX_B2p	DIFF0UT_B2p	AG29									
	VREFB3A0	I0	CLK1n		DIFF0_RX_B4n	DIFF0UT_B4n	AH29									
	VREFB3A0	I0	CLK1p		DIFF0_TX_B4p	DIFF0UT_B4p	AH28									
	VREFB3A0	I0	FPLL_B1_CLKOUT1_FPLL_B1_CLKOUTn		DIFF0_TX_B5n	DIFF0UT_B5n	AJ29									
	VREFB3A0	I0	FPLL_B1_CLKOUT0_FPLL_B1_CLKOUTp		DIFF0_TX_B5p	DIFF0UT_B5p	AK29									
	VREFB3A0	I0	FPLL_B1_CLKOUT3_FPLL_B1_FBI		DIFF0_RX_B6n	DIFF0UT_B6n	AM31									
	VREFB3A0	I0	FPLL_B1_CLKOUT2_FPLL_B1_FBI		DIFF0_RX_B6p	DIFF0UT_B6p	AN32									
	VREFB3A0	I0	VREFB3A0		DIFF0_RX_B6p	DIFF0UT_B6p	AC27									
	VREFB3A0	I0	CLK2n		DIFF0_RX_B7n	DIFF0UT_B7n	AG27									
	VREFB3A0	I0	CLK2p		DIFF0_TX_B7p	DIFF0UT_B7p	AH27									
	VREFB3A0	I0			DIFF0_TX_B8n	DIFF0UT_B8n	AP32									
	VREFB3A0	I0			DIFF0_TX_B8p	DIFF0UT_B8p	AP31	DQ1B								
	VREFB3A0	I0	CLK3n		DIFF0_RX_B9n	DIFF0UT_B9n	AG26	DQ1B								
	VREFB3A0	I0	CLK3p		DIFF0_RX_B9p	DIFF0UT_B9p	AH26	DQ1B								
	VREFB3A0	I0			DIFF0_TX_B10n	DIFF0UT_B10n	AE26									
	VREFB3A0	I0			DIFF0_TX_B10p	DIFF0UT_B10p	AF26	DQ1B								
	VREFB3A0	I0			DIFF0_RX_B11n	DIFF0UT_B11n	AL29	DQS1B/CQ1B								
	VREFB3A0	I0			DIFF0_RX_B11p	DIFF0UT_B11p	AL28	DQS1B/CQ1B/CQn1B/CQn1B								
	VREFB3A0	I0			DIFF0_TX_B12n	DIFF0UT_B12n	AN30									
	VREFB3A0	I0			DIFF0_TX_B12p	DIFF0UT_B12p	AP30	DQ1B								
	VREFB3A0	I0			DIFF0_RX_B13n	DIFF0UT_B13n	AM28	DQ1B								
	VREFB3A0	I0			DIFF0_RX_B13p	DIFF0UT_B13p	AM29	DQ1B								
	VREFB3A0	I0			DIFF0_TX_B14n	DIFF0UT_B14n	AD27									
	VREFB3A0	I0			DIFF0_TX_B14p	DIFF0UT_B14p	AE27	DQ1B								
	VREFB3A0	I0			DIFF0_RX_B15n	DIFF0UT_B15n	AJ27	DQ1B								
	VREFB3A0	I0			DIFF0_RX_B15p	DIFF0UT_B15p	AK27	DQ1B								
	VREFB3A0	I0			DIFF0_TX_B16n	DIFF0UT_B16n	AP29									
	VREFB3A0	I0			DIFF0_TX_B16p	DIFF0UT_B16p	AP28	DQ2B								
	VREFB3A0	I0			DIFF0_RX_B17n	DIFF0UT_B17n	AL27	DQ2B								
	VREFB3A0	I0			DIFF0_RX_B17p	DIFF0UT_B17p	AM27	DQ2B								
	VREFB3A0	I0			DIFF0_TX_B18n	DIFF0UT_B18n	AE28									
	VREFB3A0	I0			DIFF0_TX_B18p	DIFF0UT_B18p	AF28	DQ2B								
	VREFB3A0	I0			DIFF0_RX_B19n	DIFF0UT_B19n	AL26	DQS2B/CQ2B								
	VREFB3A0	I0			DIFF0_RX_B19p	DIFF0UT_B19p	AK26	DQS2B/CQ2B/CQn2B/CQn2B								
	VREFB3A0	I0			DIFF0_TX_B20n	DIFF0UT_B20n	AN27									
	VREFB3A0	I0			DIFF0_TX_B20p	DIFF0UT_B20p	AP27	DQ2B								
	VREFB3A0	I0			DIFF0_RX_B21n	DIFF0UT_B21n	AL26	DQ2B								
	VREFB3A0	I0			DIFF0_RX_B21p	DIFF0UT_B21p	AM26	DQ2B								
	VREFB3A0	I0			DIFF0_TX_B22n	DIFF0UT_B22n	AD29									
	VREFB3A0	I0			DIFF0_TX_B22p	DIFF0UT_B22p	AE29	DQ2B								
	VREFB3A0	I0			DIFF0_RX_B23n	DIFF0UT_B23n	AN26	DQ2B								
	VREFB3A0	I0			DIFF0_RX_B23p	DIFF0UT_B23p	AP26	DQ2B								
	VREFB3A0	I0			DIFF0_TX_B24n	DIFF0UT_B24n	AD26									
	VREFB3A0	I0			DIFF0_TX_B24p	DIFF0UT_B24p	AE26	DQ2B	DQ1B							
	VREFB3A0	I0			DIFF0_RX_B25n	DIFF0UT_B25n	AL24	DQ2B	DQ1B							
	VREFB3A0	I0			DIFF0_RX_B25p	DIFF0UT_B25p	AF24	DQ2B	DQ1B							
	VREFB3A0	I0			DIFF0_TX_B26n	DIFF0UT_B26n	AB24									
	VREFB3A0	I0			DIFF0_TX_B26p	DIFF0UT_B26p	AB25	DQ3B	DQ2B	DQ1B						



Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	QDS for X8/X9	QDS for X16/X18	QDS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0		
3B	VREFB38N0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AC24	DQS#3B/QK3B	DQ2B	DQ1B								
3B	VREFB38N0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AD24	DQS#3B/CQ#3B/QK#3B	DQ2B	DQ1B								
3B	VREFB38N0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AK25											
3B	VREFB38N0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AJ25	DQ3B	DQ2B	DQ1B								
3B	VREFB38N0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AM24	DQ3B	DQ2B	DQ1B								
3B	VREFB38N0	IO	VREFB38N0		DIFFIO_RX_B29p	DIFFOUT_B29p	AH24	DQ3B	DQ2B	DQ1B								
3B	VREFB38N0	IO					AC25											
3B	VREFB38N0	IO					AC23	DQ3B	DQ2B	DQ1B								
3B	VREFB38N0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AL25	DQ3B	DQ2B	DQ1B								
3B	VREFB38N0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AL24	DQ3B	DQ2B	DQ1B								
3B	VREFB38N0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AJ24	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AE23	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AF23	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AD23	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AP25	DQS#4B/QK4B	DQS#2B/QK2B	DQ1B								
3B	VREFB38N0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AP24	DQS#4B/CQ#4B/QK#4B	DQS#2B/CQ#2B/QK#2B	DQ1B								
3B	VREFB38N0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AM25	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AM23	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AM24	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AB23	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AN23	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AP23	DQ4B	DQ3B	DQ2B								
3B	VREFB38N0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AF25	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AS23	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AH23	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AE22	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AJ23	DQS#6B/QK5B	DQS#4B/QK3B	DQ2B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AJ22	DQS#6B/CQ#6B/QK#6B	DQS#4B/CQ#4B/QK#4B	DQ1B								
3C	VREFB3C0N0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AK22	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AG21	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AG21	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AK22	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AK23	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AK23	DQ5B	DQ4B	DQ3B								
3C	VREFB3C0N0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AM22	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AN21	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AN22	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB21	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AE21	DQS#8B/QK7B	DQS#6B/QK5B	DQ1B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AE20	DQS#8B/CQ#8B/QK#8B	DQS#6B/CQ#6B/QK#6B	DQ0B								
3C	VREFB3C0N0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AL20	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AF20	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AF20	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO	VREFB3C0N0				AB22											
3C	VREFB3C0N0	IO			DIFFIO_RX_B53n	DIFFOUT_B53n	AB20	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B53p	DIFFOUT_B53p	AL21	DQ6B	DQ5B	DQ4B								
3C	VREFB3C0N0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AH20	DQ7B	DQ6B	DQ5B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AJ20	DQ7B	DQ6B	DQ5B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AK20	DQ7B	DQ6B	DQ5B								
3C	VREFB3C0N0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AC21	DQ7B	DQ6B	DQ5B								
3C	VREFB3C0N0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AP21	DQS#7B/QK7B										
3C	VREFB3C0N0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AP20	DQS#7B/CQ#7B/QK#7B										
3C	VREFB3C0N0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AM20	DQ7B										
3C	VREFB3C0N0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AN20	DQ7B										
3C	VREFB3C0N0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AP19	DQ7B										
3C	VREFB3C0N0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AC19	DQ7B										
3C	VREFB3C0N0	IO			DIFFIO_RX_B61n	DIFFOUT_B61n	AC20	DQ7B										
3C	VREFB3C0N0	IO			DIFFIO_RX_B61p	DIFFOUT_B61p	AD20	DQ7B										
3D	VREFB3D0N0	IO	VREFB3D0N0				AD18											
3D	VREFB3D0N0	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AH19											
3D	VREFB3D0N0	IO	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AJ19											
3D	VREFB3D0N0	IO	CLK5n		DIFFIO_RX_B78n	DIFFOUT_B78n	AL19											
3D	VREFB3D0N0	IO	CLK5p		DIFFIO_RX_B78p	DIFFOUT_B78p	AM19											
3D	VREFB3D0N0	IO	FPLL_BC_CLKOUT1/FPLL_BC_CLKOUT1n		DIFFIO_TX_B79n	DIFFOUT_B79n	AE19											
3D	VREFB3D0N0	IO	FPLL_BC_CLKOUT2/FPLL_BC_CLKOUT2n		DIFFIO_TX_B79p	DIFFOUT_B79p	AF19											
3D	VREFB3D0N0	IO	FPLL_BC_CLKOUT3/FPLL_BC_CLKOUT3n		DIFFIO_RX_B80n	DIFFOUT_B80n	AM18											
3D	VREFB3D0N0	IO	FPLL_BC_CLKOUT4/FPLL_BC_CLKOUT4n		DIFFIO_RX_B80p	DIFFOUT_B80p	AN18											
3D	VREFB3D0N0	IO	CLK6n		DIFFIO_RX_B82n	DIFFOUT_B82n	AJ18											
3D	VREFB3D0N0	IO	CLK6p		DIFFIO_RX_B82p	DIFFOUT_B82p	AK18											
3D	VREFB3D0N0	IO	CLK7n		DIFFIO_RX_B84n	DIFFOUT_B84n	AF18											
3D	VREFB3D0N0	IO	CLK7p		DIFFIO_RX_B84p	DIFFOUT_B84p	AG18											
3E	VREFB3E0N0	IO	VCCD_FPLL				AA17											
3E	VREFB3E0N0	IO	VCCA_FPLL				AA18											
3E	VREFB3E0N0	IO	DN1				AB19											
4D	VREFB4D0N0	IO			DIFFIO_TX_B99n	DIFFOUT_B99n	AD17											
4D	VREFB4D0N0	IO			DIFFIO_TX_B99p	DIFFOUT_B99p	AE17	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AE16	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AF16	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AB18											
4D	VREFB4D0N0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AC18	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AF17	DQS#8B/QK8B	DQS#6B/QK6B	DQ4B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B98p	DIFFOUT_B98p	AG17	DQS#8B/CQ#8B/QK#8B	DQS#6B/CQ#6B/QK#6B	DQ3B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	AH16	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AJ16	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AJ17	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO	VREFB4D0N0				AB17											
4D	VREFB4D0N0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AC17	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AK17	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B100n	DIFFOUT_B100n	AL17	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	AM17	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B101n	DIFFOUT_B101n	AP17	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B101p	DIFFOUT_B101p	AP18	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B102n	DIFFOUT_B102n	AB16	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B102p	DIFFOUT_B102p	AC16	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B103n	DIFFOUT_B103n	AP16	DQS#8B/QK8B	DQS#6B/QK6B	DQ4B								
4D	VREFB4D0N0	IO			DIFFIO_RX_B103p	DIFFOUT_B103p	AP15	DQS#8B/CQ#8B/QK#8B	DQS#6B/CQ#6B/QK#6B	DQ3B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AG15	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AH15	DQ8B	DQ7B	DQ6B								
4D	VREFB4D0N0	IO			DIFFIO													





Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					Y1									
		DNU					W3									
		DNU					W4									
		GND					W6									
		GND					W7									
06	VREFB6N0	HPS	HPS_DDR				T7				HPS_DM_4	HPS_DM_4				
06	VREFB6N0	HPS	HPS_DDR				T8				HPS_DO_29	HPS_DO_29				
06	VREFB6N0	HPS	HPS_DDR				U2				HPS_DO_37	HPS_DO_37				
06	VREFB6N0	HPS	HPS_DDR				V1				HPS_DO_38	HPS_DO_38				
06	VREFB6N0	HPS	HPS_DDR				U3				HPS_DO_36	HPS_DO_36				
06	VREFB6N0	HPS	HPS_DDR				T3				HPS_DQS_4	HPS_DQS_4				
06	VREFB6N0	HPS	HPS_GP13				T1									
06	VREFB6N0	HPS	HPS_DDR				T4				HPS_DQS#_4	HPS_DQS#_4				
06	VREFB6N0	HPS	HPS_DDR				U1				HPS_DO_35	HPS_DO_35				
06	VREFB6N0	HPS	HPS_DDR				R1				HPS_DO_33	HPS_DO_33				
06	VREFB6N0	HPS	HPS_DDR				T6				HPS_DO_34	HPS_DO_34				
06	VREFB6N0	HPS	HPS_DDR				R2				HPS_DO_32	HPS_DO_32				
06	VREFB6N0	HPS	HPS_GP12				T6									
06	VREFB6N0	HPS	HPS_GP11				P1									
06	VREFB6N0	HPS	HPS_DDR				P2				HPS_DM_3	HPS_DM_3				
06	VREFB6N0	HPS	HPS_GP10				N1									
06	VREFB6N0	HPS	HPS_DDR				R3				HPS_DO_31	HPS_DO_31				
06	VREFB6N0	HPS	HPS_DDR				N4				HPS_DO_29	HPS_DO_29				
06	VREFB6N0	HPS	HPS_DDR				P7				HPS_DO_30	HPS_DO_30				
06	VREFB6N0	HPS	HPS_DDR				P4				HPS_DO_28	HPS_DO_28				
06	VREFB6N0	HPS	VREFB6N0_HPS				R7									
06	VREFB6N0	HPS	HPS_DDR				L1				HPS_DQS_3	HPS_DQS_3				
06	VREFB6N0	HPS	HPS_GP9				M3									
06	VREFB6N0	HPS	HPS_DDR				M2				HPS_DQS#_3	HPS_DQS#_3				
06	VREFB6N0	HPS	HPS_DDR				N3				HPS_DO_27	HPS_DO_27				
06	VREFB6N0	HPS	HPS_DDR				K1				HPS_DO_25	HPS_DO_25				
06	VREFB6N0	HPS	HPS_DDR				R4				HPS_DO_26	HPS_DO_26				
06	VREFB6N0	HPS	HPS_DDR				L2				HPS_DO_24	HPS_DO_24				
06	VREFB6N0	HPS	HPS_GP8				P5									
06	VREFB6N0	HPS	HPS_GP7				H2									
06	VREFB6N0	HPS	HPS_DDR				H1				HPS_DM_2	HPS_DM_2				
06	VREFB6N0	HPS	HPS_GP6				J2									
06	VREFB6N0	HPS	HPS_DDR				J1				HPS_DO_23	HPS_DO_23				
06	VREFB6N0	HPS	HPS_DDR				J3				HPS_DO_21	HPS_DO_21				
06	VREFB6N0	HPS	HPS_DDR				N5				HPS_DO_22	HPS_DO_22				
06	VREFB6N0	HPS	HPS_DDR				K3				HPS_DO_20	HPS_DO_20				
06	VREFB6N0	HPS	HPS_GP5				P6									
06	VREFB6N0	HPS	HPS_DDR				K4				HPS_DQS_2	HPS_DQS_2				
06	VREFB6N0	HPS	HPS_DDR				L3				HPS_DQS#_2	HPS_DQS#_2				
06	VREFB6N0	HPS	HPS_DDR				L5				HPS_DQS#_2	HPS_DQS#_2				
06	VREFB6N0	HPS	HPS_DDR				M4				HPS_DO_19	HPS_DO_19				
06	VREFB6N0	HPS	HPS_DDR				L6				HPS_DO_17	HPS_DO_17				
06	VREFB6N0	HPS	HPS_DDR				N6				HPS_DO_18	HPS_DO_18				
06	VREFB6N0	HPS	HPS_DDR				M6				HPS_DO_16	HPS_DO_16				
06	VREFB6N0	HPS	HPS_GP4				N7									
06	VREFB6N0	HPS	HPS_GP3				G3									
06	VREFB6N0	HPS	HPS_DDR				F1				HPS_DM_1	HPS_DM_1				
06	VREFB6N0	HPS	HPS_GP2				H3									
06	VREFB6N0	HPS	HPS_DDR				G1				HPS_DO_15	HPS_DO_15				
06	VREFB6N0	HPS	HPS_DDR				H4				HPS_DO_13	HPS_DO_13				
06	VREFB6N0	HPS	HPS_DDR				K5				HPS_DO_14	HPS_DO_14				
06	VREFB6N0	HPS	HPS_DDR				J4				HPS_DO_12	HPS_DO_12				
06	VREFB6N0	HPS	HPS_DDR				K6				HPS_CKE_0	HPS_CKE_0				
06	VREFB6N0	HPS	HPS_DDR				D1				HPS_DQS_1	HPS_DQS_1				
06	VREFB6N0	HPS	HPS_DDR				E1				HPS_CKE_1	HPS_CKE_1				
06	VREFB6N0	HPS	HPS_DDR				C1				HPS_DQS#_1	HPS_DQS#_1				
06	VREFB6N0	HPS	HPS_DDR				E2				HPS_DO_11	HPS_DO_11				
06	VREFB6N0	HPS	HPS_DDR				F3				HPS_DO_9	HPS_DO_9				
06	VREFB6N0	HPS	HPS_DDR				J6				HPS_DO_10	HPS_DO_10				
06	VREFB6N0	HPS	HPS_DDR				F4				HPS_DO_8	HPS_DO_8				
06	VREFB6N0	HPS	HPS_GP1				J7									
06	VREFB6N0	HPS	HPS_GP0				C2									
06	VREFB6N0	HPS	HPS_DDR				G4				HPS_DM_0	HPS_DM_0				
06	VREFB6N0	HPS	HPS_DDR				G6				HPS_DO_7	HPS_DO_7				
06	VREFB6N0	HPS	HPS_DDR				A2				HPS_DO_5	HPS_DO_5				
06	VREFB6N0	HPS	HPS_DDR				K7				HPS_DO_6	HPS_DO_6				
06	VREFB6N0	HPS	HPS_DDR				B1				HPS_DO_4	HPS_DO_4				
06	VREFB6N0	HPS	HPS_DDR				L7				HPS_ODT_1	HPS_ODT_1				
06	VREFB6N0	HPS	HPS_DDR				C3				HPS_DQS_0	HPS_DQS_0				
06	VREFB6N0	HPS	HPS_DDR				E3				HPS_ODT_0	HPS_ODT_0				
06	VREFB6N0	HPS	HPS_DDR				D4				HPS_DQS#_0	HPS_DQS#_0				
06	VREFB6N0	HPS	HPS_DDR				E4				HPS_DO_3	HPS_DO_3				
06	VREFB6N0	HPS	HPS_DDR				A4				HPS_DO_1	HPS_DO_1				
06	VREFB6N0	HPS	HPS_DDR				M8				HPS_DO_2	HPS_DO_2				
06	VREFB6N0	HPS	HPS_DDR				A3				HPS_DO_0	HPS_DO_0				
06	VREFB6N0	HPS	VREFB6N0_HPS				N9									
06	VREFB6N0	HPS	HPS_DDR				B4				HPS_A_0	HPS_CA_0				
06	VREFB6N0	HPS	HPS_DDR				C4				HPS_A_1	HPS_CA_1				
06	VREFB6N0	HPS	HPS_DDR				D5				HPS_A_4	HPS_CA_4				
06	VREFB6N0	HPS	HPS_DDR				J8				HPS_A_2	HPS_CA_2				
06	VREFB6N0	HPS	HPS_DDR				E5				HPS_A_5	HPS_CA_5				
06	VREFB6N0	HPS	HPS_DDR				K8				HPS_A_3	HPS_CA_3				
06	VREFB6N0	HPS	HPS_DDR				A6				HPS_CK#	HPS_CK#				
06	VREFB6N0	HPS	HPS_DDR				B5				HPS_A_6	HPS_CA_6				
06	VREFB6N0	HPS	HPS_DDR				B7				HPS_CK#	HPS_CK#				
06	VREFB6N0	HPS	HPS_DDR				B6				HPS_A_7	HPS_CA_7				
06	VREFB6N0	HPS	HPS_DDR				C7				HPS_BA_1					
06	VREFB6N0	HPS	HPS_DDR				G7				HPS_BA_0					
06	VREFB6N0	HPS	HPS_DDR				D6				HPS_BA_3					
06	VREFB6N0	HPS	HPS_DDR				G6				HPS_CAS#					
06	VREFB6N0	HPS	HPS_DDR				H6				HPS_RAS#					
06	VREFB6N0	HPS	HPS_DDR				F5				HPS_A_9					
06	VREFB6N0	HPS	HPS_DDR				G8				HPS_A_10					
06	VREFB6N0	HPS	HPS_DDR				F7				HPS_A_8	HPS_CA_8				
06	VREFB6N0	HPS	HPS_DDR				G9				HPS_A_11					
06	VREFB6N0	HPS	HPS_DDR				C8				HPS_CSA_0					
06	VREFB6N0	HPS	HPS_DDR				E7				HPS_A_12					
06	VREFB6N0	HPS	HPS_DDR				D7				HPS_CSA_1	HPS_CSA_1				
06	VREFB6N0	HPS	HPS_DDR				F9				HPS_A_13					
06	VREFB6N0	HPS	HPS_DDR				A8				HPS_A_14					
06	VREFB6N0	HPS	HPS_DDR				J9				HPS_WB#					
06	VREFB6N0	HPS	HPS_DDR				A7				HPS_A_15					
06	VREFB6N0	HPS	HPS_R20_0				K9									
		DNU					U4									
		GND					G10									
		GND					H10									
7A		HPS_ARST					P11									
7A		HPS_APC#					E9									
7A		HPS_TD0					P10									
7A		VCCRCSTCLK_HPS					E9									
7A		HPS_TCK					C9									
7A		HPS_TRST					B10									
7A		HPS_TDI					D9									
		GND					N10									



Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7A		HPS_PORSEL					C10									
7A		HPS_CLKI					L9									
7A		HPS_CLKO					D10									
7A	VREFB7A/B7C/D7END	HPS_TRACE_CLK					A10						TRACE_CLK			HPS GPIO48
7A	VREFB7A/B7C/D7END	HPS_TRACE_D0					K10						TRACE_D0	SPIS0_CLK	UART0_RX	HPS GPIO49
7A	VREFB7A/B7C/D7END	HPS_TRACE_D1					A11						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS GPIO50
7A	VREFB7A/B7C/D7END	HPS_TRACE_D2					I10						TRACE_D2	SPIS0_MISO	IC21_SDA	HPS GPIO51
7A	VREFB7A/B7C/D7END	HPS_TRACE_D3					A13						TRACE_D3	SPIS0_SS0	IC21_SCL	HPS GPIO52
7A	VREFB7A/B7C/D7END	HPS_TRACE_D4					B12						TRACE_D4	SPIS1_CLK		HPS GPIO53
7A	VREFB7A/B7C/D7END	HPS_TRACE_D5					A12						TRACE_D5	SPIS1_MOSI		HPS GPIO54
7A	VREFB7A/B7C/D7END	HPS_TRACE_D6					C13						TRACE_D6	SPIS1_SS0	IC20_SDA	HPS GPIO55
7A	VREFB7A/B7C/D7END	HPS_TRACE_D7					C11						TRACE_D7	SPIS1_MISO	IC20_SCL	HPS GPIO56
7A	VREFB7A/B7C/D7END	HPS_SPIM0_CLK					L10						SPIM0_CLK	IC21_SCL	UART0_CTS	HPS GPIO57
7A	VREFB7A/B7C/D7END	HPS_SPIM0_MOSI					C12						SPIM0_MOSI	IC21_SCL	UART0_RTS	HPS GPIO58
7A	VREFB7A/B7C/D7END	HPS_SPIM0_MISO					L11						SPIM0_MISO		UART1_CTS	HPS GPIO59
7A	VREFB7A/B7C/D7END	HPS_SPIM0_SS0/BOOTSEL0					E10						SPIM0_SS0		UART1_RTS	HPS GPIO60
7A	VREFB7A/B7C/D7END	HPS_UART0_RX					E11						UART0_RX	SPIM0_SS1		HPS GPIO61
7A	VREFB7A/B7C/D7END	HPS_UART0_TX_CLKSEL1					F10						UART0_TX	SPIM0_SS1		HPS GPIO62
7A	VREFB7A/B7C/D7END	HPS_IC21_SDA					F11						IC21_SDA	UART1_RX	SPIM1_CLK	HPS GPIO63
7A	VREFB7A/B7C/D7END	HPS_IC21_SCL					H11						IC21_SCL	UART1_TX	SPIM1_MOSI	HPS GPIO64
7A	VREFB7A/B7C/D7END	HPS_UART0_RX*					M10						UART0_RX	SPIM1_MISO		HPS GPIO65
7A	VREFB7A/B7C/D7END	HPS_UART0_TX_CLKSEL0					J11						UART0_TX	SPIM1_SS0		HPS GPIO66
7A	VREFB7A/B7C/D7END	HPS_SPIS1_CLK					M11						SPIS1_CLK	SPIM1_CLK		HPS GPIO67
7A	VREFB7A/B7C/D7END	HPS_SPIS1_MOSI					D12						SPIS1_MOSI	SPIM1_MOSI		HPS GPIO68
7A	VREFB7A/B7C/D7END	HPS_SPIS1_MISO					E12						SPIS1_MISO	SPIM1_MISO		HPS GPIO69
7A	VREFB7A/B7C/D7END	HPS_SPIS1_SS0					D13						SPIS1_SS0	SPIS1_SS0		HPS GPIO70
7A	VREFB7A/B7C/D7END	HPS_UART1_RX					F12						UART1_RX	SPIM1_SS1		HPS GPIO72
7A	VREFB7A/B7C/D7END	HPS_UART1_TX					J12						UART1_TX	SPIM0_CLK		HPS GPIO73
7A	VREFB7A/B7C/D7END	HPS_IC21_SDA					L12						IC21_SDA	SPIM0_MOSI		HPS GPIO74
7A	VREFB7A/B7C/D7END	HPS_IC21_SCL					K12						IC21_SCL	SPIM0_MISO		HPS GPIO75
7A	VREFB7A/B7C/D7END	HPS_SPIM0_SS0					M12						SPIM0_SS0			HPS GPIO76
7A	VREFB7A/B7C/D7END	HPS_SPIS0_CLK					F13						SPIS0_CLK	SPIM0_SS1		HPS GPIO77
7A	VREFB7A/B7C/D7END	HPS_SPIS0_MOSI					G12						SPIS0_MOSI			HPS GPIO78
7A	VREFB7A/B7C/D7END	HPS_SPIS0_MISO					G13						SPIS0_MISO			HPS GPIO79
7A	VREFB7A/B7C/D7END	HPS_SPIS0_SS0					H12						SPIS0_SS0			HPS GPIO80
7B	VREFB7A/B7C/D7END	HPS_NAND_ALE					A14						NAND_ALE	RGMIH_TX_CLK	QSPI_SS3	HPS GPIO14
7B	VREFB7A/B7C/D7END	HPS_NAND_CE					M13						NAND_CE	RGMIH_TXD0	USB1_D0	HPS GPIO15
7B	VREFB7A/B7C/D7END	HPS_NAND_CLE					B14						NAND_CLE	RGMIH_TXD1	USB1_D1	HPS GPIO16
7B	VREFB7A/B7C/D7END	HPS_NAND_BE					N13						NAND_BE	RGMIH_TXD2	USB1_D2	HPS GPIO17
7B	VREFB7A/B7C/D7END	HPS_NAND_RB					B15						NAND_RB	RGMIH_TXD3	USB1_D3	HPS GPIO18
7B	VREFB7A/B7C/D7END	HPS_NAND_DQ0					C14						NAND_DQ0	RGMIH_RXD0		HPS GPIO19
7B	VREFB7A/B7C/D7END	HPS_NAND_DQ1					C15						NAND_DQ1	RGMIH_MIO0	IC23_SDA	HPS GPIO20
7B	VREFB7A/B7C/D7END	HPS_NAND_DQ2					D14						NAND_DQ2	RGMIH_MIO1	IC23_SCL	HPS GPIO21
7B	VREFB7A/B7C/D7END	HPS_NAND_DQ3					O14						NAND_DQ3	RGMIH_RX_CTL	USB1_D4	HPS GPIO22
7B	VREFB7A/B7C/D7END	HPS_NAND_DQ4					N12						NAND_DQ4	RGMIH_TX_CTL	USB1_D5	HPS GPIO23
7B	VREFB7A/B7C/D7END	HPS_NAND_DQ5					H14						NAND_DQ5	RGMIH_RX_CLK	USB1_D6	HPS GPIO24
7B	VREFB7A/B7C/D7END	HPS_NAND_DQ6					P12						NAND_DQ6	RGMIH_RXD1	USB1_D7	HPS GPIO25
7B	VREFB7A/B7C/D7END	HPS_NAND_DQ7					K13						NAND_DQ7	RGMIH_RXD2		HPS GPIO26
7B	VREFB7A/B7C/D7END	HPS_NAND_WP					J14						NAND_WP	RGMIH_RXD3	QSPI_SS2	HPS GPIO27
7B	VREFB7A/B7C/D7END	HPS_NAND_WI/BOOTSEL2					L14						NAND_WI	QSPI_SS1		HPS GPIO28
7B	VREFB7A/B7C/D7END	HPS_QSPI_I00					K14						QSPI_I00	USB1_CLK		HPS GPIO29
7B	VREFB7A/B7C/D7END	HPS_QSPI_I01					M14						QSPI_I01	USB1_STP		HPS GPIO30
7B	VREFB7A/B7C/D7END	HPS_QSPI_I02					P14						QSPI_I02	USB1_DRP		HPS GPIO31
7B	VREFB7A/B7C/D7END	HPS_QSPI_I03					N14						QSPI_I03	USB1_NXT		HPS GPIO32
7B	VREFB7A/B7C/D7END	HPS_QSPI_SS0/BOOTSEL1					R15						QSPI_SS0			HPS GPIO33
7B	VREFB7A/B7C/D7END	HPS_QSPI_CLK					F14						QSPI_CLK			HPS GPIO34
7B	VREFB7A/B7C/D7END	HPS_QSPI_SS1					D15						QSPI_SS1			HPS GPIO35
7C	VREFB7A/B7C/D7END	HPS_SDMMC_CMD					E15						SDMMC_CMD	USB0_D0		HPS GPIO36
7C	VREFB7A/B7C/D7END	HPS_SDMMC_PWREN					J15						SDMMC_PWREN	USB0_D1		HPS GPIO37
7C	VREFB7A/B7C/D7END	HPS_SDMMC_D0					C16						SDMMC_D0	USB0_D2		HPS GPIO38
7C	VREFB7A/B7C/D7END	HPS_SDMMC_D1					K15						SDMMC_D1	USB0_D3		HPS GPIO39
7C	VREFB7A/B7C/D7END	HPS_SDMMC_D4					E16						SDMMC_D4	USB0_D4		HPS GPIO40
7C	VREFB7A/B7C/D7END	HPS_SDMMC_D5					G15						SDMMC_D5	USB0_D5		HPS GPIO41
7C	VREFB7A/B7C/D7END	HPS_SDMMC_D6					F16						SDMMC_D6	USB0_D6		HPS GPIO42
7C	VREFB7A/B7C/D7END	HPS_SDMMC_D7					G16						SDMMC_D7	USB0_D7		HPS GPIO43
7C	VREFB7A/B7C/D7END	HPS_HPS_GPIO44					H16						SDMMC_CLK	USB0_CLK		HPS GPIO44
7C	VREFB7A/B7C/D7END	HPS_SDMMC_CCLK_OUT					M15						SDMMC_CCLK_OUT	USB0_STP		HPS GPIO45
7C	VREFB7A/B7C/D7END	HPS_SDMMC_D2					L16						SDMMC_D2	USB0_DIR		HPS GPIO46
7C	VREFB7A/B7C/D7END	HPS_SDMMC_D3					L16						SDMMC_D3	USB0_NXT		HPS GPIO47
7D	VREFB7A/B7C/D7END	HPS_RGMI0_TX_CLK					A16						RGMI0_TX_CLK			HPS GPIO0
7D	VREFB7A/B7C/D7END	HPS_RGMI0_TXD0					A17						RGMI0_TXD0	USB1_D0		HPS GPIO1
7D	VREFB7A/B7C/D7END	HPS_RGMI0_TXD1					A15						RGMI0_TXD1	USB1_D1		HPS GPIO2
7D	VREFB7A/B7C/D7END	HPS_RGMI0_TXD2					B17						RGMI0_TXD2	USB1_D2		HPS GPIO3
7D	VREFB7A/B7C/D7END	HPS_RGMI0_TXD3					C16						RGMI0_TXD3	USB1_D3		HPS GPIO4
7D	VREFB7A/B7C/D7END	HPS_RGMI0_RXD0					L16						RGMI0_RXD0	USB1_D4		HPS GPIO5
7D	VREFB7A/B7C/D7END	HPS_RGMI0_MIO0					C17						RGMI0_MIO0	USB1_D5	IC22_SDA	HPS GPIO6
7D	VREFB7A/B7C/D7END	HPS_RGMI0_MIO1					M16						RGMI0_MIO1	IC22_SCL		HPS GPIO7
7D	VREFB7A/B7C/D7END	HPS_RGMI0_RX_CTL					D17						RGMI0_RX_CTL	USB1_D7		HPS GPIO8
7D	VREFB7A/B7C/D7END	HPS_RGMI0_TX_CTL					E18						RGMI0_TX_CTL			HPS GPIO9
7D	VREFB7A/B7C/D7END	HPS_RGMI0_RX_CLK					D16						RGMI0_RX_CLK	USB1_CLK		HPS GPIO10
7D	VREFB7A/B7C/D7END	HPS_RGMI0_RXD1					F18						RGMI0_RXD1	USB1_STP		HPS GPIO11
7D	VREFB7A/B7C/D7END	HPS_RGMI0_RXD2					F17						RGMI0_RXD2	USB1_DRP		HPS GPIO12
7D	VREFB7A/B7C/D7END	HPS_RGMI0_RXD3					P16						RGMI0_RXD3	USB1_NXT		HPS GPIO13
7D	VREFB7A/B7C/D7END	HPS_RGMIH_TX_CLK					G17						RGMIH_TX_CLK			HPS GPIO48
7D	VREFB7A/B7C/D7END	HPS_RGMIH_TXD1					N16						RGMIH_TXD1			HPS GPIO50
7D	VREFB7A/B7C/D7END	HPS_RGMIH_TXD1					J17						RGMIH_TXD1			HPS GPIO50
7D	VREFB7A/B7C/D7END	HPS_RGMIH_TX_CTL					G18						RGMIH_TX_CTL			HPS GPIO51
7D	VREFB7A/B7C/D7END	HPS_RGMIH_RXD0					H17						RGMIH_RXD0			HPS GPIO52
7D	VREFB7A/B7C/D7END	HPS_RGMIH_RXD1					H17						RGMIH_RXD1			HPS GPIO53
7E	VREFB7A/B7C/D7END	HPS_RGMIH_MIO0					L17						RGMIH_MIO0	SPIM0_CLK	SPIS0_CLK	HPS GPIO54
7E	VREFB7A/B7C/D7END	HPS_RGMIH_MIO1					N18						RGMIH_MIO1	SPIM0_MOSI	SPIS0_MOSI	HPS GPIO55
7E	VREFB7A/B7C/D7END	HPS_RGMIH_TXD2					M17						RGMIH_TXD2	SPIM0_MISO	SPIS0_MISO	HPS GPIO56
7E	VREFB7A/B7C/D7END	HPS_RGMIH_TXD3					N18						RGMIH_TXD3	SPIM0_SS0	SPIS0_SS0	HPS GPIO57
7E	VREFB7A/B7C/D7END	HPS_RGMIH_RX_CLK					M18						RGMIH_RX_CLK	SPIS1_CLK	SPIM1_CLK	HPS GPIO58
7E	VREFB7A/B7C/D7END	HPS_RGMIH_RX_CTL					J18						RGMIH_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	HPS GPIO59
7E	VREFB7A/B7C/D7END	HPS_RGMIH_RXD2					N17						RGMIH_RXD2	SPIS1_MISO	SPIM1_MISO	HPS GPIO60
7E	VREFB7A/B7C/D7END	HPS_RGMIH_RXD3					L18						RGMIH_RXD3	SPIS1_SS0	SPIM1_SS0	HPS GPIO61
		VCC0_FPLL					T17									
		VCC0_FPLL					T16									
8D	VREFB8D0	IO	CLK19b					DIFF0_RX_T31p	DIFFOUT_T31p							
8D	VREFB8D0	IO	CLK19a					DIFF0_RX_T31n	DIFFOUT_T31n							
8D	VREFB8D0	IO	CLK18b					DIFF0_RX_T33p	DIFFOUT_T33p							
8D	VREFB8D0	IO	CLK18a					DIFF0_RX_T33n	DIFFOUT_T33n							
8D	VREFB8D0	IO						DIFF0_RX_T35p	DIFFOUT_T35p							
8D	VREFB8D0	IO	FPLL_TC_CLKOUT2_FPLL_TC_FBP_FPL4_TC_FB1					DIFF0_RX_T35p	DIFFOUT_T35p							
8D	VREFB8D0	IO						DIFF0_TX_T36p	DIFFOUT_T36p							
8D	VREFB8D0	IO	FPLL_TC_CLKOUT1_FPLL_TC_CLKOUT0_FPLL_TC_FB0					DIFF0_TX_T36p	DIFFOUT_T36p							
8D	VREFB8D0	IO	CLK17p					DIFF0_RX_T								





Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AB27									
		GND					AB28									
		GND					AB30									
		GND					AB31									
		GND					AB32									
		GND					AC30									
		GND					AC33									
		GND					AC34									
		GND					AD31									
		GND					AD32									
		GND					AE30									
		GND					AE33									
		GND					AE34									
		GND					AF31									
		GND					AF32									
		GND					AG30									
		GND					AG33									
		GND					AG34									
		GND					AH31									
		GND					AH32									
		GND					AJ30									
		GND					AJ33									
		GND					AJ34									
		GND					AK31									
		GND					AK32									
		GND					AL33									
		GND					AL34									
		GND					EM34									
		GND					F31									
		GND					F32									
		GND					G30									
		GND					G33									
		GND					G34									
		GND					H31									
		GND					H32									
		GND					J30									
		GND					J33									
		GND					J34									
		GND					K31									
		GND					K32									
		GND					L30									
		GND					L33									
		GND					L34									
		GND					M30									
		GND					M31									
		GND					M32									
		GND					N28									
		GND					N29									
		GND					N33									
		GND					N34									
		GND					P27									
		GND					P31									
		GND					P32									
		GND					P28									
		GND					R30									
		GND					R33									
		GND					R34									
		GND					T27									
		GND					T29									
		GND					T31									
		GND					T32									
		GND					U28									
		GND					U33									
		GND					U34									
		GND					V27									
		GND					V29									
		GND					V32									
		GND					W28									
		GND					W30									
		GND					W33									
		GND					W34									
		GND					Y27									
		GND					Y29									
		GND					Y31									
		GND					Y32									
		GND					AA1									
		GND					AA2									
		GND					AB3									
		GND					AB4									
		GND					AC1									
		GND					AC2									
		GND					AC5									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE5									
		GND					AF3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG5									
		GND					AH3									
		GND					AH4									
		GND					AJ1									
		GND					AJ2									
		GND					AJ5									
		GND					AK3									
		GND					AK4									
		GND					AL1									
		GND					AL2									
		GND					AL3									
		GND					AN1									
		GND					V3									
		GND					V4									
		GND					V7									
		GND					W1									
		GND					W2									
		GND					W5									
		GND					Y3									
		GND					Y4									
		GND					Y8									
		GND					Y8									
		VCCP					R18									
		VCCP					T21									
		VCCP					U5									
		VCCP					W10									
		VCCP					Y10									
		VCCP					Y12									
		VCCP					Y22									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCP					Y24									
		VCCP					Y25									
		VCCA_FPLL					V26									
		VCCA_FPLL					V9									
		VCCA_FPLL					T26									
		VCCPLL_HPS					M9									
		VCCBATT					M27									
		VCC_AUX					AA24									
		VCC_AUX					F11									
		VCC_AUX					E24									
		VCC_AUX_SHARED					R12									
		VCCD_FPLL					Y26									
		VCCD_FPLL					V9									
		VCCD_FPLL					P26									
		VCCA_GXBLO					Y28									
		VCCA_GXBRO					V7									
		VCCA_GXBL1					T28									
		VCCCH_GXBLO					V28									
		VCCCH_GXBRO					V16									
		VCCCH_GXBL1					P28									
		VCCCL_GXBLO					V29									
		VCCCL_GXBRO					V30									
		VCCCL_GXBRO					V5									
		VCCCL_GXBL1					Y5									
		VCCCL_GXBL1					P29									
		VCCCL_GXBL1					P30									
		VCCCR_GXBL					AA30									
		VCCCR_GXBL					AB29									
		VCCCR_GXBL					N30									
		VCCCR_GXBL					R29									
		VCCCR_GXBR					AA5									
		VCCCR_GXBR					AB6									
		VCCCR_GXBR					AB6									
		VCCCT_GXBLO					T30									
		VCCCT_GXBRO					U29									
		VCCCT_GXBLO					U30									
		VCCCT_GXBR0					W6									
		VCCCT_GXBR0					A8									
		VCCCT_GXBL1					W29									
		VCCCT_GXBL1					V30									
		VCC					AA30									
		VCC					T19									
		VCC					T23									
		VCC					T26									
		VCC					V24									
		VCC					U18									
		VCC					U20									
		VCC					U22									
		VCC					U24									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V20									
		VCC					V21									
		VCC					V22									
		VCC					V23									
		VCC					W16									
		VCC					W14									
		VCC					W20									
		VCC					W22									
		VCC					W24									
		VCC					Y13									
		VCC					Y14									
		VCC					Y15									
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y21									
		VCC					Y23									
		VCC					W18									
		VCC_HPS					T11									
		VCC_HPS					U10									
		VCC_HPS					U12									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V12									
		VCC_HPS					V13									
		VCC_HPS					W12									
		VCC00A					AF27									
		VCC00A					AF30									
		VCC00A					AH30									
		VCC00A					AJ28									
		VCC00A					AK30									
		VCC00A					AN29									
		VCC00B					AF25									
		VCC00B					AK24									
		VCC00B					AN24									
		VCC00C					AD21									
		VCC00C					AF21									
		VCC00C					AJ21									
		VCC00C					AM21									
		VCC00D					AE18									
		VCC00D					AH18									
		VCC00D					AL18									
		VCC00A					AD5									
		VCC00A					AEB									
		VCC00A					AF5									
		VCC00A					AH5									
		VCC00A					AK5									
		VCC00B					AD11									
		VCC00B					AF10									
		VCC00B					AJ10									
		VCC00B					AM10									
		VCC00C					AE13									
		VCC00C					AH12									
		VCC00C					AL12									
		VCC00D					AF16									
		VCC00D					AJ16									
		VCC00D					AM15									
		VCC00D					AN17									
		VCC00A_HPS					B3									
		VCC00A_HPS					CB									
		VCC00A_HPS					DB									
		VCC00A_HPS					EB									
		VCC00A_HPS					FB									
		VCC00A_HPS					H5									
		VCC00A_HPS					H7									
		VCC00A_HPS					M7									
		VCC00B_HPS					L4									







Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					D30									
		GND					E14									
		GND					E25									
		GND					E28									
		GND					E8									
		GND					F19									
		GND					F22									
		GND					F5									
		GND					G11									
		GND					G2									
		GND					H25									
		GND					H28									
		GND					H8									
		GND					J13									
		GND					J19									
		GND					J22									
		GND					J5									
		GND					K16									
		GND					K2									
		GND					L25									
		GND					L28									
		GND					L8									
		GND					M18									
		GND					M22									
		GND					M5									
		GND					N11									
		GND					N15									
		GND					N2									
		GND					N24									
		GND					P13									
		GND					P18									
		GND					P8									
		GND					V18									
		GND					V14									
		GND					V16									
		GND					V8									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					W23									
		GND					W28									
		GND					W9									
		GND					Y18									
		GND					Z20									
		GND					Z17									
		GND					R19									
		GND					R21									
		GND					R23									
		GND					R25									
		GND					R5									
		GND					R8									
		GND					T10									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T2									
		GND					T20									
		GND					T22									
		GND					T24									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U23									
		GND					U25									
		GND					U6									
		GND					U9									
		GND					V10									

Notes:  
(1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).  
(2) GND, REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.  
(3) Pins with \* contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.  
(4) Pins with \* are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).  
(5) RESET pin is only applicable for DDR3 device.





















Bank Number	VREF	PinName/Function (Z1) (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for B0K93 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AJ38									
		GND					AJ99									
		GND					AK36									
		GND					AK37									
		GND					AL35									
		GND					AL38									
		GND					AL39									
		GND					AM36									
		GND					AM37									
		GND					AN35									
		GND					AN38									
		GND					AN39									
		GND					AP36									
		GND					AP37									
		GND					AR35									
		GND					AR38									
		GND					AR39									
		GND					AT36									
		GND					AT37									
		GND					AL35									
		GND					AV38									
		GND					AV39									
		GND					AV36									
		GND					AV39									
		GND					AW35									
		GND					AW38									
		GND					B36									
		GND					B37									
		GND					C36									
		GND					C38									
		GND					C39									
		GND					D36									
		GND					D37									
		GND					E35									
		GND					E38									
		GND					E39									
		GND					F36									
		GND					F37									
		GND					G35									
		GND					G38									
		GND					G39									
		GND					H36									
		GND					H37									
		GND					J35									
		GND					J38									
		GND					J39									
		GND					K36									
		GND					K37									
		GND					L35									
		GND					L38									
		GND					L39									
		GND					M36									
		GND					M37									
		GND					N35									
		GND					N38									
		GND					N39									
		GND					P36									
		GND					P37									
		GND					R34									
		GND					R38									
		GND					R39									
		GND					T32									
		GND					T36									
		GND					T37									
		GND					U33									
		GND					U36									
		GND					U38									
		GND					U39									
		GND					V36									
		GND					V34									
		GND					V38									
		GND					V39									
		GND					W33									
		GND					W38									
		GND					W39									
		GND					Y31									
		GND					Y32									
		GND					Y36									
		GND					Y37									
		GND					AA3									
		GND					AA4									
		GND					AA6									
		GND					AA8									
		GND					AB1									
		GND					AB2									
		GND					AB7									
		GND					AC3									
		GND					AC4									
		GND					AC9									
		GND					AD1									
		GND					AD9									
		GND					AD5									
		GND					AD7									
		GND					AE3									
		GND					AE4									
		GND					AE6									
		GND					AE8									
		GND					AF1									
		GND					AF2									
		GND					AF9									
		GND					AG3									
		GND					AG4									
		GND					AG5									
		GND					AG6									
		GND					AG7									
		GND					AG8									
		GND					AH1									
		GND					AH2									
		GND					AH5									
		GND					AJ3									
		GND					AJ4									
		GND					AK1									
		GND					AK3									
		GND					AK5									
		GND					AL3									
		GND					AL4									
		GND					AM1									









Bank Number	VREF	PinName/Function (2) (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DQR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					E32									
		GND					E5									
		GND					E9									
		GND					F14									
		GND					H11									
		GND					H17									
		GND					H5									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					J14									
		GND					K20									
		GND					L11									
		GND					L17									
		GND					L2									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L32									
		GND					L5									
		GND					L8									
		GND					N14									
		GND					N17									
		GND					N20									
		GND					P11									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P32									
		GND					P8									
		GND					W21									
		GND					T12									
		GND					T15									
		GND					T16									
		GND					T18									
		GND					T20									
		GND					T8									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U23									
		GND					U25									
		GND					U27									
		GND					U30									
		GND					U7									
		GND					V14									
		GND					V8									
		GND					V18									
		GND					V21									
		GND					V24									
		GND					V26									
		GND					V28									
		GND					V30									
		GND					V8									
		GND					W27									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W23									
		GND					W25									
		GND					W29									
		GND					Y10									
		GND					Y12									
		GND					Y14									
		GND					Y16									
		GND					Y18									
		GND					Y20									
		GND					Y22									
		GND					Y24									
		GND					Y26									
		GND					Y28									

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).  
 (2) GNB\_REFLCK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.  
 (3) Pins with \* contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.  
 (4) Pins with # are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).  
 (5) RESET pin is only applicable for DQR3 device.



**Pin Information for the Arria® V 5ASXBB5 Device  
Version 1.3**

<b>Version Number</b>	<b>Date</b>	<b>Changes Made</b>
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.