



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)	
		DNU					E33					
		DNU					F33					
		RREF_TL					F34					
GXB L1		REFCLK3Ln					R27					
GXB L1		REFCLK3p					R26					
GXB L1		GXB TX L11n					G31					
GXB L1		GXB TX L11p					G32					
GXB L1		GXB RX L11p,GXB REFCLK L11p					H34					
GXB L1		GXB RX L11n,GXB REFCLK L11n					H33					
GXB L1		GXB TX L10n					J31					
GXB L1		GXB TX L10p					J32					
GXB L1		GXB RX L10p,GXB REFCLK L10p					K34					
GXB L1		GXB RX L10n,GXB REFCLK L10n					K33					
GXB L1		GXB TX L9n					L31					
GXB L1		GXB TX L9p					L32					
GXB L1		GXB RX L9p,GXB REFCLK L9p					M34					
GXB L1		GXB RX L9n,GXB REFCLK L9n					M33					
GXB L1		GXB TX L8n					N31					
GXB L1		GXB TX L8p					N32					
GXB L1		GXB RX L8p,GXB REFCLK L8p					P34					
GXB L1		GXB RX L8n,GXB REFCLK L8n					P33					
GXB L1		GXB TX L7n					R31					
GXB L1		GXB TX L7p					R32					
GXB L1		GXB RX L7p,GXB REFCLK L7p					T34					
GXB L1		GXB RX L7n,GXB REFCLK L7n					T33					
GXB L1		GXB TX L6n					U31					
GXB L1		GXB TX L6p					U32					
GXB L1		GXB RX L6p,GXB REFCLK L6p					V34					
GXB L1		GXB RX L6n,GXB REFCLK L6n					V33					
GXB L1		REFCLK2Ln					U27					
GXB L1		REFCLK2p					U26					
GXB L0		REFCLK1Ln					W27					
GXB L0		REFCLK1p					W26					
GXB L0		GXB TX L5n					W31					
GXB L0		GXB TX L5p					W32					
GXB L0		GXB RX L5p,GXB REFCLK L5p					Y34					
GXB L0		GXB RX L5n,GXB REFCLK L5n					Y33					
GXB L0		GXB TX L4n					AA31					
GXB L0		GXB TX L4p					AA32					
GXB L0		GXB RX L4p,GXB REFCLK L4p					AB34					
GXB L0		GXB RX L4n,GXB REFCLK L4n					AB33					
GXB L0		GXB TX L3n					AC31					
GXB L0		GXB TX L3p					AC32					
GXB L0		GXB RX L3p,GXB REFCLK L3p					AD34					
GXB L0		GXB RX L3n,GXB REFCLK L3n					AD33					
GXB L0		GXB TX L2n					AE31					
GXB L0		GXB TX L2p					AE32					
GXB L0		GXB RX L2p,GXB REFCLK L2p					AF34					
GXB L0		GXB RX L2n,GXB REFCLK L2n					AF33					
GXB L0		GXB TX L1n					AG31					
GXB L0		GXB TX L1p					AG32					
GXB L0		GXB RX L1p,GXB REFCLK L1p					AH34					
GXB L0		GXB RX L1n,GXB REFCLK L1n					AH33					
GXB L0		GXB TX L0n					AJ31					
GXB L0		GXB TX L0p					AJ32					
GXB L0		GXB RX L0p,GXB REFCLK L0p					AK34					
GXB L0		GXB RX L0n,GXB REFCLK L0n					AK33					
GXB L0		REFCLK0Ln					AA28					
GXB L0		REFCLK0p					AA27					
		DNU					AL32					
3A		TDO		TDO			AC28					
3A		TMS		TMS			AF30					
3A		TCK		TCK			AN32					
3A		TDI		TDI			AC29					
3A		DCLK		DCLK			AM32					
3A		nCS0		DATA4			AM34					
3A		AS_DATA3		DATA3			AM33					
3A		AS_DATA2		DATA2			AP33					
3A		AS_DATA1		DATA1			AN33					
3A		AS_DATA0,ASDO		DATA0			AN34					
3A	VREFB3A0	IO	RZ0_0				DIFFIO_TX_B1n	DIFFOUT_B1n			AL31	
3A	VREFB3A0	IO					DIFFIO_TX_B1p	DIFFOUT_B1p			AM31	DO1B
3A	VREFB3A0	IO	CLK0n				DIFFIO_RX_B2n	DIFFOUT_B2n			AP31	DO1B
3A	VREFB3A0	IO	CLK0p				DIFFIO_RX_B2p	DIFFOUT_B2p			AP32	DO1B
3A	VREFB3A0	IO					DIFFIO_TX_B3n	DIFFOUT_B3n			AD27	
3A	VREFB3A0	IO					DIFFIO_TX_B3p	DIFFOUT_B3p			AD26	DO1B
3A	VREFB3A0	IO	CLK1n				DIFFIO_RX_B4n	DIFFOUT_B4n			AJ29	DQ3n1B/QK1B
3A	VREFB3A0	IO	CLK1p				DIFFIO_RX_B4p	DIFFOUT_B4p			AJ28	DQ3n1B/CQ2B/CQn1B/QKn1B
3A	VREFB3A0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn				DIFFIO_TX_B5n	DIFFOUT_B5n			AL30	
3A	VREFB3A0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0				DIFFIO_TX_B5p	DIFFOUT_B5p			AM30	DO1B
3A	VREFB3A0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn				DIFFIO_RX_B6n	DIFFOUT_B6n			AN30	DO1B
3A	VREFB3A0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1				DIFFIO_RX_B6p	DIFFOUT_B6p			AP30	DO1B
3A	VREFB3A0	IO	VREFB3A0								AE27	
3A	VREFB3A0	IO									AF28	DO1B
3A	VREFB3A0	IO	CLK2n				DIFFIO_RX_B7n	DIFFOUT_B7n			AH28	DO1B
3A	VREFB3A0	IO	CLK2p				DIFFIO_RX_B7p	DIFFOUT_B7p			AJ28	DO1B
3A	VREFB3A0	IO					DIFFIO_TX_B8n	DIFFOUT_B8n			AL29	
3A	VREFB3A0	IO					DIFFIO_TX_B8p	DIFFOUT_B8p			AM29	DO2B
3A	VREFB3A0	IO	CLK3n				DIFFIO_RX_B9n	DIFFOUT_B9n			AN29	DO2B
3A	VREFB3A0	IO	CLK3p				DIFFIO_RX_B9p	DIFFOUT_B9p			AP29	DO2B
3A	VREFB3A0	IO					DIFFIO_TX_B10n	DIFFOUT_B10n			AE29	
3A	VREFB3A0	IO					DIFFIO_TX_B10p	DIFFOUT_B10p			AF29	DO2B
3A	VREFB3A0	IO					DIFFIO_RX_B11n	DIFFOUT_B11n			AG27	DQ3n2B/QK2B
3A	VREFB3A0	IO					DIFFIO_RX_B11p	DIFFOUT_B11p			AH27	DO1B
3A	VREFB3A0	IO					DIFFIO_TX_B12n	DIFFOUT_B12n			AL28	DQ3n2B/CQ2B/CQn2B/QKn2B
3A	VREFB3A0	IO					DIFFIO_TX_B12p	DIFFOUT_B12p			AM28	DO2B
3A	VREFB3A0	IO					DIFFIO_RX_B13n	DIFFOUT_B13n			AP27	DO2B
3A	VREFB3A0	IO					DIFFIO_RX_B13p	DIFFOUT_B13p			AP28	DO2B
3A	VREFB3A0	IO					DIFFIO_TX_B14n	DIFFOUT_B14n			AG29	DO1B
											A_3A_15	



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
3A	VREFB3A0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AH29	DQ2B	DQ1B		A_3A_14
3A	VREFB3A0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AK27	DQ2B	DQ1B		A_3A_13
3A	VREFB3A0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AL27	DQ2B	DQ1B		A_3A_12
3A	VREFB3A0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AG26				A_3A_11
3A	VREFB3A0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AH26	DQ3B	DQ1B		A_3A_10
3A	VREFB3A0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AJ26	DQ3B	DQ1B		A_3A_9
3A	VREFB3A0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AK26	DQ3B	DQ1B		A_3A_8
3A	VREFB3A0	IO			DIFFIO_TX_B18n	DIFFOUT_B18n	AD29				A_3A_7
3A	VREFB3A0	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AE28	DQ3B	DQ1B		A_3A_6
3A	VREFB3A0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AL26	DQ3n3B/QK3B	DQ3n1B/QK1B		A_3A_5
3A	VREFB3A0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AM25	DQ33B/CQ3B/CQn3B/QKn3B	DQ31B/CQ1B/CQn1B/QKn1B		A_3A_4
3A	VREFB3A0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AN27				A_3A_3
3A	VREFB3A0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AN26	DQ3B	DQ1B		A_3A_2
3A	VREFB3A0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AP25	DQ3B	DQ1B		A_3A_1
3A	VREFB3A0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AP26	DQ3B	DQ1B		A_3A_0
3A	VREFB3A0	IO			DIFFIO_TX_B22n	DIFFOUT_B22n	AC28				CKE_3A_1
3A	VREFB3A0	IO			DIFFIO_TX_B22p	DIFFOUT_B22p	AF28	DQ3B	DQ1B		CKE_3A_0
3A	VREFB3A0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AL25	DQ3B	DQ1B		CKf_3A
3A	VREFB3A0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AM25	DQ3B	DQ1B		CK_3A
3B	VREFB3B0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AE23				RESETf_3A
3B	VREFB3B0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AE24	DQ4B	DQ1B		DQ1_3B_8
3B	VREFB3B0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AC24	DQ4B	DQ1B		DQ1_3B_7
3B	VREFB3B0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AC25	DQ4B	DQ1B		DQ1_3B_6
3B	VREFB3B0	IO			DIFFIO_TX_B26n	DIFFOUT_B26n	AA25				
3B	VREFB3B0	IO			DIFFIO_TX_B26p	DIFFOUT_B26p	AB25	DQ4B	DQ1B		DM1_3B
3B	VREFB3B0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AE24	DQ5n4B/QK4B	DQ5n2B	DQ1B	DQ5n1_3B
3B	VREFB3B0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AE25	DQ54B/CQ4B/CQn4B/QKn4B	DQ52B	DQ1B	DQ51_3B
3B	VREFB3B0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AF25				
3B	VREFB3B0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AG24	DQ4B	DQ1B		DQ1_3B_5
3B	VREFB3B0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AH24	DQ4B	DQ1B		DQ1_3B_4
3B	VREFB3B0	IO	VREFB3B0		DIFFIO_RX_B29p	DIFFOUT_B29p	AH25	DQ4B	DQ1B		DQ1_3B_3
3B	VREFB3B0	IO					Y23				
3B	VREFB3B0	IO					AB24	DQ4B	DQ1B		DQ1_3B_2
3B	VREFB3B0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AJ25	DQ4B	DQ1B		DQ1_3B_1
3B	VREFB3B0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AK24	DQ4B	DQ1B		DQ1_3B_0
3B	VREFB3B0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AK23				
3B	VREFB3B0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AL24	DQ5B	DQ1B		DQ2_3B_8
3B	VREFB3B0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AF23	DQ5B	DQ1B		DQ2_3B_7
3B	VREFB3B0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AG23	DQ5B	DQ1B		DQ2_3B_6
3B	VREFB3B0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC23				
3B	VREFB3B0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AD23	DQ5B	DQ1B		DM2_3B
3B	VREFB3B0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AH23	DQ5n4B/QK5B	DQ5n2B/QK2B	DQ1B	DQ5n1_3B
3B	VREFB3B0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AJ23	DQ55B/CQ5B/CQn5B/QKn5B	DQ53B/CQ3B/CQn3B/QKn3B	DQ1B	DQ52_3B
3B	VREFB3B0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AL23				
3B	VREFB3B0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AM23	DQ5B	DQ1B		DQ2_3B_5
3B	VREFB3B0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AN23	DQ5B	DQ1B		DQ2_3B_4
3B	VREFB3B0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AN24	DQ5B	DQ1B		DQ2_3B_3
3B	VREFB3B0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA23				
3B	VREFB3B0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AB23	DQ5B	DQ1B		DQ2_3B_2
3B	VREFB3B0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AP22	DQ5B	DQ1B		DQ2_3B_1
3B	VREFB3B0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AP23	DQ5B	DQ1B		DQ2_3B_0
3C	VREFB3C0	IO			DIFFIO_TX_B39n	DIFFOUT_B39n	AE21				
3C	VREFB3C0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AE22	DQ6B	DQ1B		DQ3_3C_8
3C	VREFB3C0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AL21	DQ6B	DQ1B		DQ3_3C_7
3C	VREFB3C0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AL22	DQ6B	DQ1B		DQ3_3C_6
3C	VREFB3C0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22				
3C	VREFB3C0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AC22	DQ6B	DQ1B		DM3_3C
3C	VREFB3C0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AH21	DQ5n6B/QK6B	DQ5n1B/QK1B	DQ1B	DQ5n3_3C
3C	VREFB3C0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AH22	DQ56B/CQ6B/CQn6B/QKn6B	DQ53_3C	DQ1B	DQ52_3C
3C	VREFB3C0	IO			DIFFIO_TX_B43n	DIFFOUT_B43n	AF22				
3C	VREFB3C0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AG21	DQ6B	DQ1B		DQ3_3C_5
3C	VREFB3C0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AJ22	DQ6B	DQ1B		DQ3_3C_4
3C	VREFB3C0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AK21	DQ6B	DQ1B		DQ3_3C_3
3C	VREFB3C0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AA21				
3C	VREFB3C0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AB21	DQ6B	DQ1B		DQ3_3C_2
3C	VREFB3C0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AM22	DQ6B	DQ1B		DQ3_3C_1
3C	VREFB3C0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AN21	DQ6B	DQ1B		DQ3_3C_0
3C	VREFB3C0	IO			DIFFIO_TX_B47n	DIFFOUT_B47n	AC21				
3C	VREFB3C0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AD21	DQ7B	DQ1B		DQ4_3C_8
3C	VREFB3C0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AN20	DQ7B	DQ1B		DQ4_3C_7
3C	VREFB3C0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AP20	DQ7B	DQ1B		DQ4_3C_6
3C	VREFB3C0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AA20				
3C	VREFB3C0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB20	DQ7B	DQ1B		DM4_3C
3C	VREFB3C0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AL20	DQ5n7B/QK7B	DQ5n3B/QK3B	DQ1B	DQ5n4_3C
3C	VREFB3C0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AM20	DQ57B/CQ7B/CQn7B/QKn7B	DQ53B/CQ3B/CQn3B/QKn3B	DQ1B	DQ54_3C
3C	VREFB3C0	IO			DIFFIO_TX_B51n	DIFFOUT_B51n	AJ20				
3C	VREFB3C0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AK20	DQ7B	DQ1B		DQ4_3C_5
3C	VREFB3C0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AC20	DQ7B	DQ1B		DQ4_3C_4
3C	VREFB3C0	IO	VREFB3C0		DIFFIO_RX_B52p	DIFFOUT_B52p	AH20	DQ7B	DQ1B		DQ4_3C_3
3C	VREFB3C0	IO					AC20				
3C	VREFB3C0	IO					AD20	DQ7B	DQ1B		DQ4_3C_2
3C	VREFB3C0	IO			DIFFIO_RX_B53n	DIFFOUT_B53n	AE20	DQ7B	DQ1B		DQ4_3C_1
3C	VREFB3C0	IO			DIFFIO_RX_B53p	DIFFOUT_B53p	AF20	DQ7B	DQ1B		DQ4_3C_0
3D	VREFB3D0	IO			DIFFIO_TX_B54n	DIFFOUT_B54n	AH19				
3D	VREFB3D0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AJ19	DQ8B	DQ4B		
3D	VREFB3D0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AL19	DQ8B	DQ4B		
3D	VREFB3D0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AM19	DQ8B	DQ4B		
3D	VREFB3D0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AB19				
3D	VREFB3D0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AC19	DQ8B	DQ4B		
3D	VREFB3D0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AN18	DQ5n8B/QK8B	DQ4B		
3D	VREFB3D0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AP19	DQ58B/CQ8B/CQn8B/QKn8B	DQ4B		
3D	VREFB3D0	IO			DIFFIO_TX_B58n	DIFFOUT_B58n	AE19				
3D	VREFB3D0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AF19	DQ8B	DQ4B		
3D	VREFB3D0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AK18	DQ8B	DQ4B		
3D	VREFB3D0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AL18	DQ8B	DQ4B		
3D	VREFB3D0	IO	VREFB3D0				AB18				
3D	VREFB3D0	IO					AA18	DQ8B	DQ4B		
3D	VREFB3D0	IO	CLK4n		DIFFIO_RX_B60n	DIFFOUT_B60n	AG18	DQ8B	DQ4B		
3D	VREFB3D0	IO	CLK4p		DIFFIO_RX_B60p	DIFFOUT_B60p	AH18	DQ8B	DQ4B		



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
3D	VREFB3DNO	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AN17				
3D	VREFB3DNO	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AP17	DO9B			
3D	VREFB3DNO	IO	CLK5n		DIFFIO_RX_B62n	DIFFOUT_B62n	AG17	DO9B			DO4B
3D	VREFB3DNO	IO	CLK5p		DIFFIO_RX_B62p	DIFFOUT_B62p	AH17	DO9B			DO4B
3D	VREFB3DNO	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B63n	DIFFOUT_B63n	AA17				
3D	VREFB3DNO	IO	FPLL_BC_CLKOUT3,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B63p	DIFFOUT_B63p	AB17	DO9B			
3D	VREFB3DNO	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBn		DIFFIO_RX_B64n	DIFFOUT_B64n	AJ17	DO9nB/QK9B			DO9n4B/QK4B
3D	VREFB3DNO	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B64p	DIFFOUT_B64p	AK17	DO9nB/CQ9B/CQn9B/QKn9B			DO9n4B/CQ4B/CQn4B/QKn4B
3D	VREFB3DNO	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AL17				
3D	VREFB3DNO	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AM17	DO9B			DO4B
3D	VREFB3DNO	IO	CLK6n		DIFFIO_RX_B66n	DIFFOUT_B66n	AE17	DO9B			DO4B
3D	VREFB3DNO	IO	CLK6p		DIFFIO_RX_B66p	DIFFOUT_B66p	AF17	DO9B			DO4B
3D	VREFB3DNO	IO			DIFFIO_TX_B67n	DIFFOUT_B67n	AC17				
3D	VREFB3DNO	IO			DIFFIO_TX_B67p	DIFFOUT_B67p	AC18	DO9B			DO4B
3D	VREFB3DNO	IO	CLK7n		DIFFIO_RX_B68n	DIFFOUT_B68n	AD17	DO9B			DO4B
3D	VREFB3DNO	IO	CLK7p		DIFFIO_RX_B68p	DIFFOUT_B68p	AE18	DO9B			DO4B
		VCCD_FPLL					Y17				
		VCCA_FPLL					Y18				
		DNU					AD18				
4D	VREFB4DNO	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AF18				CS#r 4D_1
4D	VREFB4DNO	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AN18	DO10B			CS#r 4D_0
4D	VREFB4DNO	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AH18	DO10B			DO5B
4D	VREFB4DNO	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AJ18	DO10B			DO5B
4D	VREFB4DNO	IO			DIFFIO_TX_B71n	DIFFOUT_B71n	AE18				A_4D_15
4D	VREFB4DNO	IO			DIFFIO_TX_B71p	DIFFOUT_B71p	AF18	DO10B			ODT_4D_1
4D	VREFB4DNO	IO			DIFFIO_RX_B72n	DIFFOUT_B72n	Y18	DO9n10B/QK10B			W#r 4D
4D	VREFB4DNO	IO			DIFFIO_RX_B72p	DIFFOUT_B72p	AA18	DO9n10B/CQ10B/CQn10B/QKn10B			DO5B
4D	VREFB4DNO	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AB18				CASH_4D
4D	VREFB4DNO	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AC16	DO10B			RAS#_4D
4D	VREFB4DNO	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AL18	DO10B			BA_4D_2
4D	VREFB4DNO	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AM18	DO10B			BA_4D_1
4D	VREFB4DNO	IO	VREFB4DNO				AJ14				BA_4D_0
4D	VREFB4DNO	IO					AK14	DO10B			A_4D_14
4D	VREFB4DNO	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AL14	DO10B			DO5B
4D	VREFB4DNO	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AM14	DO10B			DO5B
4D	VREFB4DNO	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AA14				A_4D_12
4D	VREFB4DNO	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AB15	DO11B			A_4D_11
4D	VREFB4DNO	IO			DIFFIO_RX_B77n	DIFFOUT_B77n	AK15	DO11B			DO5B
4D	VREFB4DNO	IO			DIFFIO_RX_B77p	DIFFOUT_B77p	AL15	DO11B			DO5B
4D	VREFB4DNO	IO			DIFFIO_TX_B78n	DIFFOUT_B78n	AG14				A_4D_7
4D	VREFB4DNO	IO			DIFFIO_TX_B78p	DIFFOUT_B78p	AH14	DO11B			A_4D_6
4D	VREFB4DNO	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AG15	DO9n11B/QK11B			DO5B/QK5B
4D	VREFB4DNO	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AH15	DO9n11B/CQ11B/CQn11B/QKn11B			DO5B/CQ5B/CQn5B/QKn5B
4D	VREFB4DNO	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AD15				A_4D_3
4D	VREFB4DNO	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AE15	DO11B			A_4D_2
4D	VREFB4DNO	IO			DIFFIO_RX_B81n	DIFFOUT_B81n	AE14	DO11B			A_4D_1
4D	VREFB4DNO	IO			DIFFIO_RX_B81p	DIFFOUT_B81p	AF14	DO11B			A_4D_0
4D	VREFB4DNO	IO			DIFFIO_TX_B82n	DIFFOUT_B82n	AB14				CKE_4D_1
4D	VREFB4DNO	IO			DIFFIO_TX_B82p	DIFFOUT_B82p	AC15	DO11B			CKE_4D_0
4D	VREFB4DNO	IO			DIFFIO_RX_B83n	DIFFOUT_B83n	AC14	DO11B			CK#_4D
4D	VREFB4DNO	IO			DIFFIO_RX_B83p	DIFFOUT_B83p	AD14	DO11B			CK_4D
4C	VREFB4CNO	IO			DIFFIO_TX_B84n	DIFFOUT_B84n	AB13				RESET#_4D
4C	VREFB4CNO	IO			DIFFIO_TX_B84p	DIFFOUT_B84p	AC13	DO12B		DO2B	DO1_4C_8
4C	VREFB4CNO	IO			DIFFIO_RX_B85n	DIFFOUT_B85n	AN14	DO12B		DO2B	DO1_4C_7
4C	VREFB4CNO	IO			DIFFIO_RX_B85p	DIFFOUT_B85p	AP14	DO12B		DO2B	DO1_4C_6
4C	VREFB4CNO	IO			DIFFIO_TX_B86n	DIFFOUT_B86n	AM12				
4C	VREFB4CNO	IO			DIFFIO_TX_B86p	DIFFOUT_B86p	AP13	DO12B		DO2B	DM1_4C
4C	VREFB4CNO	IO			DIFFIO_RX_B87n	DIFFOUT_B87n	AL13	DO9n12B/QK12B		DO2B	DO9n1_4C
4C	VREFB4CNO	IO			DIFFIO_RX_B87p	DIFFOUT_B87p	AM13	DO9n12B/CQ12B/CQn12B/QKn12B		DO2B	DO9n1_4C
4C	VREFB4CNO	IO			DIFFIO_TX_B88n	DIFFOUT_B88n	Y11				
4C	VREFB4CNO	IO			DIFFIO_TX_B88p	DIFFOUT_B88p	AA12	DO12B		DO2B	DO1_4C_5
4C	VREFB4CNO	IO			DIFFIO_RX_B89n	DIFFOUT_B89n	AK12	DO12B		DO2B	DO1_4C_4
4C	VREFB4CNO	IO			DIFFIO_RX_B89p	DIFFOUT_B89p	AL12	DO12B		DO2B	DO1_4C_3
4C	VREFB4CNO	IO	VREFB4CNO				AK11				
4C	VREFB4CNO	IO					AL11	DO12B		DO2B	DO1_4C_2
4C	VREFB4CNO	IO			DIFFIO_RX_B90n	DIFFOUT_B90n	AH13	DO12B		DO2B	DO1_4C_1
4C	VREFB4CNO	IO			DIFFIO_RX_B90p	DIFFOUT_B90p	AJ13	DO12B		DO2B	DO1_4C_0
4C	VREFB4CNO	IO			DIFFIO_TX_B91n	DIFFOUT_B91n	AB11				
4C	VREFB4CNO	IO			DIFFIO_TX_B91p	DIFFOUT_B91p	AB12	DO13B		DO2B	DO2_4C_8
4C	VREFB4CNO	IO			DIFFIO_RX_B92n	DIFFOUT_B92n	AG12	DO13B		DO2B	DO2_4C_7
4C	VREFB4CNO	IO			DIFFIO_RX_B92p	DIFFOUT_B92p	AH12	DO13B		DO2B	DO2_4C_6
4C	VREFB4CNO	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AH11				
4C	VREFB4CNO	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AJ11	DO13B		DO2B	DO2_4C_5
4C	VREFB4CNO	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AE13	DO9n13B/QK13B		DO2B	DO9n2_4C
4C	VREFB4CNO	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AF13	DO9n13B/CQ13B/CQn13B/QKn13B		DO2B	DO9n2_4C
4C	VREFB4CNO	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AC11				
4C	VREFB4CNO	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AC12	DO13B		DO2B	DO2_4C_5
4C	VREFB4CNO	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AK12	DO13B		DO2B	DO2_4C_4
4C	VREFB4CNO	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AE12	DO13B		DO2B	DO2_4C_3
4C	VREFB4CNO	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	AD11				
4C	VREFB4CNO	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	AE11	DO13B		DO2B	DO2_4C_2
4C	VREFB4CNO	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AF11	DO13B		DO2B	DO2_4C_1
4C	VREFB4CNO	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AG11	DO13B		DO2B	DO2_4C_0
4B	VREFB4BNO	IO			DIFFIO_TX_B99n	DIFFOUT_B99n	AD9				
4B	VREFB4BNO	IO			DIFFIO_TX_B99p	DIFFOUT_B99p	AE9	DO14B		DO2B	DO3_4B_8
4B	VREFB4BNO	IO			DIFFIO_RX_B100n	DIFFOUT_B100n	AM11	DO14B		DO2B	DO3_4B_7
4B	VREFB4BNO	IO			DIFFIO_RX_B100p	DIFFOUT_B100p	AN11	DO14B		DO2B	DO3_4B_6
4B	VREFB4BNO	IO			DIFFIO_TX_B101n	DIFFOUT_B101n	AL10				
4B	VREFB4BNO	IO			DIFFIO_TX_B101p	DIFFOUT_B101p	AM10	DO14B		DO2B	DO3_4B_5
4B	VREFB4BNO	IO			DIFFIO_RX_B102n	DIFFOUT_B102n	AP10	DO9n14B/QK14B		DO2B	DO9n3_4B
4B	VREFB4BNO	IO			DIFFIO_RX_B102p	DIFFOUT_B102p	AP11	DO9n14B/CQ14B/CQn14B/QKn14B		DO2B	DO9n3_4B
4B	VREFB4BNO	IO			DIFFIO_TX_B103n	DIFFOUT_B103n	AA10				
4B	VREFB4BNO	IO			DIFFIO_TX_B103p	DIFFOUT_B103p	AB10	DO14B		DO2B	DO3_4B_5
4B	VREFB4BNO	IO			DIFFIO_RX_B104n	DIFFOUT_B104n	AH10	DO14B		DO2B	DO3_4B_4
4B	VREFB4BNO	IO			DIFFIO_RX_B104p	DIFFOUT_B104p	AJ10	DO14B		DO2B	DO3_4B_3
4B	VREFB4BNO	IO			DIFFIO_TX_B105n	DIFFOUT_B105n	AK9				
4B	VREFB4BNO	IO			DIFFIO_TX_B105p	DIFFOUT_B105p	AL9	DO14B		DO2B	DO3_4B_2
4B	VREFB4BNO	IO			DIFFIO_RX_B106n	DIFFOUT_B106n	AN9	DO14B		DO2B	DO3_4B_1
4B	VREFB4BNO	IO			DIFFIO_RX_B106p	DIFFOUT_B106p	AN8	DO14B		DO2B	DO3_4B_0



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
4B	VREFB4B0	IO			DIFFIO_TX_B107n	DIFFOUT_B107n	AC9				
4B	VREFB4B0	IO			DIFFIO_TX_B107p	DIFFOUT_B107p	AC10	DO15B	DO7B	DO2B	DO4_4B_8
4B	VREFB4B0	IO			DIFFIO_RX_B108n	DIFFOUT_B108n	AG9	DO15B	DO7B	DO2B	DO4_4B_7
4B	VREFB4B0	IO			DIFFIO_RX_B108p	DIFFOUT_B108p	AH9	DO15B	DO7B	DO2B	DO4_4B_6
4B	VREFB4B0	IO			DIFFIO_TX_B109n	DIFFOUT_B109n	AE10				
4B	VREFB4B0	IO			DIFFIO_TX_B109p	DIFFOUT_B109p	AF10	DO15B	DO7B	DO2B	DM4_4B
4B	VREFB4B0	IO			DIFFIO_RX_B110n	DIFFOUT_B110n	AL8	DQSn15B/QK15B	DQSn7B/QK7B	DO2B	DQSn4_4B
4B	VREFB4B0	IO			DIFFIO_RX_B110p	DIFFOUT_B110p	AM8	DQSn15B/CO15B/Con15B/QKn15B	DQSn7B/CO7B/Con7B/QKn7B	DO2B	DQSn4_4B
4B	VREFB4B0	IO			DIFFIO_TX_B111n	DIFFOUT_B111n	AC8				
4B	VREFB4B0	IO			DIFFIO_TX_B111p	DIFFOUT_B111p	AD8	DO15B	DO7B	DO2B	DO4_4B_5
4B	VREFB4B0	IO			DIFFIO_RX_B112n	DIFFOUT_B112n	AJ8	DO15B	DO7B	DO2B	DO4_4B_4
4B	VREFB4B0	IO			DIFFIO_RX_B112p	DIFFOUT_B112p	AK8	DO15B	DO7B	DO2B	DO4_4B_3
4B	VREFB4B0	IO	VREFB4B0				AE8				
4B	VREFB4B0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AF8	DO15B	DO7B	DO2B	DO4_4B_2
4B	VREFB4B0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AH8	DO15B	DO7B	DO2B	DO4_4B_1
4A	VREFB4A0	IO			DIFFIO_TX_B114n	DIFFOUT_B114n	AP8				DO4_4B_0
4A	VREFB4A0	IO		DATA10	DIFFIO_TX_B114p	DIFFOUT_B114p	AP7	DO16B		DO8B	
4A	VREFB4A0	IO		DATA5	DIFFIO_RX_B115n	DIFFOUT_B115n	AL7	DO16B	DO8B		
4A	VREFB4A0	IO		DATA6	DIFFIO_RX_B115p	DIFFOUT_B115p	AM7	DO16B	DO8B		
4A	VREFB4A0	IO		DATA12	DIFFIO_TX_B116n	DIFFOUT_B116n	AM6				
4A	VREFB4A0	IO		DATA13	DIFFIO_TX_B116p	DIFFOUT_B116p	AN6	DO16B	DO8B		
4A	VREFB4A0	IO		DATA7	DIFFIO_RX_B117n	DIFFOUT_B117n	AP6	DQSn16B/QK16B	DO8B		
4A	VREFB4A0	IO		DATA8	DIFFIO_RX_B117p	DIFFOUT_B117p	AP5	DQSn16B/CO16B/Con16B/QKn16B	DO8B		
4A	VREFB4A0	IO		DATA14	DIFFIO_TX_B118n	DIFFOUT_B118n	AE7				
4A	VREFB4A0	IO		DATA15	DIFFIO_TX_B118p	DIFFOUT_B118p	AF7	DO16B	DO8B		
4A	VREFB4A0	IO		DATA9	DIFFIO_RX_B119n	DIFFOUT_B119n	AM6	DO16B	DO8B		
4A	VREFB4A0	IO		CLKUSR	DIFFIO_RX_B119p	DIFFOUT_B119p	AN5	DO16B	DO8B		
4A	VREFB4A0	IO	VREFB4A0				AK6				
4A	VREFB4A0	IO					AL6	DO16B	DO8B		
4A	VREFB4A0	IO	CLK11n		DIFFIO_RX_B120n	DIFFOUT_B120n	AH7	DO16B	DO8B		
4A	VREFB4A0	IO	CLK11p		DIFFIO_RX_B120p	DIFFOUT_B120p	AJ7	DO16B	DO8B		
4A	VREFB4A0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B121n	DIFFOUT_B121n	AD6				
4A	VREFB4A0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B121p	DIFFOUT_B121p	AE6	DO17B		DO8B	
4A	VREFB4A0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B122n	DIFFOUT_B122n	AP3	DO17B	DO8B		
4A	VREFB4A0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B122p	DIFFOUT_B122p	AP4	DO17B	DO8B		
4A	VREFB4A0	IO			DIFFIO_TX_B123n	DIFFOUT_B123n	AH6				
4A	VREFB4A0	IO			DIFFIO_TX_B123p	DIFFOUT_B123p	AJ6	DO17B	DO8B		
4A	VREFB4A0	IO	CLK10n		DIFFIO_RX_B124n	DIFFOUT_B124n	AP2	DQSn17B/QK17B	DQSn8B/QK8B		
4A	VREFB4A0	IO	CLK10p		DIFFIO_RX_B124p	DIFFOUT_B124p	AN3	DQSn17B/CO17B/Con17B/QKn17B	DQSn8B/CO8B/Con8B/QKn8B		
4A	VREFB4A0	IO			DIFFIO_TX_B125n	DIFFOUT_B125n	AC7				
4A	VREFB4A0	IO			DIFFIO_TX_B125p	DIFFOUT_B125p	AC6	DO17B	DO8B		
4A	VREFB4A0	IO	CLK9n		DIFFIO_RX_B126n	DIFFOUT_B126n	AL4	DO17B	DO8B		
4A	VREFB4A0	IO	CLK9p		DIFFIO_RX_B126p	DIFFOUT_B126p	AL5	DO17B	DO8B		
4A	VREFB4A0	IO			DIFFIO_TX_B127n	DIFFOUT_B127n	AM3				
4A	VREFB4A0	IO	R20_1		DIFFIO_TX_B127p	DIFFOUT_B127p	AM6	DO17B	DO8B		
4A	VREFB4A0	IO	CLK8n		DIFFIO_RX_B128n	DIFFOUT_B128n	AF5	DO17B	DO8B		
4A	VREFB4A0	IO	CLK8p		DIFFIO_RX_B128p	DIFFOUT_B128p	AG6	DO17B	DO8B		
	RREF_BR						AM1				
	DNU						AM2				
	DNU						AM2				
GXB R0	REFCLK0Rp						AA8				
GXB R0	REFCLK0Rn						AA7				
GXB R0	GXB_RX_R0n,GXB_REFCLK_R0n						AK2				
GXB R0	GXB_RX_R0p,GXB_REFCLK_R0p						AK1				
GXB R0	GXB_TX_R0p						AJ3				
GXB R0	GXB_TX_R0n						AJ4				
GXB R0	GXB_RX_R1n,GXB_REFCLK_R1n						AH2				
GXB R0	GXB_RX_R1p,GXB_REFCLK_R1p						AH1				
GXB R0	GXB_TX_R1p						AG3				
GXB R0	GXB_TX_R1n						AG4				
GXB R0	GXB_RX_R2n,GXB_REFCLK_R2n						AF2				
GXB R0	GXB_RX_R2p,GXB_REFCLK_R2p						AF1				
GXB R0	GXB_TX_R2p						AE3				
GXB R0	GXB_TX_R2n						AE4				
GXB R0	GXB_RX_R3n,GXB_REFCLK_R3n						AD2				
GXB R0	GXB_RX_R3p,GXB_REFCLK_R3p						AD1				
GXB R0	GXB_TX_R3p						AC3				
GXB R0	GXB_TX_R3n						AC4				
GXB R0	GXB_RX_R4n,GXB_REFCLK_R4n						AB2				
GXB R0	GXB_RX_R4p,GXB_REFCLK_R4p						AB1				
GXB R0	GXB_TX_R4p						AA3				
GXB R0	GXB_TX_R4n						AA4				
GXB R0	GXB_RX_R5n,GXB_REFCLK_R5n						Y2				
GXB R0	GXB_RX_R5p,GXB_REFCLK_R5p						Y1				
GXB R0	GXB_TX_R5p						W3				
GXB R0	GXB_TX_R5n						W4				
GXB R0	REFCLK1Rp						W9				
GXB R0	REFCLK1Rn						W8				
GXB R1	REFCLK2Rp						U9				
GXB R1	REFCLK2Rn						U8				
GXB R1	GXB_RX_R6n,GXB_REFCLK_R6n						V2				
GXB R1	GXB_RX_R6p,GXB_REFCLK_R6p						V1				
GXB R1	GXB_TX_R6p						U3				
GXB R1	GXB_TX_R6n						U4				
GXB R1	GXB_RX_R7n,GXB_REFCLK_R7n						T2				
GXB R1	GXB_RX_R7p,GXB_REFCLK_R7p						T1				
GXB R1	GXB_TX_R7p						R3				
GXB R1	GXB_TX_R7n						R4				
GXB R1	GXB_RX_R8n,GXB_REFCLK_R8n						P2				
GXB R1	GXB_RX_R8p,GXB_REFCLK_R8p						P1				
GXB R1	GXB_TX_R8p						N3				
GXB R1	GXB_TX_R8n						N4				
GXB R1	GXB_RX_R9n,GXB_REFCLK_R9n						M2				
GXB R1	GXB_RX_R9p,GXB_REFCLK_R9p						M1				
GXB R1	GXB_TX_R9p						L3				
GXB R1	GXB_TX_R9n						L4				
GXB R1	GXB_RX_R10n,GXB_REFCLK_R10n						K2				
GXB R1	GXB_RX_R10p,GXB_REFCLK_R10p						K1				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
GXB_R1		GXB_TX_R10p					J3				
GXB_R1		GXB_TX_R10n					J4				
GXB_R1		GXB_RX_R11n,GXB_REFCLK_R11n					H2				
GXB_R1		GXB_RX_R11p,GXB_REFCLK_R11p					H1				
GXB_R1		GXB_TX_R11p					G3				
GXB_R1		GXB_TX_R11n					G4				
GXB_R1		REFCLK3Rp					R9				
GXB_R1		REFCLK3Rn					R8				
		DNU					K5				
		GND					H5				
7A	VREFB7A0	IO	CLK12p		DIFFIO_RX_T1p	DIFFOUT_T1p	E3	DO1T		DO1T	
7A	VREFB7A0	IO	CLK12n		DIFFIO_RX_T1n	DIFFOUT_T1n	E4	DO1T		DO1T	
7A	VREFB7A0	IO	RZQ_5		DIFFIO_TX_T2p	DIFFOUT_T2p	E1	DO1T		DO1T	
7A	VREFB7A0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	F1				
7A	VREFB7A0	IO	CLK13p		DIFFIO_RX_T3p	DIFFOUT_T3p	D1	DO1T		DO1T	
7A	VREFB7A0	IO	CLK13n		DIFFIO_RX_T3n	DIFFOUT_T3n	E2	DO1T		DO1T	
7A	VREFB7A0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	G6	DO1T		DO1T	
7A	VREFB7A0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	H6				
7A	VREFB7A0	IO	CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	G1	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T		
7A	VREFB7A0	IO	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	C2	DQSn1T/QK1T	DQSn1T/QK1T		
7A	VREFB7A0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	E5	DO1T		DO1T	
7A	VREFB7A0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	F6				
7A	VREFB7A0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FBn		DIFFIO_RX_T7p	DIFFOUT_T7p	C3	DO1T		DO1T	
7A	VREFB7A0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	D3	DO1T		DO1T	
7A	VREFB7A0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	J6	DO1T		DO1T	
7A	VREFB7A0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	K6				
7A	VREFB7A0	IO	CLK15p		DIFFIO_RX_T9p	DIFFOUT_T9p	A3	DO2T		DO1T	
7A	VREFB7A0	IO	CLK15n		DIFFIO_RX_T9n	DIFFOUT_T9n	B3	DO2T		DO1T	
7A	VREFB7A0	IO					L6	DO2T		DO1T	
7A	VREFB7A0	IO	VREFB7A0				M7				
7A	VREFB7A0	IO		DEV_OE	DIFFIO_RX_T10p	DIFFOUT_T10p	C6	DO2T		DO1T	
7A	VREFB7A0	IO		DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	D5	DO2T		DO1T	
7A	VREFB7A0	IO		nPERSTR0	DIFFIO_TX_T11p	DIFFOUT_T11p	A2	DO2T		DO1T	
7A	VREFB7A0	IO		nPERSTL0	DIFFIO_TX_T11n	DIFFOUT_T11n	B2				
7A	VREFB7A0	IO		C/P_CONFDONE	DIFFIO_RX_T12p	DIFFOUT_T12p	B5	DQS2T/CQ2T/CQn2T/QKn2T	DQS2T/CQ2T/CQn2T/QKn2T		
7A	VREFB7A0	IO		CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	C4	DQSn2T/QK2T	DQSn2T/QK2T		
7A	VREFB7A0	IO		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	A5	DO2T		DO1T	
7A	VREFB7A0	IO		PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	A4				
7A	VREFB7A0	IO		INIT_DONE	DIFFIO_RX_T14p	DIFFOUT_T14p	D6	DO2T		DO1T	
7A	VREFB7A0	IO		nCEO	DIFFIO_RX_T14n	DIFFOUT_T14n	E6	DO2T		DO1T	
7A	VREFB7A0	IO		PR_ERROR	DIFFIO_TX_T15p	DIFFOUT_T15p	J7	DO2T		DO1T	
7A	VREFB7A0	IO		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15n	K7				
7B	VREFB7B0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	K9	DO3T		DO2T	DO4_7B_0
7B	VREFB7B0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	K8	DO3T		DO2T	DO4_7B_1
7B	VREFB7B0	IO					M10	DO3T		DO2T	DO4_7B_2
7B	VREFB7B0	IO	VREFB7B0				P11				
7B	VREFB7B0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	C8	DO3T		DO2T	DO4_7B_3
7B	VREFB7B0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	D7	DO3T		DO2T	DO4_7B_4
7B	VREFB7B0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	E8	DO3T		DO2T	DO4_7B_5
7B	VREFB7B0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	F7				
7B	VREFB7B0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	N10	DQS3T/CQ3T/CQn3T/QKn3T	DQS3T/CQ3T/CQn3T/QKn3T	DO1T	DO34_7B
7B	VREFB7B0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	N11	DQSn3T/QK3T	DQSn3T/QK3T	DO1T	DO344_7B
7B	VREFB7B0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	G8	DO3T		DO2T	DO4_7B_7
7B	VREFB7B0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	G7				
7B	VREFB7B0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	H8	DO3T		DO2T	DO4_7B_6
7B	VREFB7B0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	J8	DO3T		DO2T	DO4_7B_7
7B	VREFB7B0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	L9	DO3T		DO2T	DO4_7B_8
7B	VREFB7B0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	M8				
7B	VREFB7B0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	B6	DO4T		DO2T	DO3_7B_0
7B	VREFB7B0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	C7	DO4T		DO2T	DO3_7B_1
7B	VREFB7B0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	E9	DO4T		DO2T	DO3_7B_2
7B	VREFB7B0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	F8				
7B	VREFB7B0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	A7	DO4T		DO2T	DO3_7B_3
7B	VREFB7B0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	A6	DO4T		DO2T	DO3_7B_4
7B	VREFB7B0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	G9	DO4T		DO2T	DO3_7B_5
7B	VREFB7B0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	H9				
7B	VREFB7B0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	D8	DQS4T/CQ4T/CQn4T/QKn4T	DQS4T/CQ4T/CQn4T/QKn4T	DO1T	DO33_7B
7B	VREFB7B0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	D9	DQSn4T/QK4T	DQSn4T/QK4T	DO1T	DO334_7B
7B	VREFB7B0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	A8	DO4T		DO2T	DO3_7B_6
7B	VREFB7B0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B8				
7B	VREFB7B0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	A10	DO4T		DO2T	DO3_7B_6
7B	VREFB7B0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	B9	DO4T		DO2T	DO3_7B_7
7B	VREFB7B0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	J10	DO4T		DO2T	DO3_7B_8
7B	VREFB7B0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	K10				
7C	VREFB7C0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F10	DO5T		DO3T	DO2_7C_0
7C	VREFB7C0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	G10	DO5T		DO3T	DO2_7C_1
7C	VREFB7C0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	J11	DO5T		DO3T	DO2_7C_2
7C	VREFB7C0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	K11				
7C	VREFB7C0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	G11	DO5T		DO3T	DO2_7C_3
7C	VREFB7C0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	H11	DO5T		DO3T	DO2_7C_4
7C	VREFB7C0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	K12	DO5T		DO3T	DO2_7C_5
7C	VREFB7C0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	L11				
7C	VREFB7C0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	E11	DQS5T/CQ5T/CQn5T/QKn5T	DQS5T/CQ5T/CQn5T/QKn5T	DO1T	DO32_7C
7C	VREFB7C0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	F11	DQSn5T/QK5T	DQSn5T/QK5T	DO1T	DO324_7C
7C	VREFB7C0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C10	DO5T		DO3T	DO2_7C_7
7C	VREFB7C0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D10				
7C	VREFB7C0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	G12	DO5T		DO3T	DO2_7C_6
7C	VREFB7C0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	H12	DO5T		DO3T	DO2_7C_7
7C	VREFB7C0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	L12	DO5T		DO3T	DO2_7C_8
7C	VREFB7C0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	M12				
7C	VREFB7C0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	A11	DO6T		DO3T	DO1_7C_0
7C	VREFB7C0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	B11	DO6T		DO3T	DO1_7C_1
7C	VREFB7C0	IO					M13	DO6T		DO3T	DO1_7C_2
7C	VREFB7C0	IO	VREFB7C0								
7C	VREFB7C0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	C11	DO6T		DO3T	DO1_7C_3
7C	VREFB7C0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	D11	DO6T		DO3T	DO1_7C_4
7C	VREFB7C0	IO			DIFFIO_TX_T41p	DIFFOUT_T41p	J13	DO6T		DO3T	DO1_7C_5
7C	VREFB7C0	IO			DIFFIO_TX_T41n	DIFFOUT_T41n	K13				
7C	VREFB7C0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	A13	DQS6T/CQ6T/CQn6T/QKn6T	DQS6T/CQ6T/CQn6T/QKn6T	DO1T	DQS1_7C



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F152	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 hard memory PHY (3)
7C	VREFB7CN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	B12	DQSn8T/QK6T	DQ3T	DO1T	DQSn7_C7C
7C	VREFB7CN0	IO			DIFFIO_TX_T43p	DIFFOUT_T43p	D12	DQ6T	DO3T	DO1T	DM1_C7C
7C	VREFB7CN0	IO			DIFFIO_TX_T43n	DIFFOUT_T43n	E12				
7C	VREFB7CN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	F13	DQ6T	DQ3T	DO1T	DO1_C7C_6
7C	VREFB7CN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	G13	DQ6T	DQ3T	DO1T	DO1_C7C_7
7C	VREFB7CN0	IO			DIFFIO_TX_T45p	DIFFOUT_T45p	H11	DQ6T	DQ3T	DO1T	DO1_C7C_8
7C	VREFB7CN0	IO			DIFFIO_TX_T45n	DIFFOUT_T45n	N12				RESETA_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	H14	DO7T	DO4T		CK_D7
7D	VREFB7DN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	J14	DO7T	DO4T		CKp_D7
7D	VREFB7DN0	IO			DIFFIO_TX_T47p	DIFFOUT_T47p	K14	DO7T	DO4T		CKE_D7_0
7D	VREFB7DN0	IO			DIFFIO_TX_T47n	DIFFOUT_T47n	L14				CKE_D7_1
7D	VREFB7DN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	F14	DO7T	DO4T		A_D7_0
7D	VREFB7DN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	G14	DO7T	DO4T		A_D7_1
7D	VREFB7DN0	IO			DIFFIO_TX_T49p	DIFFOUT_T49p	M14	DO7T	DO4T		A_D7_2
7D	VREFB7DN0	IO			DIFFIO_TX_T49n	DIFFOUT_T49n	M15				A_D7_3
7D	VREFB7DN0	IO			DIFFIO_RX_T50p	DIFFOUT_T50p	G15	DQSn7T/CQ7T/CQn7T/QKn7T	DQSn7T/CQ4T/CQn4T/QKn4T	DQSn7T/QK4T	A_D7_4
7D	VREFB7DN0	IO			DIFFIO_RX_T50n	DIFFOUT_T50n	H15	DQSn7T/QK7T	DQSn7T/QK4T	DQSn7T/QK4T	A_D7_5
7D	VREFB7DN0	IO			DIFFIO_TX_T51p	DIFFOUT_T51p	C13	DO7T	DO4T		A_D7_6
7D	VREFB7DN0	IO			DIFFIO_TX_T51n	DIFFOUT_T51n	D13				A_D7_7
7D	VREFB7DN0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	D14	DO7T	DO4T		A_D7_8
7D	VREFB7DN0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	E14	DO7T	DO4T		A_D7_9
7D	VREFB7DN0	IO			DIFFIO_TX_T53p	DIFFOUT_T53p	K15	DO7T	DO4T		A_D7_10
7D	VREFB7DN0	IO			DIFFIO_TX_T53n	DIFFOUT_T53n	L15				A_D7_11
7D	VREFB7DN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	B14	DQ8T	DO4T		A_D7_12
7D	VREFB7DN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	C14	DQ8T	DO4T		A_D7_13
7D	VREFB7DN0	IO	VREFB7DN0				N15	DQ8T	DO4T		A_D7_14
7D	VREFB7DN0	IO					N14				
7D	VREFB7DN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	A14	DQ8T	DO4T		BA_D7_0
7D	VREFB7DN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	B15	DQ8T	DO4T		BA_D7_1
7D	VREFB7DN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	D15	DQ8T	DO4T		BA_D7_2
7D	VREFB7DN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E15				RASB_D7
7D	VREFB7DN0	IO			DIFFIO_RX_T57p	DIFFOUT_T57p	F15	DQSn8T/CQ8T/CQn8T/QK8T	DO4T		CASB_D7
7D	VREFB7DN0	IO			DIFFIO_RX_T57n	DIFFOUT_T57n	G16	DQSn8T/QK8T	DO4T		WEA_D7
7D	VREFB7DN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	J16	DQ8T	DO4T		ODT_D7_0
7D	VREFB7DN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	K16				ODT_D7_1
7D	VREFB7DN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	C16	DQ8T	DO4T		A_D7_15
7D	VREFB7DN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	D16	DQ8T	DO4T		
7D	VREFB7DN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	M16	DQ8T	DO4T		CSW_D7_0
7D	VREFB7DN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	N16				CSW_D7_1
		VCCA_FPLL					R17				
		VCCD_FPLL					R16				
		DNU					L18				
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T61p	DIFFOUT_T61p	A16	DQ9T	DO5T		
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T61n	DIFFOUT_T61n	A17	DQ9T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	K17	DQ9T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	L17				
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T63p	DIFFOUT_T63p	K18	DQ9T	DO5T		
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T63n	DIFFOUT_T63n	K19	DQ9T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	D17	DQ9T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	E17				
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2_FPLL_TC_FBp_FPLL_TC_FBn		DIFFIO_RX_T65p	DIFFOUT_T65p	F17	DQSn9T/CQ9T/CQn9T/QK9n9T	DQSn9T/CQ5T/CQn5T/QK5n5T	DQSn9T/QK5T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3_FPLL_TC_FBn		DIFFIO_RX_T65n	DIFFOUT_T65n	G17	DQSn9T/QK9T	DQSn9T/QK5T	DQSn9T/QK5T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0_FPLL_TC_CLKOUT1_FPLL_TC_FBp		DIFFIO_TX_T66p	DIFFOUT_T66p	M17	DQ9T	DO5T		
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1_FPLL_TC_CLKOUTn		DIFFIO_TX_T66n	DIFFOUT_T66n	N17				
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T67p	DIFFOUT_T67p	H17	DQ9T	DO5T		
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T67n	DIFFOUT_T67n	J17	DQ9T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	B17	DQ9T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	C17				
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T69p	DIFFOUT_T69p	A19	DO10T	DO5T		
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T69n	DIFFOUT_T69n	A20	DO10T	DO5T		
8D	VREFB8DN0	IO					M18	DO10T	DO5T		
8D	VREFB8DN0	IO	VREFB8DN0				N18				
8D	VREFB8DN0	IO			DIFFIO_RX_T70p	DIFFOUT_T70p	C19	DO10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T70n	DIFFOUT_T70n	B18	DO10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T71p	DIFFOUT_T71p	G18	DO10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T71n	DIFFOUT_T71n	G19				
8D	VREFB8DN0	IO			DIFFIO_RX_T72p	DIFFOUT_T72p	H18	DQSn10T/CQ10T/CQn10T/QK10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T72n	DIFFOUT_T72n	J19	DQSn10T/QK10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T73p	DIFFOUT_T73p	M19	DO10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T73n	DIFFOUT_T73n	N19				
8D	VREFB8DN0	IO			DIFFIO_RX_T74p	DIFFOUT_T74p	D19	DO10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T74n	DIFFOUT_T74n	D18	DO10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T75p	DIFFOUT_T75p	E19	DO10T	DO5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T75n	DIFFOUT_T75n	F18				
8C	VREFB8CN0	IO			DIFFIO_RX_T76p	DIFFOUT_T76p	K20	DO11T	DO6T	DO2T	DO4_8C_0
8C	VREFB8CN0	IO			DIFFIO_RX_T76n	DIFFOUT_T76n	L20	DO11T	DO6T	DO2T	DO4_8C_1
8C	VREFB8CN0	IO					M20	DO11T	DO6T	DO2T	DO4_8C_2
8C	VREFB8CN0	IO	VREFB8CN0				N20				DO4_8C_3
8C	VREFB8CN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	A22	DO11T	DO6T	DO2T	DO4_8C_3
8C	VREFB8CN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	B21	DO11T	DO6T	DO2T	DO4_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	B20	DO11T	DO6T	DO2T	DO4_8C_5
8C	VREFB8CN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	C20				
8C	VREFB8CN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	D20	DQSn11T/CQ11T/CQn11T/QK11T	DQSn11T/CQ6T/CQn6T/QK6n6T	DO2T	DQSn4_8C
8C	VREFB8CN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	E20	DQSn11T/QK11T	DQSn11T/QK6T	DO2T	DQSn4_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	K21	DO11T	DO6T	DO2T	DM4_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	L21				
8C	VREFB8CN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	F20	DO11T	DO6T	DO2T	DO4_8C_6
8C	VREFB8CN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	G20	DO11T	DO6T	DO2T	DO4_8C_7
8C	VREFB8CN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	H20	DO11T	DO6T	DO2T	DO4_8C_8
8C	VREFB8CN0	IO			DIFFIO_TX_T82n	DIFFOUT_T82n	J20				
8C	VREFB8CN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	D21	DO12T	DO6T	DO2T	DO3_8C_0
8C	VREFB8CN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	E21	DO12T	DO6T	DO2T	DO3_8C_1
8C	VREFB8CN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	M21	DO12T	DO6T	DO2T	DO3_8C_2
8C	VREFB8CN0	IO			DIFFIO_TX_T84n	DIFFOUT_T84n	N21				
8C	VREFB8CN0	IO			DIFFIO_RX_T85p	DIFFOUT_T85p	C22	DO12T	DO6T	DO2T	DO3_8C_3
8C	VREFB8CN0	IO			DIFFIO_RX_T85n	DIFFOUT_T85n	D22	DO12T	DO6T	DO2T	DO3_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T86p	DIFFOUT_T86p	G21	DO12T	DO6T	DO2T	DO3_8C_5
8C	VREFB8CN0	IO			DIFFIO_TX_T86n	DIFFOUT_T86n	H21				
8C	VREFB8CN0	IO			DIFFIO_RX_T87p	DIFFOUT_T87p	F22	DQSn12T/CQ12T/CQn12T/QK12T	DO6T	DQSn12T/CQ2T/CQn2T/QK2T	DQSn3_8C



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
SC	VREFB8C0	IO			DIFFIO_RX_T87n	DIFFOUT_T87n	G22	DQSn12T/QK12T	DOE6	DQSn2T/QK2T	DQSn3_C8
SC	VREFB8C0	IO			DIFFIO_TX_T88p	DIFFOUT_T88p	M22	DO12T	DOE6	DO2T	DM3_C8
SC	VREFB8C0	IO			DIFFIO_TX_T88n	DIFFOUT_T88n	N22				
SC	VREFB8C0	IO			DIFFIO_RX_T89p	DIFFOUT_T89p	A23	DO12T	DOE6	DO2T	DO3_C8_6
SC	VREFB8C0	IO			DIFFIO_RX_T89n	DIFFOUT_T89n	B23	DO12T	DOE6	DO2T	DO3_C8_7
SC	VREFB8C0	IO			DIFFIO_TX_T90p	DIFFOUT_T90p	J23	DO12T	DOE6	DO2T	DO3_C8_8
SC	VREFB8C0	IO			DIFFIO_TX_T90n	DIFFOUT_T90n	K22				
SB	VREFB8B0	IO			DIFFIO_RX_T91p	DIFFOUT_T91p	H23	DO13T	DO7T	DO2T	DO2_BB_0
SB	VREFB8B0	IO			DIFFIO_RX_T91n	DIFFOUT_T91n	J23	DO13T	DO7T	DO2T	DO2_BB_1
SB	VREFB8B0	IO			DIFFIO_TX_T92p	DIFFOUT_T92p	K24	DO13T	DO7T	DO2T	DO2_BB_2
SB	VREFB8B0	IO			DIFFIO_TX_T92n	DIFFOUT_T92n	L24				
SB	VREFB8B0	IO			DIFFIO_RX_T93p	DIFFOUT_T93p	B24	DO13T	DO7T	DO2T	DO2_BB_3
SB	VREFB8B0	IO			DIFFIO_RX_T93n	DIFFOUT_T93n	C23	DO13T	DO7T	DO2T	DO2_BB_4
SB	VREFB8B0	IO			DIFFIO_TX_T94p	DIFFOUT_T94p	D23	DO13T	DO7T	DO2T	DO2_BB_5
SB	VREFB8B0	IO			DIFFIO_TX_T94n	DIFFOUT_T94n	E23				
SB	VREFB8B0	IO			DIFFIO_RX_T95p	DIFFOUT_T95p	F23	DQSn13T/CQ13T/CQn13T/QKn13T	DQSnT/CQnT/CQnT/QKnT	DO2T	DQSn2_BB
SB	VREFB8B0	IO			DIFFIO_RX_T95n	DIFFOUT_T95n	G23	DQSn13T/QK13T	DQSnT/QK1T	DO2T	DQSn2_BB
SB	VREFB8B0	IO			DIFFIO_TX_T96p	DIFFOUT_T96p	M23	DO13T	DO7T	DO2T	DM2_BB
SB	VREFB8B0	IO			DIFFIO_TX_T96n	DIFFOUT_T96n	N23				
SB	VREFB8B0	IO			DIFFIO_RX_T97p	DIFFOUT_T97p	D24	DO13T	DO7T	DO2T	DO2_BB_6
SB	VREFB8B0	IO			DIFFIO_RX_T97n	DIFFOUT_T97n	E24	DO13T	DO7T	DO2T	DO2_BB_7
SB	VREFB8B0	IO			DIFFIO_TX_T98p	DIFFOUT_T98p	K23	DO13T	DO7T	DO2T	DO2_BB_8
SB	VREFB8B0	IO			DIFFIO_TX_T98n	DIFFOUT_T98n	L23				
SB	VREFB8B0	IO			DIFFIO_RX_T99p	DIFFOUT_T99p	G24	DO14T	DO7T	DO2T	DO1_BB_0
SB	VREFB8B0	IO			DIFFIO_RX_T99n	DIFFOUT_T99n	H24	DO14T	DO7T	DO2T	DO1_BB_1
SB	VREFB8B0	IO	VREFB8B0				M24	DO14T	DO7T	DO2T	DO1_BB_2
SB	VREFB8B0	IO					N24				
SB	VREFB8B0	IO			DIFFIO_RX_T100p	DIFFOUT_T100p	A26	DO14T	DO7T	DO2T	DO1_BB_3
SB	VREFB8B0	IO			DIFFIO_RX_T100n	DIFFOUT_T100n	A25	DO14T	DO7T	DO2T	DO1_BB_4
SB	VREFB8B0	IO			DIFFIO_TX_T101p	DIFFOUT_T101p	C25	DO14T	DO7T	DO2T	DO1_BB_5
SB	VREFB8B0	IO			DIFFIO_TX_T101n	DIFFOUT_T101n	D25				
SB	VREFB8B0	IO			DIFFIO_RX_T102p	DIFFOUT_T102p	F25	DQSn14T/CQ14T/CQn14T/QKn14T	DO7T	DO2T	DQSn1_BB
SB	VREFB8B0	IO			DIFFIO_RX_T102n	DIFFOUT_T102n	G25	DQSn14T/QK14T	DO7T	DO2T	DQSn1_BB
SB	VREFB8B0	IO			DIFFIO_TX_T103p	DIFFOUT_T103p	M25	DO14T	DO7T	DO2T	DM1_BB
SB	VREFB8B0	IO			DIFFIO_TX_T103n	DIFFOUT_T103n	N25				
SB	VREFB8B0	IO			DIFFIO_RX_T104p	DIFFOUT_T104p	B26	DO14T	DO7T	DO2T	DO1_BB_6
SB	VREFB8B0	IO			DIFFIO_RX_T104n	DIFFOUT_T104n	C26	DO14T	DO7T	DO2T	DO1_BB_7
SB	VREFB8B0	IO			DIFFIO_TX_T105p	DIFFOUT_T105p	J25	DO14T	DO7T	DO2T	DO1_BB_8
SB	VREFB8B0	IO			DIFFIO_TX_T105n	DIFFOUT_T105n	K25				RESET#_8A
SA	VREFB8A0	IO			DIFFIO_RX_T106p	DIFFOUT_T106p	E26	DO15T	DO8T	DO8T	CK_8A
SA	VREFB8A0	IO			DIFFIO_RX_T106n	DIFFOUT_T106n	F26	DO15T	DO8T	DO8T	CK#_8A
SA	VREFB8A0	IO			DIFFIO_TX_T107p	DIFFOUT_T107p	K29	DO15T	DO8T	DO8T	CKE_8A_0
SA	VREFB8A0	IO			DIFFIO_TX_T107n	DIFFOUT_T107n	L29				CKE_8A_1
SA	VREFB8A0	IO			DIFFIO_RX_T108p	DIFFOUT_T108p	D26	DO15T	DO8T	DO8T	A_8A_0
SA	VREFB8A0	IO			DIFFIO_RX_T108n	DIFFOUT_T108n	E27	DO15T	DO8T	DO8T	A_8A_1
SA	VREFB8A0	IO			DIFFIO_TX_T109p	DIFFOUT_T109p	A27	DO15T	DO8T	DO8T	A_8A_2
SA	VREFB8A0	IO			DIFFIO_TX_T109n	DIFFOUT_T109n	B27				A_8A_3
SA	VREFB8A0	IO			DIFFIO_RX_T110p	DIFFOUT_T110p	G26	DQSn15T/CQ15T/CQn15T/QKn15T	DQSnT/CQnT/CQnT/QKnT	DO8T	A_8A_4
SA	VREFB8A0	IO			DIFFIO_RX_T110n	DIFFOUT_T110n	H26	DQSn15T/QK15T	DQSnT/QK8T	DO8T	A_8A_5
SA	VREFB8A0	IO			DIFFIO_TX_T111p	DIFFOUT_T111p	K27	DO15T	DO8T	DO8T	A_8A_6
SA	VREFB8A0	IO			DIFFIO_TX_T111n	DIFFOUT_T111n	L27				A_8A_7
SA	VREFB8A0	IO			DIFFIO_RX_T112p	DIFFOUT_T112p	D27	DO15T	DO8T	DO8T	A_8A_8
SA	VREFB8A0	IO			DIFFIO_RX_T112n	DIFFOUT_T112n	C28	DO15T	DO8T	DO8T	A_8A_9
SA	VREFB8A0	IO			DIFFIO_TX_T113p	DIFFOUT_T113p	C29	DO15T	DO8T	DO8T	A_8A_10
SA	VREFB8A0	IO			DIFFIO_TX_T113n	DIFFOUT_T113n	D28				A_8A_11
SA	VREFB8A0	IO			DIFFIO_RX_T114p	DIFFOUT_T114p	G27	DO16T	DO8T	DO8T	A_8A_12
SA	VREFB8A0	IO			DIFFIO_RX_T114n	DIFFOUT_T114n	G28	DO16T	DO8T	DO8T	A_8A_13
SA	VREFB8A0	IO			DIFFIO_TX_T115p	DIFFOUT_T115p	J26	DO16T	DO8T	DO8T	A_8A_14
SA	VREFB8A0	IO			DIFFIO_TX_T115n	DIFFOUT_T115n	K26				A_8A_15
SA	VREFB8A0	IO			DIFFIO_RX_T116p	DIFFOUT_T116p	A29	DO16T	DO8T	DO8T	BA_8A_0
SA	VREFB8A0	IO			DIFFIO_RX_T116n	DIFFOUT_T116n	A28	DO16T	DO8T	DO8T	BA_8A_1
SA	VREFB8A0	IO			DIFFIO_TX_T117p	DIFFOUT_T117p	B29	DO16T	DO8T	DO8T	BA_8A_2
SA	VREFB8A0	IO			DIFFIO_TX_T117n	DIFFOUT_T117n	B30				BA#_8A
SA	VREFB8A0	IO			DIFFIO_RX_T118p	DIFFOUT_T118p	F28	DQSn16T/CQ16T/CQn16T/QKn16T	DO8T	DO8T	CAS#_8A
SA	VREFB8A0	IO			DIFFIO_RX_T118n	DIFFOUT_T118n	F29	DQSn16T/QK16T	DO8T	DO8T	WE#_8A
SA	VREFB8A0	IO			DIFFIO_TX_T119p	DIFFOUT_T119p	H27	DO16T	DO8T	DO8T	ODT_8A_0
SA	VREFB8A0	IO			DIFFIO_TX_T119n	DIFFOUT_T119n	J27				ODT_8A_1
SA	VREFB8A0	IO	CLK23p		DIFFIO_RX_T120p	DIFFOUT_T120p	D29	DO16T	DO8T	DO8T	
SA	VREFB8A0	IO	CLK23n		DIFFIO_RX_T120n	DIFFOUT_T120n	E29	DO16T	DO8T	DO8T	
SA	VREFB8A0	IO			DIFFIO_TX_T121p	DIFFOUT_T121p	D30	DO16T	DO8T	DO8T	CS#_8A_0
SA	VREFB8A0	IO	CLK22p		DIFFIO_TX_T121n	DIFFOUT_T121n	E30				CS#_8A_1
SA	VREFB8A0	IO	CLK22n		DIFFIO_RX_T122p	DIFFOUT_T122p	G29	DO17T			
SA	VREFB8A0	IO	CLK22n		DIFFIO_RX_T122n	DIFFOUT_T122n	H29	DO17T			
SA	VREFB8A0	IO					L26	DO17T			
SA	VREFB8A0	IO	VREFB8A0				M27				
SA	VREFB8A0	IO	FPLL_TL_CLKOUT2_FPLL_TL_FBp,FPLL_TL_FBn		DIFFIO_RX_T123p	DIFFOUT_T123p	A31	DO17T			
SA	VREFB8A0	IO	FPLL_TL_CLKOUT3_FPLL_TL_FBp		DIFFIO_RX_T123n	DIFFOUT_T123n	A30	DO17T			
SA	VREFB8A0	IO	FPLL_TL_CLKOUT7_FPLL_TL_CLKOUT7p,FPLL_TL_FB0		DIFFIO_TL_T124p	DIFFOUT_T124p	C31	DO17T			
SA	VREFB8A0	IO	FPLL_TL_CLKOUT1_FPLL_TL_CLKOUT1n		DIFFIO_TX_T124n	DIFFOUT_T124n	D31				
SA	VREFB8A0	IO	CLK21p		DIFFIO_RX_T125p	DIFFOUT_T125p	A32	DQSn17T/CQ17T/CQn17T/QKn17T			
SA	VREFB8A0	IO	CLK21n		DIFFIO_RX_T125n	DIFFOUT_T125n	B32	DQSn17T/QK17T			
SA	VREFB8A0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	J28	DO17T			
SA	VREFB8A0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	K28				
SA	VREFB8A0	IO	CLK20p		DIFFIO_RX_T127p	DIFFOUT_T127p	D33	DO17T			
SA	VREFB8A0	IO	CLK20n		DIFFIO_RX_T127n	DIFFOUT_T127n	C32	DO17T			
SA	VREFB8A0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	D32	DO17T			
SA	VREFB8A0	IO	RZ0_6		DIFFIO_TX_T128n	DIFFOUT_T128n	E32				
SA		MSEL0		MSEL0							D34
SA		MSEL1		MSEL1							H30
SA		MSEL2		MSEL2							K30
SA		MSEL3		MSEL3							M29
SA		MSEL4		MSEL4							M30
SA		CONF_DONE		CONF_DONE							C34
SA		nSTATUS		nSTATUS							B34
SA		nCE		nCE							A33
SA		nCONFIG		nCONFIG							C33
		GND									B33
		GND									AA26
		GND									AA33



Note (1)

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		GND					AA34				
		GND					AB27				
		GND					AB28				
		GND					AB29				
		GND					AB30				
		GND					AB31				
		GND					AB32				
		GND					AC30				
		GND					AC33				
		GND					AC34				
		GND					AD31				
		GND					AD32				
		GND					AE30				
		GND					AE33				
		GND					AE34				
		GND					AF31				
		GND					AF32				
		GND					AG30				
		GND					AG33				
		GND					AG34				
		GND					AH31				
		GND					AH32				
		GND					AJ30				
		GND					AJ33				
		GND					AJ34				
		GND					AK31				
		GND					AK32				
		GND					AL33				
		GND					AL34				
		GND					E34				
		GND					F31				
		GND					F32				
		GND					G30				
		GND					G33				
		GND					G34				
		GND					H31				
		GND					H32				
		GND					J30				
		GND					J33				
		GND					J34				
		GND					K31				
		GND					K32				
		GND					L30				
		GND					L33				
		GND					L34				
		GND					M31				
		GND					M32				
		GND					N28				
		GND					N29				
		GND					N33				
		GND					N34				
		GND					P27				
		GND					P31				
		GND					P32				
		GND					R28				
		GND					R30				
		GND					R33				
		GND					R34				
		GND					T27				
		GND					T29				
		GND					T31				
		GND					T32				
		GND					U28				
		GND					U33				
		GND					U34				
		GND					V27				
		GND					V31				
		GND					V32				
		GND					W28				
		GND					W30				
		GND					W33				
		GND					W34				
		GND					Y27				
		GND					Y28				
		GND					Y31				
		GND					Y32				
		GND					AA1				
		GND					AA2				
		GND					AA8				
		GND					AB3				
		GND					AB4				
		GND					AB5				
		GND					AB7				
		GND					AB8				
		GND					AC1				
		GND					AC2				
		GND					AC5				
		GND					AD3				
		GND					AD4				
		GND					AE1				
		GND					AE2				
		GND					AE5				
		GND					AF3				
		GND					AF4				
		GND					AG1				
		GND					AG2				
		GND					AG5				
		GND					AH3				
		GND					AH4				





Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		GND					AJ1				
		GND					AJ2				
		GND					AJ5				
		GND					AK3				
		GND					AK4				
		GND					AL1				
		GND					AL2				
		GND					AL3				
		GND					AN1				
		GND					F3				
		GND					F4				
		GND					G1				
		GND					G2				
		GND					G5				
		GND					H3				
		GND					H4				
		GND					J1				
		GND					J2				
		GND					J5				
		GND					K3				
		GND					K4				
		GND					L1				
		GND					L2				
		GND					L5				
		GND					M3				
		GND					M4				
		GND					M5				
		GND					N1				
		GND					N2				
		GND					N6				
		GND					P3				
		GND					P4				
		GND					P8				
		GND					R1				
		GND					R2				
		GND					R5				
		GND					R7				
		GND					T3				
		GND					T4				
		GND					T6				
		GND					T8				
		GND					U1				
		GND					U2				
		GND					U7				
		GND					V3				
		GND					V4				
		GND					V6				
		GND					W1				
		GND					W2				
		GND					W5				
		GND					W7				
		GND					Y3				
		GND					Y4				
		GND					Y6				
		GND					Y8				
		VCCP					P18				
		VCCP					R13				
		VCCP					R21				
		VCCP					T10				
		VCCP					U25				
		VCCP					V10				
		VCCP					W25				
		VCCP					Y12				
		VCCP					Y19				
		VCCP					Y22				
		VCCA_FPLL					V26				
		VCCA_FPLL					V9				
		VCCA_FPLL					T26				
		VCCA_FPLL					T9				
		VCCBAT					M28				
		VCC_AUX					P12				
		VCC_AUX					P24				
		VCC_AUX					W11				
		VCC_AUX					Y24				
		VCCD_FPLL					Y26				
		VCCD_FPLL					Y9				
		VCCD_FPLL					P26				
		VCCA_GXBL0					P9				
		VCCA_GXBL0					Y28				
		VCCA_GXBL1					Y7				
		VCCA_GXBL1					T28				
		VCCA_GXBL1					T7				
		VCCCH_GXBL0					V28				
		VCCCH_GXBL0					V7				
		VCCCH_GXBL1					P28				
		VCCCH_GXBL1					P7				
		VCCCL_GXBL0					V29				
		VCCCL_GXBL0					V30				
		VCCCL_GXBL0					V5				
		VCCCL_GXBL0					V6				
		VCCCL_GXBL1					P29				
		VCCCL_GXBL1					P30				
		VCCCL_GXBL1					P5				
		VCCCL_GXBL1					P6				
		VCCR_GXBL					AA29				
		VCCR_GXBL					AA30				
		VCCR_GXBL					N30				
		VCCR_GXBL					U29				
		VCCR_GXBL					U30				



Note (1)

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		VCCR_GXBR					AA5				
		VCCR_GXBR					AA6				
		VCCR_GXBR					N5				
		VCCR_GXBR					U5				
		VCCR_GXBR					U6				
		VCCT_GXBL0					W29				
		VCCT_GXBL0					Y30				
		VCCT_GXBR0					W6				
		VCCT_GXBR0					Y5				
		VCCT_GXBL1					R29				
		VCCT_GXBL1					T30				
		VCCT_GXBR1					R6				
		VCCT_GXBR1					T5				
		VCC					R14				
		VCC					R15				
		VCC					R19				
		VCC					R23				
		VCC					R25				
		VCC					T12				
		VCC					T14				
		VCC					T16				
		VCC					T18				
		VCC					T20				
		VCC					T22				
		VCC					T24				
		VCC					U11				
		VCC					U12				
		VCC					U13				
		VCC					U15				
		VCC					U17				
		VCC					U19				
		VCC					U20				
		VCC					U21				
		VCC					U22				
		VCC					U23				
		VCC					V12				
		VCC					V14				
		VCC					V16				
		VCC					V20				
		VCC					V22				
		VCC					V24				
		VCC					W13				
		VCC					W15				
		VCC					W17				
		VCC					W19				
		VCC					W21				
		VCC					W23				
		VCC					Y13				
		VCC					Y20				
		VCC					V18				
		VCCIO3A					AD30				
		VCCIO3A					AF27				
		VCCIO3A					AH30				
		VCCIO3A					AJ27				
		VCCIO3A					AK30				
		VCCIO3A					AM27				
		VCCIO3B					AF24				
		VCCIO3B					AJ24				
		VCCIO3B					AM24				
		VCCIO3B					AP24				
		VCCIO3C					AF21				
		VCCIO3C					AJ21				
		VCCIO3C					AM21				
		VCCIO3C					AP21				
		VCCIO3D					AF18				
		VCCIO3D					AJ18				
		VCCIO3D					AM18				
		VCCIO3D					AP18				
		VCCIO4A					AD5				
		VCCIO4A					AF5				
		VCCIO4A					AH5				
		VCCIO4A					AM5				
		VCCIO4B					AF9				
		VCCIO4B					AJ9				
		VCCIO4B					AM9				
		VCCIO4B					AP9				
		VCCIO4C					AF12				
		VCCIO4C					AJ12				
		VCCIO4C					AM12				
		VCCIO4C					AP12				
		VCCIO4D					AF15				
		VCCIO4D					AJ15				
		VCCIO4D					AM15				
		VCCIO4D					AP15				
		VCCIO7A					C5				
		VCCIO7A					F2				
		VCCIO7A					F5				
		VCCIO7A					L7				
		VCCIO7B					A9				
		VCCIO7B					C9				
		VCCIO7B					F9				
		VCCIO7B					J9				
		VCCIO7C					A12				
		VCCIO7C					C12				
		VCCIO7C					F12				
		VCCIO7C					J12				
		VCCIO7D					A15				
		VCCIO7D					C15				
		VCCIO7D					F15				



Note (1)

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		VCCIO7D					J15				
		VCCIO8A					C27				
		VCCIO8A					C30				
		VCCIO8A					F27				
		VCCIO8A					F30				
		VCCIO8A					J29				
		VCCIO8A					M26				
		VCCIO8B					A24				
		VCCIO8B					C24				
		VCCIO8B					F24				
		VCCIO8B					J24				
		VCCIO8C					A21				
		VCCIO8C					C21				
		VCCIO8C					F21				
		VCCIO8C					J21				
		VCCIO8D					A18				
		VCCIO8D					C18				
		VCCIO8D					F18				
		VCCIO8D					J18				
		VCCPD3					AB26				
		VCCPD3					AC27				
		VCCPD3					Y21				
		VCCPD3					Y25				
		VCCPD4A					AB6				
		VCCPD4A					AB9				
		VCCPD4BCD					Y10				
		VCCPD4BCD					Y14				
		VCCPD4BCD					Y16				
		VCCPD7A					N8				
		VCCPD7A					N9				
		VCCPD7BCD					P14				
		VCCPD7BCD					P16				
		VCCPD7BCD					R11				
		VCCPD8					N26				
		VCCPD8					N27				
		VCCPD8					P20				
		VCCPD8					P22				
		VCCPGM					M9				
		VCCPGM					AC26				
		GND					AA11				
		GND					AA13				
		GND					AA16				
		GND					AA19				
		GND					AA22				
		GND					AA24				
		GND					AD10				
		GND					AD12				
		GND					AD16				
		GND					AD19				
		GND					AD22				
		GND					AD25				
		GND					AD28				
		GND					AD7				
		GND					AG10				
		GND					AG13				
		GND					AG16				
		GND					AG19				
		GND					AG22				
		GND					AG25				
		GND					AG28				
		GND					AG7				
		GND					AK10				
		GND					AK13				
		GND					AK16				
		GND					AK19				
		GND					AK22				
		GND					AK25				
		GND					AK28				
		GND					AK7				
		GND					AN10				
		GND					AN13				
		GND					AN16				
		GND					AN19				
		GND					AN22				
		GND					AN25				
		GND					AN28				
		GND					AN31				
		GND					AN4				
		GND					AN7				
		GND					B1				
		GND					B10				
		GND					B13				
		GND					B16				
		GND					B19				
		GND					B22				
		GND					B25				
		GND					B28				
		GND					B31				
		GND					B4				
		GND					B7				
		GND					D2				
		GND					D4				
		GND					E10				
		GND					E13				
		GND					E16				
		GND					E19				
		GND					E22				
		GND					E25				
		GND					E28				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		GND					E31				
		GND					E7				
		GND					H10				
		GND					H13				
		GND					H16				
		GND					H19				
		GND					H22				
		GND					H25				
		GND					H28				
		GND					H7				
		GND					L10				
		GND					L13				
		GND					L16				
		GND					L19				
		GND					L22				
		GND					L25				
		GND					L28				
		GND					L8				
		GND					M6				
		GND					N7				
		GND					P10				
		GND					P13				
		GND					P15				
		GND					P17				
		GND					P19				
		GND					P21				
		GND					P23				
		GND					P25				
		GND					R10				
		GND					R12				
		GND					R18				
		GND					R20				
		GND					R22				
		GND					R24				
		GND					T11				
		GND					T13				
		GND					T15				
		GND					T17				
		GND					T19				
		GND					T21				
		GND					T23				
		GND					T25				
		GND					U10				
		GND					U14				
		GND					U16				
		GND					U24				
		GND					V11				
		GND					V13				
		GND					V15				
		GND					V17				
		GND					V19				
		GND					V21				
		GND					V23				
		GND					V25				
		GND					W10				
		GND					W12				
		GND					W14				
		GND					W16				
		GND					W18				
		GND					W20				
		GND					W22				
		GND					W24				
		GND					U18				

Notes:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).
- (2) GXB\_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
- (3) RESET pin is only applicable for DDR3 device.



**Pin Information for the Arria® V 5AGXFA5 Device  
Version 1.3**

<b>Version Number</b>	<b>Date</b>	<b>Changes Made</b>
1.0	11/4/2011	Preliminary release.
1.1	1/3/2012	Split VCC to VCC and VCCP
1.2	1/23/2013	- Removed Preliminary - Rename the CQ and DQS pins in DQS and hard memory PHY columns
1.3	7/31/2015	Removed LPDDR2 hard memory PHY, RLDRAMII hard memory PHY, and QDRII hard memory PHY columns.