



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672 (3)	DQS for X8/X9	DQS for X16/ X18	DDR3/DDR2 Hard Memory PHY (4)
		DNU					C25			
		DNU					C25			
		RREF_TL					D26			
GXB L1		GXB TX_L8n					E23*			
GXB L1		GXB TX_L8p					E24*			
GXB L1		GXB RX_L8p,GXB_REFCLK_L8p					F26*			
GXB L1		GXB RX_L8n,GXB_REFCLK_L8n					F25*			
GXB L1		GXB TX_L7n					G23			
GXB L1		GXB TX_L7p					G24			
GXB L1		GXB RX_L7p,GXB_REFCLK_L7p					H26			
GXB L1		GXB RX_L7n,GXB_REFCLK_L7n					H25			
GXB L1		GXB TX_L6n					J23*			
GXB L1		GXB TX_L6p					J24*			
GXB L1		GXB RX_L6p,GXB_REFCLK_L6p					K26*			
GXB L1		GXB RX_L6n,GXB_REFCLK_L6n					K25*			
GXB L1		REFCLK2Ln					N19			
GXB L1		REFCLK2Lp					N18			
GXB L0		REFCLK1Lp					R19			
GXB L0		REFCLK1Lp					R18			
GXB L0		GXB TX_L5n					L23*			
GXB L0		GXB TX_L5p					L24*			
GXB L0		GXB RX_L5p,GXB_REFCLK_L5p					M26*			
GXB L0		GXB RX_L5n,GXB_REFCLK_L5n					M25*			
GXB L0		GXB TX_L4n					N23			
GXB L0		GXB TX_L4p					N24			
GXB L0		GXB RX_L4p,GXB_REFCLK_L4p					P26			
GXB L0		GXB RX_L4n,GXB_REFCLK_L4n					P25			
GXB L0		GXB TX_L3n					R23*			
GXB L0		GXB TX_L3p					R24*			
GXB L0		GXB RX_L3p,GXB_REFCLK_L3p					T26*			
GXB L0		GXB RX_L3n,GXB_REFCLK_L3n					T25*			
GXB L0		GXB TX_L2n					U23			
GXB L0		GXB TX_L2p					U24			
GXB L0		GXB RX_L2p,GXB_REFCLK_L2p					V26			
GXB L0		GXB RX_L2n,GXB_REFCLK_L2n					V25			
GXB L0		GXB TX_L1n					W23			
GXB L0		GXB TX_L1p					W24			
GXB L0		GXB RX_L1p,GXB_REFCLK_L1p					Y26			
GXB L0		GXB RX_L1n,GXB_REFCLK_L1n					Y25			
GXB L0		GXB TX_L0n					AA23			
GXB L0		GXB TX_L0p					AA24			
GXB L0		GXB RX_L0p,GXB_REFCLK_L0p					AB26			
GXB L0		GXB RX_L0n,GXB_REFCLK_L0n					AB25			
GXB L0		REFCLK0Ln					U19			
GXB L0		REFCLK0Lp					U18			
		DNU					V20			
3A		TDO		TDO			AE26			
3A		TMS		TMS			V22			
3A		TCK		TCK			AE24			
3A		TDI		TDI			AD24			
3A		DCLK		DCLK			AC23			
3A		nCS0		DATA4			AD26			
3A		AS_DATA3		DATA3			AD25			
3A		AS_DATA2		DATA2			AF25			
3A		AS_DATA1		DATA1			AE25			
3A		AS_DATA0,ASDO		DATA0			AF24			
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AA20			
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AB19	DO1B		
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AB21	DO1B		
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AC21	DO1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	Y21			
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AA21	DO1B		
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AC22	DQS1B/QK1B		
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AD22	DQS1B/CQ1B/CQn1B/QKn1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AD23			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AE23	DO1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AF22	DO1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AF23	DO1B		
3A	VREFB3AN0	IO	VREFB3AN0				V20			
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	Y19	DO1B		
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AF21	DO1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AC20			
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AD20			
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AF19			
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AF20			
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AC19			
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AD19			
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AE18			
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AF18			
3D	VREFB3DN0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AA18			
3D	VREFB3DN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AB18	DO2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AD18	DO2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AE18	DO2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	Y17			
3D	VREFB3DN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AA17	DO2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	W18	DQS2B/QK2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	Y18	DQS2B/CQ2B/CQn2B/QKn2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AC17			
3D	VREFB3DN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AD17	DO2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AB16	DO2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AC16	DO2B	DO1B	
3D	VREFB3DN0	IO	VREFB3DN0				Y16			
3D	VREFB3DN0	IO					AA16	DO2B	DO1B	
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B37n	DIFFOUT_B37n	V16	DO2B	DO1B	
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B37p	DIFFOUT_B37p	W16	DO2B	DO1B	
3D	VREFB3DN0	IO			DIFFIO_TX_B38n	DIFFOUT_B38n	AD16			
3D	VREFB3DN0	IO			DIFFIO_TX_B38p	DIFFOUT_B38p	AE16	DO3B	DO1B	
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B39n	DIFFOUT_B39n	AF15	DO3B	DO1B	



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672 (3)	DQS for X8/X9	DQS for X16/ X18	DDR3/DDR2 Hard Memory PHY (4)
3D	VREFB3DNO	IO	CLK6p		DIFFIO_RX_B39p	DIFFOUT_B39p	AF16	DQ3B	DQ1B	
3D	VREFB3DNO	IO	FPLL_BC_CLKOUT1_FPLL_BC_CLKOUTn		DIFFIO_TX_B40n	DIFFOUT_B40n	AA15			
3D	VREFB3DNO	IO	FPLL_BC_CLKOUT0_FPLL_BC_CLKOUTn_FPLL_BC_FB0		DIFFIO_TX_B40p	DIFFOUT_B40p	AB15	DQ3B	DQ1B	
3D	VREFB3DNO	IO	FPLL_BC_CLKOUT3_FPLL_BC_FBn		DIFFIO_RX_B41n	DIFFOUT_B41n	V15	DQS3B/QK3B	DQS1B/QK1B	
3D	VREFB3DNO	IO	FPLL_BC_CLKOUT2_FPLL_BC_FBp_FPLL_BC_FB1		DIFFIO_RX_B41p	DIFFOUT_B41p	W15	DQS3B/CQ3B/CQn3B/QKn3B	DQS1B/CO1B/COn1B/QKn1B	
3D	VREFB3DNO	IO			DIFFIO_TX_B42n	DIFFOUT_B42n	AD15			
3D	VREFB3DNO	IO			DIFFIO_TX_B42p	DIFFOUT_B42p	AE15	DQ3B	DQ1B	
3D	VREFB3DNO	IO	CLK6n		DIFFIO_RX_B43n	DIFFOUT_B43n	AC14	DQ3B	DQ1B	
3D	VREFB3DNO	IO	CLK6p		DIFFIO_RX_B43p	DIFFOUT_B43p	AD14	DQ3B	DQ1B	
3D	VREFB3DNO	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	Y14			
3D	VREFB3DNO	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AA14	DQ3B	DQ1B	
3D	VREFB3DNO	IO	CLK7n		DIFFIO_RX_B45n	DIFFOUT_B45n	AF14	DQ3B	DQ1B	
3D	VREFB3DNO	IO	CLK7p		DIFFIO_RX_B45p	DIFFOUT_B45p	AF13	DQ3B	DQ1B	
		VCCD_FPLL					U13			
		VCCA_FPLL					U14			
		DNU					V13			
4D	VREFB4DNO	IO			DIFFIO_TX_B46n	DIFFOUT_B46n	V13			CS# 4D_1
4D	VREFB4DNO	IO			DIFFIO_TX_B46p	DIFFOUT_B46p	W13	DQ4B	DQ2B	CS# 4D_0
4D	VREFB4DNO	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	AB13	DQ4B	DQ2B	
4D	VREFB4DNO	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	AC13	DQ4B	DQ2B	
4D	VREFB4DNO	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	Y13			A_4D_15
4D	VREFB4DNO	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AA13	DQ4B	DQ2B	ODT 4D_1
4D	VREFB4DNO	IO			DIFFIO_RX_B49n	DIFFOUT_B49n	AD13	DQS4B/QK4B	DQ2B	QDT 4D_0
4D	VREFB4DNO	IO			DIFFIO_RX_B49p	DIFFOUT_B49p	AE13	DQS4B/CQ4B/CO4B/QK4B	DQ2B	WE# 4D
4D	VREFB4DNO	IO			DIFFIO_TX_B50n	DIFFOUT_B50n	V12			CAS# 4D
4D	VREFB4DNO	IO			DIFFIO_TX_B50p	DIFFOUT_B50p	W12	DQ4B	DQ2B	RAS# 4D
4D	VREFB4DNO	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	AD12	DQ4B	DQ2B	BA_4D_2
4D	VREFB4DNO	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	AE12	DQ4B	DQ2B	BA_4D_1
4D	VREFB4DNO	IO	VREFB4DNO				AA12			BA_4D_0
4D	VREFB4DNO	IO					AB12	DQ4B	DQ2B	
4D	VREFB4DNO	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AF12	DQ4B	DQ2B	A_4D_14
4D	VREFB4DNO	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AF11	DQ4B	DQ2B	A_4D_13
4D	VREFB4DNO	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AC11			A_4D_12
4D	VREFB4DNO	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AD11	DQ5B	DQ2B	A_4D_11
4D	VREFB4DNO	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AC10	DQ5B	DQ2B	A_4D_10
4D	VREFB4DNO	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AD10	DQ5B	DQ2B	A_4D_9
4D	VREFB4DNO	IO			DIFFIO_TX_B55n	DIFFOUT_B55n	Y11			A_4D_8
4D	VREFB4DNO	IO			DIFFIO_TX_B55p	DIFFOUT_B55p	AA11	DQ5B	DQ2B	A_4D_7
4D	VREFB4DNO	IO			DIFFIO_RX_B56n	DIFFOUT_B56n	AE10	DQS5B/QK5B	DQ2B	A_4D_6
4D	VREFB4DNO	IO			DIFFIO_RX_B56p	DIFFOUT_B56p	AF9	DQS5B/CQ5B/CO5B/QK5B	DQS2B/CO2B/CQn2B/QKn2B	A_4D_5
4D	VREFB4DNO	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AD9			A_4D_4
4D	VREFB4DNO	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AE9	DQ5B	DQ2B	A_4D_3
4D	VREFB4DNO	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	V10	DQ5B	DQ2B	A_4D_2
4D	VREFB4DNO	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	W10	DQ5B	DQ2B	A_4D_1
4D	VREFB4DNO	IO			DIFFIO_TX_B59n	DIFFOUT_B59n	Y10			CKE_4D_1
4D	VREFB4DNO	IO			DIFFIO_TX_B59p	DIFFOUT_B59p	AA10	DQ5B	DQ2B	CKE_4D_0
4D	VREFB4DNO	IO			DIFFIO_RX_B60n	DIFFOUT_B60n	AB9	DQ5B	DQ2B	CK# 4D
4C	VREFB4CNO	IO			DIFFIO_RX_B60p	DIFFOUT_B60p	AC9	DQ5B	DQ2B	CK 4D
4C	VREFB4CNO	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	V9			RESET# 4D
4C	VREFB4CNO	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	W9	DQ6B	DQ3B	DQ1_4C_8
4C	VREFB4CNO	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AC8	DQ6B	DQ3B	DQ1_4C_7
4C	VREFB4CNO	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AD8	DQ6B	DQ3B	DQ1_4C_6
4C	VREFB4CNO	IO			DIFFIO_TX_B63n	DIFFOUT_B63n	Y9			
4C	VREFB4CNO	IO			DIFFIO_TX_B63p	DIFFOUT_B63p	AA9	DQ6B	DQ3B	DM1_4C
4C	VREFB4CNO	IO			DIFFIO_RX_B64n	DIFFOUT_B64n	AF8	DQS6B/QK6B	DQ3B	DQS#1_4C
4C	VREFB4CNO	IO			DIFFIO_RX_B64p	DIFFOUT_B64p	AF7	DQS6B/CQ6B/CO6B/QK6B	DQ3B	DQS1_4C
4C	VREFB4CNO	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AE6			
4C	VREFB4CNO	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AF6	DQ6B	DQ3B	DQ1_4C_5
4C	VREFB4CNO	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AC7	DQ6B	DQ3B	DQ1_4C_4
4C	VREFB4CNO	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AD7	DQ6B	DQ3B	DQ1_4C_3
4C	VREFB4CNO	IO	VREFB4CNO				Y8			
4C	VREFB4CNO	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AA8	DQ6B	DQ3B	DQ1_4C_2
4C	VREFB4CNO	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AF5	DQ6B	DQ3B	DQ1_4C_1
4C	VREFB4CNO	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AD6	DQ6B	DQ3B	DQ1_4C_0
4C	VREFB4CNO	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AE6			
4C	VREFB4CNO	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AC5	DQ7B	DQ3B	DQ2_4C_8
4C	VREFB4CNO	IO			DIFFIO_RX_B69n	DIFFOUT_B69n	AE3	DQ7B	DQ3B	DQ2_4C_7
4C	VREFB4CNO	IO			DIFFIO_RX_B69p	DIFFOUT_B69p	AF3	DQ7B	DQ3B	DQ2_4C_6
4C	VREFB4CNO	IO			DIFFIO_TX_B70n	DIFFOUT_B70n	Y7			
4C	VREFB4CNO	IO			DIFFIO_TX_B70p	DIFFOUT_B70p	AA7	DQ7B	DQ3B	DM2_4C
4C	VREFB4CNO	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	AD5	DQS7B/QK7B	DQS#2_4C	
4C	VREFB4CNO	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AD4	DQS7B/CQ7B/CO7B/QKn7B	DQS3B/CO3B/COn3B/QKn3B	DQS2_4C
4C	VREFB4CNO	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AC3			
4C	VREFB4CNO	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AD3	DQ7B	DQ3B	DQ2_4C_5
4C	VREFB4CNO	IO			DIFFIO_RX_B73n	DIFFOUT_B73n	AB2	DQ7B	DQ3B	DQ2_4C_4
4C	VREFB4CNO	IO			DIFFIO_RX_B73p	DIFFOUT_B73p	AC1	DQ7B	DQ3B	DQ2_4C_3
4C	VREFB4CNO	IO			DIFFIO_TX_B74n	DIFFOUT_B74n	AB6			
4C	VREFB4CNO	IO			DIFFIO_TX_B74p	DIFFOUT_B74p	AC6	DQ7B	DQ3B	DQ2_4C_2
4C	VREFB4CNO	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AB4	DQ7B	DQ3B	DQ2_4C_1
4C	VREFB4CNO	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AB3	DQ7B	DQ3B	DQ2_4C_0
4A	VREFB4ANO	IO		DATA10	DIFFIO_TX_B83n	DIFFOUT_B83n	AA1			
4A	VREFB4ANO	IO		DATA11	DIFFIO_TX_B83p	DIFFOUT_B83p	AB1	DQ8B		
4A	VREFB4ANO	IO		DATA5	DIFFIO_RX_B84n	DIFFOUT_B84n	Y1	DQ8B		
4A	VREFB4ANO	IO		DATA6	DIFFIO_RX_B84p	DIFFOUT_B84p	AA2	DQ8B		
4A	VREFB4ANO	IO		DATA12	DIFFIO_TX_B85n	DIFFOUT_B85n	W7			
4A	VREFB4ANO	IO		DATA13	DIFFIO_TX_B85p	DIFFOUT_B85p	W6	DQ8B		
4A	VREFB4ANO	IO		DATA7	DIFFIO_RX_B86n	DIFFOUT_B86n	AA3	DQS#8B/QK8B		
4A	VREFB4ANO	IO		DATA8	DIFFIO_RX_B86p	DIFFOUT_B86p	AA4	DQS#8B/CQ8B/CO8B/QKn8B		
4A	VREFB4ANO	IO		DATA14	DIFFIO_TX_B87n	DIFFOUT_B87n	AA5			
4A	VREFB4ANO	IO		DATA15	DIFFIO_TX_B87p	DIFFOUT_B87p	AA6	DQ8B		
4A	VREFB4ANO	IO		DATA9	DIFFIO_RX_B88n	DIFFOUT_B88n	Y5	DQ8B		
4A	VREFB4ANO	IO		CLKUSR	DIFFIO_RX_B88p	DIFFOUT_B88p	Y4	DQ8B		
4A	VREFB4ANO	IO	VREFB4ANO				V7			
4A	VREFB4ANO	IO	RZQ_1				W6	DQ8B		
4A	VREFB4ANO	IO			DIFFIO_RX_B89n	DIFFOUT_B89n	W3	DQ8B		
4A	VREFB4ANO	IO			DIFFIO_RX_B89p	DIFFOUT_B89p	W4	DQ8B		
		RREF_BR					AE1			
		DNU					AD1			
		DNU					AD2			



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672 (3)	DQS for X8/X9	DQS for X16/ X18	DDR3/DDR2 Hard Memory PHY (4)
5A	VREFB5A0	IO					W1	DQ1R	DQ1R	
5A	VREFB5A0	IO					V1	DQ1R	DQ1R	
5A	VREFB5A0	IO					T7	DQ1R	DQ1R	
5A	VREFB5A0	IO	VREFB5A0				U7			
5A	VREFB5A0	IO					V4	DQ1R	DQ1R	
5A	VREFB5A0	IO					V5	DQ1R	DQ1R	
5A	VREFB5A0	IO					W2	DQ1R	DQ1R	
5A	VREFB5A0	IO					V2			
5A	VREFB5A0	IO					V3	DQS1R/CO1R/CO1R/OQk1R	DQS1R/CO1R/CO1R/OQk1R	
5A	VREFB5A0	IO					U3	DQS1R/OQK1R	DQS1R/OQK1R	
5A	VREFB5A0	IO					U6	DQ1R	DQ1R	
5A	VREFB5A0	IO					U6			
5A	VREFB5A0	IO					T1	DQ1R	DQ1R	
5A	VREFB5A0	IO					U1	DQ1R	DQ1R	
5A	VREFB5A0	IO					T3	DQ1R	DQ1R	
5A	VREFB5A0	IO					T4			
5A	VREFB5A0	IO					T2	DQ2R	DQ1R	
5A	VREFB5A0	IO					R3	DQ2R	DQ1R	
5A	VREFB5A0	IO					T6	DQ2R	DQ1R	
5A	VREFB5A0	IO					R5			
5A	VREFB5A0	IO					P1	DQ2R	DQ1R	
5A	VREFB5A0	IO					R2	DQ2R	DQ1R	
5A	VREFB5A0	IO					P3	DQ2R	DQ1R	
5A	VREFB5A0	IO					P4			
5A	VREFB5A0	IO	CLK15p				N2	DQS2R/CO2R/CO2R/OQk2R	DQ1R	
5A	VREFB5A0	IO	CLK15n				N3	DQS2R/OQK2R	DQ1R	
5A	VREFB5A0	IO					R6	DQ2R	DQ1R	
5A	VREFB5A0	IO					P6			
5A	VREFB5A0	IO	CLK14p				M1	DQ2R	DQ1R	
5A	VREFB5A0	IO	CLK14n				N1	DQ2R	DQ1R	
5A	VREFB5A0	IO					N5	DQ2R	DQ1R	
5A	VREFB5A0	IO					N6			
6A	VREFB6A0	IO	CLK13p				M2	DQ3R	DQ2R	
6A	VREFB6A0	IO	CLK13n				L1	DQ3R	DQ2R	
6A	VREFB6A0	IO					M3	DQ3R	DQ2R	
6A	VREFB6A0	IO					M4			
6A	VREFB6A0	IO	CLK12p				H1	DQ3R	DQ2R	
6A	VREFB6A0	IO	CLK12n				J1	DQ3R	DQ2R	
6A	VREFB6A0	IO					L3	DQ3R	DQ2R	
6A	VREFB6A0	IO					L4			
6A	VREFB6A0	IO	FPLL_RC_CLKOUT2:FPLL_RC_FBn:FPLL_RC_FB1				K2	DQS3R/CO3R/CO3R/OQk3R	DQS2R/CO2R/CO2R/OQk2R	
6A	VREFB6A0	IO	FPLL_RC_CLKOUT3:FPLL_RC_FBn				K3	DQS3R/OQK3R	DQS2R/OQK2R	
6A	VREFB6A0	IO	FPLL_RC_CLKOUT0:FPLL_RC_CLKOUTp:FPLL_RC_FB0				M6	DQ3R	DQ2R	
6A	VREFB6A0	IO	FPLL_RC_CLKOUT1:FPLL_RC_CLKOUTn				L6			
6A	VREFB6A0	IO					J2	DQ3R	DQ2R	
6A	VREFB6A0	IO					J3	DQ3R	DQ2R	
6A	VREFB6A0	IO					F1	DQ3R	DQ2R	
6A	VREFB6A0	IO					E1			
6A	VREFB6A0	IO					F2	DQ4R	DQ2R	
6A	VREFB6A0	IO					G2	DQ4R	DQ2R	
6A	VREFB6A0	IO					K4	DQ4R	DQ2R	
6A	VREFB6A0	IO	VREFB6A0				K5			
6A	VREFB6A0	IO					G3	DQ4R	DQ2R	
6A	VREFB6A0	IO					H3	DQ4R	DQ2R	
6A	VREFB6A0	IO					J4	DQ4R	DQ2R	
6A	VREFB6A0	IO					J5			
6A	VREFB6A0	IO					D1	DQS4R/CO4R/CO4R/OQk4R	DQ2R	
6A	VREFB6A0	IO					D2	DQS4R/OQK4R	DQ2R	
6A	VREFB6A0	IO					K6	DQ4R	DQ2R	
6A	VREFB6A0	IO					K7			
6A	VREFB6A0	IO					E3	DQ4R	DQ2R	
6A	VREFB6A0	IO					F3	DQ4R	DQ2R	
6A	VREFB6A0	IO					B1	DQ4R	DQ2R	
6A	VREFB6A0	IO					C1			
7A		DNU					H6			
7A		GND					G5			
7A	VREFB7A0	IO					F4	DQ1T		
7A	VREFB7A0	IO					G4	DQ1T		
7A	VREFB7A0	IO					J6	DQ1T		
7A	VREFB7A0	IO	VREFB7A0				J7			
7A	VREFB7A0	IO					C3	DQ1T		
7A	VREFB7A0	IO					C2	DQ1T		
7A	VREFB7A0	IO	RZQ 5				G6	DQ1T		
7A	VREFB7A0	IO					F6			
7A	VREFB7A0	IO	MPERSTL0				A2	DQS1T/CO1T/CO1T/OQk1T		
7A	VREFB7A0	IO	OP_CONF_DONE				A3	DQS1T/OQK1T		
7A	VREFB7A0	IO	CRC_ERROR				D4	DQ1T		
7A	VREFB7A0	IO	PR_DONE				E4			
7A	VREFB7A0	IO	PR_REQUEST				C4	DQ1T		
7A	VREFB7A0	IO	INIT_DONE				B3	DQ1T		
7A	VREFB7A0	IO	PCEO				A4	DQ1T		
7A	VREFB7A0	IO	PR_ERROR				B4			
7A	VREFB7A0	IO	PR_READY				D6	DQ2T	DQ1T	DQ2_7C_0
7C	VREFB7C0	IO					E6	DQ2T	DQ1T	DQ2_7C_1
7C	VREFB7C0	IO					J9	DQ2T	DQ1T	DQ2_7C_2
7C	VREFB7C0	IO					J8			
7C	VREFB7C0	IO					E7	DQ2T	DQ1T	DQ2_7C_3
7C	VREFB7C0	IO					F7	DQ2T	DQ1T	DQ2_7C_4
7C	VREFB7C0	IO					C5	DQ2T	DQ1T	DQ2_7C_5
7C	VREFB7C0	IO					D5			
7C	VREFB7C0	IO					A5	DQS2T/CO2T/CO2T/OQk2T	DQS1T/CO1T/CO1T/OQk1T	DQS2_7C
7C	VREFB7C0	IO					A6	DQS2T/OQK2T	DQS1T/OQK1T	DQS2_7C
7C	VREFB7C0	IO					F8	DQ2T	DQ1T	DM2_7C
7C	VREFB7C0	IO					G8			
7C	VREFB7C0	IO					B6	DQ2T	DQ1T	DQ2_7C_6
7C	VREFB7C0	IO					C6	DQ2T	DQ1T	DQ2_7C_7
7C	VREFB7C0	IO					B7	DQ2T	DQ1T	DQ2_7C_8
7C	VREFB7C0	IO					C7			
7C	VREFB7C0	IO					G9	DQ3T	DQ1T	DQ1_7C_0



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672 (3)	DQS for X8/X9	DQS for X16/ X18	DDR3/DDR2 Hard Memory PHY (4)
7C	VREFB7CN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	H9	DQ3T	DQ1T	DQ1_7C_1
7C	VREFB7CN0	IO					E10	DQ3T	DQ1T	DQ1_7C_2
7C	VREFB7CN0	IO	VREFB7CN0				F10			
7C	VREFB7CN0	IO			DIFFIO_RX_T24p	DIFFOUT_T24p	C8	DQ3T	DQ1T	DQ1_7C_3
7C	VREFB7CN0	IO			DIFFIO_RX_T24n	DIFFOUT_T24n	D8	DQ3T	DQ1T	DQ1_7C_4
7C	VREFB7CN0	IO			DIFFIO_TX_T25p	DIFFOUT_T25p	A8	DQ3T	DQ1T	DQ1_7C_5
7C	VREFB7CN0	IO			DIFFIO_TX_T25n	DIFFOUT_T25n	A9			
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	D9	DQS3T/CO3T/COh3T/OKh3T	DQ1T	DQS#1_7C
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	E9	DQS#3T/OK3T	DQ1T	
7C	VREFB7CN0	IO			DIFFIO_TX_T27p	DIFFOUT_T27p	J10	DQ3T	DQ1T	DM1_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T27n	DIFFOUT_T27n	K10			
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T28p	G10	DQ3T	DQ1T	DQ1_7C_6
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T28n	H10	DQ3T	DQ1T	DQ1_7C_7
7C	VREFB7CN0	IO			DIFFIO_TX_T29p	DIFFOUT_T29p	B9	DQ3T	DQ1T	DQ1_7C_8
7C	VREFB7CN0	IO			DIFFIO_TX_T29n	DIFFOUT_T29n	C9			RESET#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T30p	DIFFOUT_T30p	B10	DQ4T	DQ2T	CK_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T30n	DIFFOUT_T30n	C10	DQ4T	DQ2T	CK#_7D
7D	VREFB7DN0	IO			DIFFIO_TX_T31p	DIFFOUT_T31p	F11	DQ4T	DQ2T	CKE_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T31n	DIFFOUT_T31n	G11			CKE_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T32p	DIFFOUT_T32p	J11	DQ4T	DQ2T	A_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	K12	DQ4T	DQ2T	A_7D_1
7D	VREFB7DN0	IO			DIFFIO_TX_T33p	DIFFOUT_T33p	C11	DQ4T	DQ2T	A_7D_2
7D	VREFB7DN0	IO			DIFFIO_TX_T33n	DIFFOUT_T33n	D11			A_7D_3
7D	VREFB7DN0	IO			DIFFIO_RX_T34p	DIFFOUT_T34p	A11	DQS4T/CO4T/COh4T/OKh4T	DQS2T/CO2T/COh2T/OKh2T	A_7D_4
7D	VREFB7DN0	IO			DIFFIO_RX_T34n	DIFFOUT_T34n	A12	DQS#4T/OK4T	DQS#2T/OK2T	A_7D_5
7D	VREFB7DN0	IO			DIFFIO_TX_T35p	DIFFOUT_T35p	F12	DQ4T	DQ2T	A_7D_6
7D	VREFB7DN0	IO			DIFFIO_TX_T35n	DIFFOUT_T35n	G12			A_7D_7
7D	VREFB7DN0	IO			DIFFIO_RX_T36p	DIFFOUT_T36p	H12	DQ4T	DQ2T	A_7D_8
7D	VREFB7DN0	IO			DIFFIO_RX_T36n	DIFFOUT_T36n	J12	DQ4T	DQ2T	A_7D_9
7D	VREFB7DN0	IO			DIFFIO_TX_T37p	DIFFOUT_T37p	D12	DQ4T	DQ2T	A_7D_10
7D	VREFB7DN0	IO			DIFFIO_TX_T37n	DIFFOUT_T37n	E12			A_7D_11
7D	VREFB7DN0	IO			DIFFIO_RX_T38p	DIFFOUT_T38p	B12	DQ5T	DQ2T	A_7D_12
7D	VREFB7DN0	IO			DIFFIO_RX_T38n	DIFFOUT_T38n	C12	DQ5T	DQ2T	A_7D_13
7D	VREFB7DN0	IO	VREFB7DN0				G13	DQ5T	DQ2T	A_7D_14
7D	VREFB7DN0	IO					H13			
7D	VREFB7DN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	A13	DQ5T	DQ2T	BA_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	B13	DQ5T	DQ2T	BA_7D_1
7D	VREFB7DN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C14	DQ5T	DQ2T	BA_7D_2
7D	VREFB7DN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	D14			RAS#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T41p	DIFFOUT_T41p	D13	DQS5T/CO5T/COh5T/OKh5T	DQ2T	CAS#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T41n	DIFFOUT_T41n	E13	DQS#5T/OK5T	DQ2T	WE#_7D
7D	VREFB7DN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	F14	DQ5T	DQ2T	ODT_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	G14			ODT_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	A15	DQ5T	DQ2T	A_7D_15
7D	VREFB7DN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	A14	DQ5T	DQ2T	
7D	VREFB7DN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	J13	DQ5T	DQ2T	CS#_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	J14			CS#_7D_1
		VCCA_FPLL					L13			
		VCCD_FPLL					L12			
		DNU					K14			
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T45p	DIFFOUT_T45p	G15	DQ6T	DQ3T	
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T45n	DIFFOUT_T45n	H15	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	J15	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	K15			
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T47p	DIFFOUT_T47p	B15	DQ6T	DQ3T	
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T47n	DIFFOUT_T47n	C15	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	D15	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	E15			
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2_FPLL_TC_Fb0_FPLL_TC_FB1		DIFFIO_RX_T49p	DIFFOUT_T49p	H16	DQS6T/CO6T/COh6T/OKh6T	DQS3T/CO3T/COh3T/OKh3T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3_FPLL_TC_Fb0		DIFFIO_RX_T49n	DIFFOUT_T49n	J16	DQS#6T/OK6T	DQS#3T/OK3T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0_FPLL_TC_CLKOUTp_FPLL_TC_FB0		DIFFIO_TX_T50p	DIFFOUT_T50p	F16	DQ6T	DQ3T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1_FPLL_TC_CLKOUTn		DIFFIO_TX_T50n	DIFFOUT_T50n	G16			
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T51p	DIFFOUT_T51p	A17	DQ6T	DQ3T	
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T51n	DIFFOUT_T51n	A16	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	D16	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	E16			
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T53p	DIFFOUT_T53p	B16	DQ7T	DQ3T	
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T53n	DIFFOUT_T53n	C17	DQ7T	DQ3T	
8D	VREFB8DN0	IO					F17	DQ7T	DQ3T	
8D	VREFB8DN0	IO	VREFB8DN0				G17			
8D	VREFB8DN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	J17	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	K17	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T55p	DIFFOUT_T55p	J18	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T55n	DIFFOUT_T55n	K18			
8D	VREFB8DN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	D17	DQS7T/CO7T/COh7T/OKh7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T56n	DIFFOUT_T56n	C18	DQS#7T/OK7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	E18	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T57n	DIFFOUT_T57n	F18			
8D	VREFB8DN0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	G18	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T58n	DIFFOUT_T58n	H18	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	B18	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T59n	DIFFOUT_T59n	A19			
8A	VREFB8AN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	C19			
8A	VREFB8AN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	D19			
8A	VREFB8AN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	E19			
8A	VREFB8AN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	F19			
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T81p	DIFFOUT_T81p	A20			
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T81n	DIFFOUT_T81n	B19			
8A	VREFB8AN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	A21			
8A	VREFB8AN0	IO			DIFFIO_TX_T82n	DIFFOUT_T82n	A22			
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T83p	DIFFOUT_T83p	B21	DQ8T		
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T83n	DIFFOUT_T83n	C21	DQ8T		
8A	VREFB8AN0	IO					F20	DQ8T		
8A	VREFB8AN0	IO	VREFB8AN0		DIFFIO_TX_T84p	DIFFOUT_T84p	G20			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2_FPLL_TL_Fb0_FPLL_TL_FB1		DIFFIO_RX_T84n	DIFFOUT_T84n	C20	DQ8T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3_FPLL_TL_Fb0		DIFFIO_RX_T84n	DIFFOUT_T84n	D20	DQ8T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0_FPLL_TL_CLKOUTp_FPLL_TL_FB0		DIFFIO_TX_T85p	DIFFOUT_T85p	G21	DQ8T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1_FPLL_TL_CLKOUTn		DIFFIO_TX_T85n	DIFFOUT_T85n	H21			
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T86p	DIFFOUT_T86p	B22	DQS8T/CO8T/COh8T/OKh8T		



Pin Information for the Arria® V 5AGTMC3 Device
Version 1.1
Note (1)

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672 (3)	DQS for X8/X9	DQS for X16/ X18	DDR3/DDR2 Hard Memory PHY (4)
8A	VREFB8A0	IO	CLK21n		DIFFIO_RX_T86n	DIFFOUT_T86n	A23	DQS#8T/QK8T		
8A	VREFB8A0	IO			DIFFIO_TX_T87p	DIFFOUT_T87p	H19	DQ#8T		
8A	VREFB8A0	IO			DIFFIO_TX_T87n	DIFFOUT_T87n	J19			
8A	VREFB8A0	IO	CLK20p		DIFFIO_RX_T88p	DIFFOUT_T88p	C23	DQ#8T		
8A	VREFB8A0	IO	CLK20n		DIFFIO_RX_T88n	DIFFOUT_T88n	C22	DQ#8T		
8A	VREFB8A0	IO			DIFFIO_TX_T89p	DIFFOUT_T89p	D21	DQ#8T		
8A	VREFB8A0	IO	RZQ_6		DIFFIO_TX_T89n	DIFFOUT_T89n	E21	DQ#8T		
8A		MSEL0		MSEL0			A24			
8A		MSEL1		MSEL1			K20			
8A		MSEL2		MSEL2			A25			
8A		MSEL3		MSEL3			B24			
8A		MSEL4		MSEL4			B25			
8A		CONF_DONE		CONF_DONE			F22			
8A		nSTATUS		nSTATUS			J20			
8A		nCE		nCE			H22			
8A		nCONFIG		nCONFIG			C24			
8A		GND					B26			
		GND					AA22			
		GND					AA25			
		GND					AA26			
		GND					AB23			
		GND					AB24			
		GND					AC24			
		GND					AC25			
		GND					AC26			
		GND					C26			
		GND					D23			
		GND					D24			
		GND					E22			
		GND					E25			
		GND					E26			
		GND					F23			
		GND					F24			
		GND					G22			
		GND					G25			
		GND					G26			
		GND					H23			
		GND					H24			
		GND					J22			
		GND					J25			
		GND					J26			
		GND					K23			
		GND					K24			
		GND					L19			
		GND					L20			
		GND					L22			
		GND					L25			
		GND					L26			
		GND					M19			
		GND					M23			
		GND					M24			
		GND					N20			
		GND					N22			
		GND					N25			
		GND					N26			
		GND					P19			
		GND					P23			
		GND					P24			
		GND					R20			
		GND					R22			
		GND					R25			
		GND					R26			
		GND					T19			
		GND					T21			
		GND					T23			
		GND					T24			
		GND					U20			
		GND					U25			
		GND					U26			
		GND					V18			
		GND					V19			
		GND					V21			
		GND					V22			
		GND					V23			
		GND					V24			
		GND					W22			
		GND					W26			
		GND					W26			
		GND					Y23			
		GND					Y24			
		VCCP					L11			
		VCCP					L15			
		VCCP					L9			
		VCCP					M8			
		VCCP					N17			
		VCCP					R17			
		VCCP					T8			
		VCCP					U11			
		VCCP					U15			
		VCCP					U9			
		VCCA_FPLL					P18			
		VCCA_FPLL					P7			
		VCCA_FPLL					M18			
		VCCBAT					J21			
		VCC_AUX					L10			
		VCC_AUX					L17			
		VCC_AUX					U10			
		VCC_AUX					U17			
		VCCD_FPLL					T18			



Bank Number	VREF	PinNameFunction (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672 (3)	DQS for X8/X9	DQS for X16/ X18	DDR3/DDR2 Hard Memory PHY (4)
		VCCD_FPLL					N7			
		VCCD_FPLL					L18			
		VCCA_GXBL0					T20			
		VCCA_GXBL1					M20			
		VCCCH_GXBL0					P20			
		VCCCH_GXBL1					L21			
		VCCL_GXBL0					P21			
		VCCL_GXBL0					P22			
		VCCL_GXBL1					K22			
		VCCR_GXBL					K21			
		VCCR_GXBL					N21			
		VCCR_GXBL					U21			
		VCCR_GXBL					U22			
		VCCT_GXBL0					R21			
		VCCT_GXBL0					T22			
		VCCT_GXBL1					M21			
		VCCT_GXBL1					M22			
		VCC					M10			
		VCC					M12			
		VCC					M14			
		VCC					M16			
		VCC					M17			
		VCC					N13			
		VCC					N15			
		VCC					N9			
		VCC					P10			
		VCC					P14			
		VCC					P16			
		VCC					P9			
		VCC					R11			
		VCC					R13			
		VCC					R15			
		VCC					R9			
		VCC					T10			
		VCC					T12			
		VCC					T14			
		VCC					T16			
		VCC					P12			
		VCCIO3A					AA19			
		VCCIO3A					AB22			
		VCCIO3A					AD21			
		VCCIO3D					AC15			
		VCCIO3D					AC18			
		VCCIO3D					AF17			
		VCCIO3D					Y15			
		VCCIO4A					Y3			
		VCCIO4A					Y6			
		VCCIO4C					AB7			
		VCCIO4C					AC4			
		VCCIO4C					AE7			
		VCCIO4C					AF4			
		VCCIO4D					AB10			
		VCCIO4D					AC12			
		VCCIO4D					AF10			
		VCCIO4D					Y12			
		VCCIO5A					N4			
		VCCIO5A					R1			
		VCCIO5A					R4			
		VCCIO5A					U4			
		VCCIO6A					G1			
		VCCIO6A					K1			
		VCCIO6A					M5			
		VCCIO6A					H4			
		VCCIO7A					D3			
		VCCIO7A					F5			
		VCCIO7C					A7			
		VCCIO7C					D7			
		VCCIO7C					F9			
		VCCIO7C					G7			
		VCCIO7D					A10			
		VCCIO7D					C13			
		VCCIO7D					D10			
		VCCIO7D					F13			
		VCCIO8A					O22			
		VCCIO8A					F21			
		VCCIO8A					G19			
		VCCIO8D					A18			
		VCCIO8D					C16			
		VCCIO8D					D18			
		VCCIO8D					F15			
		VCCPD3					V17			
		VCCPD3					W19			
		VCCPD4A					V8			
		VCCPD4BCD					U12			
		VCCPD4BCD					V11			
		VCCPD5					R7			
		VCCPD5					P8			
		VCCPD6					M7			
		VCCPD6					L7			
		VCCPD7A					K8			
		VCCPD7BCD					K13			
		VCCPD7BCD					K9			
		VCCPD8					K16			
		VCCPD8					K19			
		VCCPGM					H7			
		VCCPGM					W21			
		GND					AB11			
		GND					AB14			
		GND					AB17			



Pin Information for the Arria® V 5AGTMC3 Device
Version 1.1
Note (1)

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672 (3)	DQS for X8/X9	DQS for X16/ X18	DDR3/DDR2 Hard Memory PHY (4)
		GND					AB20			
		GND					AB5			
		GND					AB8			
		GND					AC2			
		GND					AE11			
		GND					AE14			
		GND					AE17			
		GND					AE2			
		GND					AE20			
		GND					AE22			
		GND					AE5			
		GND					AE8			
		GND					AF2			
		GND					B11			
		GND					B14			
		GND					B17			
		GND					B2			
		GND					B20			
		GND					B23			
		GND					B5			
		GND					B8			
		GND					E11			
		GND					E14			
		GND					E17			
		GND					E2			
		GND					E20			
		GND					E5			
		GND					E8			
		GND					H11			
		GND					H14			
		GND					H17			
		GND					H2			
		GND					H20			
		GND					H5			
		GND					H8			
		GND					K11			
		GND					L14			
		GND					L16			
		GND					L2			
		GND					L5			
		GND					L8			
		GND					M11			
		GND					M13			
		GND					M15			
		GND					M17			
		GND					M9			
		GND					N10			
		GND					N14			
		GND					N16			
		GND					N8			
		GND					P11			
		GND					P13			
		GND					P15			
		GND					P17			
		GND					P2			
		GND					P5			
		GND					R10			
		GND					R12			
		GND					R14			
		GND					R16			
		GND					R8			
		GND					T11			
		GND					T13			
		GND					T15			
		GND					T17			
		GND					T5			
		GND					T9			
		GND					U16			
		GND					U2			
		GND					U8			
		GND					W11			
		GND					W14			
		GND					W17			
		GND					W20			
		GND					W5			
		GND					W8			
		GND					Y2			
		GND					N12			

Notes:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).
- (2) The GXB_REFCLK pin is not supported in the current Quartus II version, but will be supported in the future Quartus II release version.
- (3) Pins with * are with reference to the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).
- (4) The RESET pin is only applicable for DDR3 devices.



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (3, 4)	DQS for X8/X9 (5)	DQS for X16/X18	DDR3/DDR2 Hard Memory PHY (6)	Board Connection Requirement for Pin Migration Only
		DNU					E29				
		DNU					F28				
		RREF_TL					F30				
GXB_L1		GXB_TX_L8n					G27*				
GXB_L1		GXB_TX_L8p					G28*				
GXB_L1		GXB_RX_L8p.GXB_REFCLK_L8p					H30*				
GXB_L1		GXB_RX_L8n.GXB_REFCLK_L8n					H29*				
GXB_L1		GXB_TX_L7n					J27				
GXB_L1		GXB_TX_L7p					J28				
GXB_L1		GXB_RX_L7p.GXB_REFCLK_L7p					K30				
GXB_L1		GXB_RX_L7n.GXB_REFCLK_L7n					K29				
GXB_L1		GXB_TX_L6n					L27*				
GXB_L1		GXB_TX_L6p					L28*				
GXB_L1		GXB_RX_L6p.GXB_REFCLK_L6p					M30*				
GXB_L1		GXB_RX_L6n.GXB_REFCLK_L6n					M29*				
GXB_L1		REFCLK2Ln					R23				
GXB_L1		REFCLK2Lp					R22				
GXB_L0		REFCLK1Ln					U23				
GXB_L0		REFCLK1Lp					U22				
GXB_L0		GXB_TX_L5n					N27*				
GXB_L0		GXB_TX_L5p					N28*				
GXB_L0		GXB_RX_L5p.GXB_REFCLK_L5p					P30*				
GXB_L0		GXB_RX_L5n.GXB_REFCLK_L5n					P29*				
GXB_L0		GXB_TX_L4n					R27				
GXB_L0		GXB_TX_L4p					R28				
GXB_L0		GXB_RX_L4p.GXB_REFCLK_L4p					T30				
GXB_L0		GXB_RX_L4n.GXB_REFCLK_L4n					T29				
GXB_L0		GXB_TX_L3n					U27*				
GXB_L0		GXB_TX_L3p					U28*				
GXB_L0		GXB_RX_L3p.GXB_REFCLK_L3p					V30*				
GXB_L0		GXB_RX_L3n.GXB_REFCLK_L3n					V29*				
GXB_L0		GXB_TX_L2n					W27				
GXB_L0		GXB_TX_L2p					W28				
GXB_L0		GXB_RX_L2p.GXB_REFCLK_L2p					Y30				
GXB_L0		GXB_RX_L2n.GXB_REFCLK_L2n					Y29				
GXB_L0		GXB_TX_L1n					AA27				
GXB_L0		GXB_TX_L1p					AA28				
GXB_L0		GXB_RX_L1p.GXB_REFCLK_L1p					AB29*				
GXB_L0		GXB_RX_L1n.GXB_REFCLK_L1n					AB28				
GXB_L0		GXB_TX_L0n					AC27				
GXB_L0		GXB_TX_L0p					AC28				
GXB_L0		GXB_RX_L0p.GXB_REFCLK_L0p					AD30				
GXB_L0		GXB_RX_L0n.GXB_REFCLK_L0n					AD29				
GXB_L0		REFCLK0Ln					W23				
GXB_L0		REFCLK0Lp					W22				
		DNU					AB26				
3A		TDO		TDO			AF30				
3A		TMS		TMS			AG30				
3A		TCK		TCK			AG29				
3A		TDI		TDI			AF29				
3A		DCLK		DCLK			AJ29				
3A		ACS0		DATA4			AA26				
3A		AS_DATA3		DATA3			AH30				
3A		AS_DATA2		DATA2			AJ30				
3A		AS_DATA1		DATA1			AK29				
3A		AS_DATA0.ASIO		DATA0			AK28				
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AF28				
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AG28	DQ1B			
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AF27	DQ1B			
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AG27	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	AE27				
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AE28	DQ1B			
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AH28	DQS1B/OK1B			
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AJ28	DQS1B/CQ1B/CQn1B/QKn1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1.FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AJ27				
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0.FPLL_BL_CLKOUTp.FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AK27	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3.FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AB25	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2.FPLL_BL_FBp.FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AC25	DQ1B			
3A	VREFB3AN0	IO	VREFB3AN0				AD25				
3A	VREFB3AN0	IO					AE25	DQ1B			
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AG28	DQ1B			
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AH26	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AK26				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AK25	DQ2B			
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AF25	DQ2B			
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AG25	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AB23				
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AB24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AH25	DQS2B/OK2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AJ25	DQS2B/CQ2B/CQn2B/QKn2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AC24				
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AD24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AF24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AG24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AC23				
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AE23	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AJ24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AK24	DQ2B			
3D	VREFB3DN0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AC22				DQ1B
3D	VREFB3DN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AC23				DQ1B
3D	VREFB3DN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AA22	DQ3B			DQ1B
3D	VREFB3DN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AB22	DQ3B			DQ1B
3D	VREFB3DN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AB21				DQ1B
3D	VREFB3DN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AC21	DQ3B			DQ1B
3D	VREFB3DN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AG23	DQS3B/OK3B			DQ1B
3D	VREFB3DN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AH23	DQS3B/CQ3B/CQn3B/QKn3B			DQ1B
3D	VREFB3DN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AD21				DQ1B
3D	VREFB3DN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AE22	DQ3B			DQ1B
3D	VREFB3DN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AF22	DQ3B			DQ1B
3D	VREFB3DN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AG22	DQ3B			DQ1B
3D	VREFB3DN0	IO	VREFB3DN0				AA21				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (3), (4)	DQS for X8/X9 (5)	DQS for X16/X18	DDR3/DDR2 Hard Memory PHY (6)	Board Connection Requirement for Pin Migration Only
3D	VREFB3DN0	IO					Y20	DQ3B	DQ1B		
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B37n	DIFFOUT_B37n	AH22	DQ3B	DQ1B		
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B37p	DIFFOUT_B37p	AJ22	DQ3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_TX_B38n	DIFFOUT_B38n	AD20				
3D	VREFB3DN0	IO			DIFFIO_TX_B38p	DIFFOUT_B38p	AE20				
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B39n	DIFFOUT_B39n	AJ21	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B39p	DIFFOUT_B39p	AG21	DQ4B	DQ1B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1_FPLL_BC_CLKOUTn		DIFFIO_TX_B40n	DIFFOUT_B40n	AA19				
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0_FPLL_BC_CLKOUTp_FPLL_BC_FB0		DIFFIO_TX_B40p	DIFFOUT_B40p	AB19	DQ4B	DQ1B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3_FPLL_BC_FBn		DIFFIO_RX_B41n	DIFFOUT_B41n	AG20	DQ5nB/QK4B	DQ3nB/QK1B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2_FPLL_BC_FBp_FPLL_BC_FB1		DIFFIO_RX_B41p	DIFFOUT_B41p	AA20	DQ5nB/CQ4B/CQn4B/QKn4B	DQ51B/CQ1B/CQn1B/QKn1B		
3D	VREFB3DN0	IO			DIFFIO_TX_B42n	DIFFOUT_B42n	AA20				
3D	VREFB3DN0	IO			DIFFIO_TX_B42p	DIFFOUT_B42p	AB20	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B43n	DIFFOUT_B43n	AJ21	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B43p	DIFFOUT_B43p	AK22	DQ4B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AC19				
3D	VREFB3DN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AD19	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B45n	DIFFOUT_B45n	AK20	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B45p	DIFFOUT_B45p	AK21	DQ4B	DQ1B		
			VCCD_FPLL				W15				
			VCCA_FPLL				W16				
			DNJ				Y16				
4D	VREFB4DN0	IO			DIFFIO_TX_B46n	DIFFOUT_B46n	AJ19			CS#_4D_1	
4D	VREFB4DN0	IO			DIFFIO_TX_B46p	DIFFOUT_B46p	AK18	DQ5B	DQ2B	CS#_4D_0	
4D	VREFB4DN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	AF19	DQ5B	DQ2B		
4D	VREFB4DN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	AG19	DQ5B	DQ2B	A_4D_15	
4D	VREFB4DN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AC18			ODT_4D_1	
4D	VREFB4DN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AD18	DQ5B	DQ2B	ODT_4D_0	
4D	VREFB4DN0	IO			DIFFIO_RX_B49n	DIFFOUT_B49n	AH19	DQ5nB/QK5B	DQ2B	WE#_4D	
4D	VREFB4DN0	IO			DIFFIO_RX_B49p	DIFFOUT_B49p	AH18	DQ5nB/CQ5B/CQn5B/QKn5B	DQ2B	CAS#_4D	
4D	VREFB4DN0	IO			DIFFIO_TX_B50n	DIFFOUT_B50n	AA18			RAS#_4D	
4D	VREFB4DN0	IO			DIFFIO_TX_B50p	DIFFOUT_B50p	AB18	DQ5B	DQ2B	BA_4D_2	
4D	VREFB4DN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	AF18	DQ5B	DQ2B	BA_4D_1	
4D	VREFB4DN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	AG18	DQ5B	DQ2B	BA_4D_0	
4D	VREFB4DN0	IO	VREFB4DN0				AD17				
4D	VREFB4DN0	IO					AE17	DQ5B	DQ2B	A_4D_14	
4D	VREFB4DN0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AA17	DQ5B	DQ2B	A_4D_13	
4D	VREFB4DN0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AB17	DQ5B	DQ2B	A_4D_12	
4D	VREFB4DN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AA16			A_4D_11	
4D	VREFB4DN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AB16	DQ6B	DQ2B	A_4D_10	
4D	VREFB4DN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AG17	DQ6B	DQ2B	A_4D_9	
4D	VREFB4DN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AH17	DQ6B	DQ2B	A_4D_8	
4D	VREFB4DN0	IO			DIFFIO_TX_B55n	DIFFOUT_B55n	AC16			A_4D_7	
4D	VREFB4DN0	IO			DIFFIO_TX_B55p	DIFFOUT_B55p	AD16	DQ6B	DQ2B	A_4D_6	
4D	VREFB4DN0	IO			DIFFIO_RX_B56n	DIFFOUT_B56n	AJ18	DQ5nB/QK6B	DQ3nB/QK2B	A_4D_5	
4D	VREFB4DN0	IO			DIFFIO_RX_B56p	DIFFOUT_B56p	AK17	DQ5nB/CQ6B/CQn6B/QKn6B	DQ32B/CQ2B/CQn2B/QKn2B	A_4D_4	
4D	VREFB4DN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AF16			A_4D_3	
4D	VREFB4DN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AG16	DQ6B	DQ2B	A_4D_2	
4D	VREFB4DN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AA15	DQ6B	DQ2B	A_4D_1	
4D	VREFB4DN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AB15	DQ6B	DQ2B	A_4D_0	
4D	VREFB4DN0	IO			DIFFIO_TX_B59n	DIFFOUT_B59n	AC15			CKE_4D_1	
4D	VREFB4DN0	IO			DIFFIO_TX_B59p	DIFFOUT_B59p	AD15	DQ6B	DQ2B	CKE_4D_0	
4D	VREFB4DN0	IO			DIFFIO_RX_B60n	DIFFOUT_B60n	AJ16	DQ6B	DQ2B	CKE_4D	
4D	VREFB4DN0	IO			DIFFIO_RX_B60p	DIFFOUT_B60p	AK16	DQ6B	DQ2B	CK_4D	
4C	VREFB4CN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AA14			RESE#_4D	
4C	VREFB4CN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AB14	DQ7B	DQ3B	DQ1_4C_8	
4C	VREFB4CN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AG15	DQ7B	DQ3B	DQ1_4C_7	
4C	VREFB4CN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AH15	DQ7B	DQ3B	DQ1_4C_6	
4C	VREFB4CN0	IO			DIFFIO_TX_B63n	DIFFOUT_B63n	AE15				
4C	VREFB4CN0	IO			DIFFIO_TX_B63p	DIFFOUT_B63p	AF15	DQ7B	DQ3B	DM1_4C	
4C	VREFB4CN0	IO			DIFFIO_RX_B64n	DIFFOUT_B64n	AJ15	DQ5nB/QK7B	DQ3B	DQ5nB_4C	
4C	VREFB4CN0	IO			DIFFIO_RX_B64p	DIFFOUT_B64p	AK14	DQ5nB/CQ7B/CQn7B/QKn7B	DQ3B	DQ51_4C	
4C	VREFB4CN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AG14				
4C	VREFB4CN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AH14	DQ7B	DQ3B	DQ1_4C_5	
4C	VREFB4CN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AD13	DQ7B	DQ3B	DQ1_4C_4	
4C	VREFB4CN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AE13	DQ7B	DQ3B	DQ1_4C_3	
4C	VREFB4CN0	IO	VREFB4CN0				AD14				
4C	VREFB4CN0	IO					AE14	DQ7B	DQ3B	DQ1_4C_2	
4C	VREFB4CN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AH13	DQ7B	DQ3B	DQ1_4C_1	
4C	VREFB4CN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AJ13	DQ7B	DQ3B	DQ1_4C_0	
4C	VREFB4CN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AC13				
4C	VREFB4CN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AD12	DQ8B	DQ3B	DQ2_4C_8	
4C	VREFB4CN0	IO			DIFFIO_RX_B69n	DIFFOUT_B69n	AF12	DQ8B	DQ3B	DQ2_4C_7	
4C	VREFB4CN0	IO			DIFFIO_RX_B69p	DIFFOUT_B69p	AG12	DQ8B	DQ3B	DQ2_4C_6	
4C	VREFB4CN0	IO			DIFFIO_TX_B70n	DIFFOUT_B70n	AA13				
4C	VREFB4CN0	IO			DIFFIO_TX_B70p	DIFFOUT_B70p	AB13	DQ8B	DQ3B	DM2_4C	
4C	VREFB4CN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	AG12	DQ5nB/QK8B	DQ3nB/QK3B	DQ5nB_4C	
4C	VREFB4CN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AH12	DQ5nB/CQ8B/CQn8B/QKn8B	DQ35B/CQ3B/CQn3B/QKn3B	DQ52_4C	
4C	VREFB4CN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AJ12				
4C	VREFB4CN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AK12	DQ8B	DQ3B	DQ2_4C_5	
4C	VREFB4CN0	IO			DIFFIO_RX_B73n	DIFFOUT_B73n	AB12	DQ8B	DQ3B	DQ2_4C_4	
4C	VREFB4CN0	IO			DIFFIO_RX_B73p	DIFFOUT_B73p	AC12	DQ8B	DQ3B	DQ2_4C_3	
4C	VREFB4CN0	IO			DIFFIO_TX_B74n	DIFFOUT_B74n	Y12				
4C	VREFB4CN0	IO			DIFFIO_TX_B74p	DIFFOUT_B74p	Y13	DQ8B	DQ3B	DQ2_4C_2	
4C	VREFB4CN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AG11	DQ8B	DQ3B	DQ2_4C_1	
4C	VREFB4CN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AH11	DQ8B	DQ3B	DQ2_4C_0	
4B	VREFB4BN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AD11				
4B	VREFB4BN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AE11	DQ9B		DQ3_4B_8	
4B	VREFB4BN0	IO			DIFFIO_RX_B77n	DIFFOUT_B77n	AA12	DQ9B		DQ3_4B_7	
4B	VREFB4BN0	IO			DIFFIO_RX_B77p	DIFFOUT_B77p	AB11	DQ9B		DQ3_4B_6	
4B	VREFB4BN0	IO			DIFFIO_TX_B78n	DIFFOUT_B78n	AA11				
4B	VREFB4BN0	IO			DIFFIO_TX_B78p	DIFFOUT_B78p	AA10	DQ9B		DM3_4B	
4B	VREFB4BN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AK11	DQ5nB/QK9B		DQ5nB_4B	
4B	VREFB4BN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AK10	DQ5nB/CQ9B/CQn9B/QKn9B		DQ53_4B	
4B	VREFB4BN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AF10				
4B	VREFB4BN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AG10	DQ9B		DQ3_4B_5	
4B	VREFB4BN0	IO			DIFFIO_RX_B81n	DIFFOUT_B81n	AB10	DQ9B		DQ3_4B_4	
4B	VREFB4BN0	IO	VREFB4BN0		DIFFIO_RX_B81p	DIFFOUT_B81p	AB9	DQ9B		DQ3_4B_3	
4B	VREFB4BN0	IO					AD9				
4B	VREFB4BN0	IO					AD10	DQ9B		DQ3_4B_2	
4B	VREFB4BN0	IO			DIFFIO_RX_B82n	DIFFOUT_B82n	AH9	DQ9B		DQ3_4B_1	



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (3), (4)	DQS for X8/X9 (5)	DQS for X16/X18	DDR3/DDR2 Hard Memory PHY (6)	Board Connection Requirement for Pin Migration Only
4B	VREFB4BN	IO			DIFFIO_RX_B82p	DIFFOUT_B82p	AJ10	DQ9B			
4A	VREFB4AN	IO		DATA10	DIFFIO_TX_B83n	DIFFOUT_B83n	AF7			DQ3_4B_0	
4A	VREFB4AN	IO		DATA11	DIFFIO_TX_B83p	DIFFOUT_B83p	AG6	DQ10B			
4A	VREFB4AN	IO		DATA5	DIFFIO_RX_B84n	DIFFOUT_B84n	AJ6	DQ10B			
4A	VREFB4AN	IO		DATA6	DIFFIO_RX_B84p	DIFFOUT_B84p	AK6	DQ10B			
4A	VREFB4AN	IO		DATA12	DIFFIO_TX_B85n	DIFFOUT_B85n	AA8				
4A	VREFB4AN	IO		DATA13	DIFFIO_TX_B85p	DIFFOUT_B85p	AB7	DQ10B			
4A	VREFB4AN	IO		DATA7	DIFFIO_RX_B86n	DIFFOUT_B86n	AK5	DQSn10B/QK10B			
4A	VREFB4AN	IO		DATA8	DIFFIO_RX_B86p	DIFFOUT_B86p	AK4	DQSn10B/QK10B			
4A	VREFB4AN	IO		DATA14	DIFFIO_TX_B87n	DIFFOUT_B87n	AD7				
4A	VREFB4AN	IO		DATA15	DIFFIO_TX_B87p	DIFFOUT_B87p	AE7	DQ10B			
4A	VREFB4AN	IO		DATA9	DIFFIO_RX_B88n	DIFFOUT_B88n	AA6	DQ10B			
4A	VREFB4AN	IO		CLKUSR	DIFFIO_RX_B88p	DIFFOUT_B88p	AB6	DQ10B			
4A	VREFB4AN	IO	VREFB4AND				AC6				
4A	VREFB4AN	IO	RZQ_1				AF4	DQ10B			
4A	VREFB4AN	IO			DIFFIO_RX_B89n	DIFFOUT_B89n	AE6	DQ10B			
4A	VREFB4AN	IO			DIFFIO_RX_B89p	DIFFOUT_B89p	AF6	DQ10B			
		RREF_BR					AF1				
		DNU					AF2				
		DNU					AG2				
5A	VREFB5AN	IO					AD4	DQ1R			GND
5A	VREFB5AN	IO					AE5	DQ1R			
5A	VREFB5AN	IO					Y9	DQ1R			GND
5A	VREFB5AN	IO					W8				GND
5A	VREFB5AN	IO					AD3	DQ1R			GND
5A	VREFB5AN	IO					AE3	DQ1R			GND
5A	VREFB5AN	IO					AB4	DQ1R			GND
5A	VREFB5AN	IO					AA5				GND
5A	VREFB5AN	IO					AC3	DQSn1R/CO1R/CO1R/QK1R			DNU
5A	VREFB5AN	IO					AC4	DQSn1R/CO1R			DNU
5A	VREFB5AN	IO					Y7	DQ1R			GND
5A	VREFB5AN	IO					W8				GND
5A	VREFB5AN	IO					AA3	DQ1R			DNU
5A	VREFB5AN	IO					AB3	DQ1R			GND
5A	VREFB5AN	IO					AD1	DQ1R			GND
5A	VREFB5AN	IO					AD2				GND
5A	VREFB5AN	IO					Y6	DQ2R	DQ1R		GND
5A	VREFB5AN	IO					W6	DQ2R	DQ1R		GND
5A	VREFB5AN	IO					W7	DQ2R	DQ1R		GND
5A	VREFB5AN	IO	VREFB5AND				V7				GND
5A	VREFB5AN	IO					AB1	DQ2R	DQ1R		GND
5A	VREFB5AN	IO					AB2	DQ2R	DQ1R		GND
5A	VREFB5AN	IO					Y1	DQ2R	DQ1R		GND
5A	VREFB5AN	IO					AA2				GND
5A	VREFB5AN	IO					Y4	DQSn2R/CO2R/CO2R/QK2R	DQSn1R/CO1R/CO1R/QK1R		GND
5A	VREFB5AN	IO					W4	DQSn2R/CO2R	DQSn1R/CO1R		DNU
5A	VREFB5AN	IO					W5	DQ2R	DQ1R		GND
5A	VREFB5AN	IO					V5				GND
5A	VREFB5AN	IO					Y3	DQ2R	DQ1R		GND
5A	VREFB5AN	IO					W3	DQ2R	DQ1R		DNU
5A	VREFB5AN	IO					W1	DQ2R	DQ1R		GND
5A	VREFB5AN	IO					W2				GND
5A	VREFB5AN	IO					V3	DQ3R	DQ1R		GND
5A	VREFB5AN	IO					V4	DQ3R	DQ1R		GND
5A	VREFB5AN	IO					V6	DQ3R	DQ1R		GND
5A	VREFB5AN	IO					U6				GND
5A	VREFB5AN	IO					V1	DQ3R	DQ1R		GND
5A	VREFB5AN	IO					Y2	DQ3R	DQ1R		GND
5A	VREFB5AN	IO					U3	DQ3R	DQ1R		DNU
5A	VREFB5AN	IO					T3				GND
5A	VREFB5AN	IO	CLK15p				T1	DQSn3R/CO3R/CO3R/QK3R	DQ1R		GND
5A	VREFB5AN	IO	CLK15n				T2	DQSn3R/CO3R	DQ1R		GND
5A	VREFB5AN	IO					U9	DQ3R	DQ1R		GND
5A	VREFB5AN	IO					U10				GND
5A	VREFB5AN	IO	CLK14p				T4	DQ3R	DQ1R		GND
5A	VREFB5AN	IO	CLK14n				T5	DQ3R	DQ1R		GND
5A	VREFB5AN	IO					T6	DQ3R	DQ1R		GND
5A	VREFB5AN	IO					T7				GND
6A	VREFB6AN	IO		CLK13p			P6	DQ4R	DQ2R		GND
6A	VREFB6AN	IO		CLK13n			R6	DQ4R	DQ2R		GND
6A	VREFB6AN	IO					P7	DQ4R	DQ2R		GND
6A	VREFB6AN	IO					R8				GND
6A	VREFB6AN	IO	CLK12p				R4	DQ4R	DQ2R		DNU
6A	VREFB6AN	IO	CLK12n				R5	DQ4R	DQ2R		GND
6A	VREFB6AN	IO					R3	DQ4R	DQ2R		DNU
6A	VREFB6AN	IO					P4				GND
6A	VREFB6AN	IO	FPLL_RC_CLKOUT2,FPLL_RC_FBp,FPLL_RC_FB1				R1	DQSn4R/CO4R/CO4R/QK4R	DQSn2R/CO2R/CO2R/QK2R		GND
6A	VREFB6AN	IO	FPLL_RC_CLKOUT3,FPLL_RC_FBn				R2	DQSn4R/CO4R	DQSn2R/CO2R		GND
6A	VREFB6AN	IO	FPLL_RC_CLKOUT0,FPLL_RC_CLKOUTp,FPLL_RC_FB0				R9	DQ4R	DQ2R		GND
6A	VREFB6AN	IO	FPLL_RC_CLKOUT1,FPLL_RC_CLKOUTn				R10				GND
6A	VREFB6AN	IO					P3	DQ4R	DQ2R		GND
6A	VREFB6AN	IO					N4	DQ4R	DQ2R		DNU
6A	VREFB6AN	IO					P1	DQ4R	DQ2R		GND
6A	VREFB6AN	IO					N2				GND
6A	VREFB6AN	IO					N3	DQ5R	DQ2R		DNU
6A	VREFB6AN	IO					M3	DQ5R	DQ2R		GND
6A	VREFB6AN	IO					N9	DQ5R	DQ2R		GND
6A	VREFB6AN	IO	VREFB6AND				N10				GND
6A	VREFB6AN	IO					M1	DQ5R	DQ2R		GND
6A	VREFB6AN	IO					M2	DQ5R	DQ2R		GND
6A	VREFB6AN	IO					L3	DQ5R	DQ2R		DNU
6A	VREFB6AN	IO					L4				DNU
6A	VREFB6AN	IO					N5	DQSn5R/CO5R/CO5R/QK5R	DQ2R		GND
6A	VREFB6AN	IO					N6	DQSn5R/CO5R	DQ2R		GND
6A	VREFB6AN	IO					N7	DQ5R	DQ2R		GND
6A	VREFB6AN	IO					N8				GND
6A	VREFB6AN	IO					K1	DQ5R	DQ2R		GND
6A	VREFB6AN	IO					K2	DQ5R	DQ2R		GND
6A	VREFB6AN	IO					K3	DQ5R	DQ2R		GND
6A	VREFB6AN	IO					J3				DNU
6A	VREFB6AN	IO					H1	DQ6R			GND



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (3), (4)	DQS for X8/X9 (5)	DQS for X16/X18	DDR3/DDR2 Hard Memory PHY (6)	Board Connection Requirement for Pin Migration Only
6A	VREFB6AND	IO					J2	DQ6R			GND
6A	VREFB6AND	IO					M5	DQ6R			GND
6A	VREFB6AND	IO					M6				GND
6A	VREFB6AND	IO					G1	DQ6R			GND
6A	VREFB6AND	IO					G2	DQ6R			GND
6A	VREFB6AND	IO					H3	DQ6R			GND
6A	VREFB6AND	IO					J4				DNU
6A	VREFB6AND	IO					H4	DQ56R/CQ6R/CQn6R/QKn6R			GND
6A	VREFB6AND	IO					G4	DQ56R/QK6R			DNU
6A	VREFB6AND	IO					L6	DQ6R			GND
6A	VREFB6AND	IO					M7				GND
6A	VREFB6AND	IO					F3	DQ6R			GND
6A	VREFB6AND	IO					G3	DQ6R			DNU
6A	VREFB6AND	IO					E3	DQ6R			GND
6A	VREFB6AND	IO					F4				GND
7A		DNU					H5				
7A		GND					F5				
7A	VREFB7AND	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	C5	DQ1T			
7A	VREFB7AND	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	D5	DQ1T			
7A	VREFB7AND	IO					J6	DQ1T			
7A	VREFB7AND	IO	VREFB7AND				K6				
7A	VREFB7AND	IO		DEV_OE	DIFFIO_RX_T2p	DIFFOUT_T2p	A5	DQ1T			
7A	VREFB7AND	IO		DEV_CLRn	DIFFIO_RX_T2n	DIFFOUT_T2n	A4	DQ1T			
7A	VREFB7AND	IO	RZQ_5				E4	DQ1T			
7A	VREFB7AND	IO		nPERSTL0			K7				
7A	VREFB7AND	IO		CyP_CONFDONE	DIFFIO_RX_T4p	DIFFOUT_T4p	D6	DQS1T/CQ1T/CQn1T/QKn1T			
7A	VREFB7AND	IO		CRC_ERROR	DIFFIO_RX_T4n	DIFFOUT_T4n	E6	DQS1T/QK1T			
7A	VREFB7AND	IO		PR_DONE	DIFFIO_TX_T5p	DIFFOUT_T5p	G6	DQ1T			
7A	VREFB7AND	IO		PR_REQUEST	DIFFIO_TX_T5n	DIFFOUT_T5n	H6				
7A	VREFB7AND	IO		INIT_DONE	DIFFIO_RX_T6p	DIFFOUT_T6p	A6	DQ1T			
7A	VREFB7AND	IO		nCEO	DIFFIO_RX_T6n	DIFFOUT_T6n	B6	DQ1T			
7A	VREFB7AND	IO		PR_ERROR	DIFFIO_TX_T7p	DIFFOUT_T7p	G7	DQ1T			
7A	VREFB7AND	IO		PR_READY	DIFFIO_TX_T7n	DIFFOUT_T7n	H7				
7B	VREFB7BND	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	D9	DQ2T			DQ3_7B_0
7B	VREFB7BND	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	E9	DQ2T			DQ3_7B_1
7B	VREFB7BND	IO					B10	DQ2T			DQ3_7B_2
7B	VREFB7BND	IO	VREFB7BND				K8				
7B	VREFB7BND	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	A11	DQ2T			DQ3_7B_3
7B	VREFB7BND	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	A10	DQ2T			DQ3_7B_4
7B	VREFB7BND	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	J10	DQ2T			DQ3_7B_5
7B	VREFB7BND	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	K10				
7B	VREFB7BND	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	C10	DQS2T/CQ2T/CQn2T/QKn2T			DQ3_7B
7B	VREFB7BND	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	D10	DQS2T/QK2T			DQ3_7B_7B
7B	VREFB7BND	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	E10	DQ2T			DM3_7B
7B	VREFB7BND	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	F10				
7B	VREFB7BND	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	C11	DQ2T			DQ3_7B_6
7B	VREFB7BND	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	D11	DQ2T			DQ3_7B_7
7B	VREFB7BND	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	G10	DQ2T			DQ3_7B_8
7B	VREFB7BND	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	H10				
7C	VREFB7CND	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	J11	DQ3T	DQ1T		DQ2_7C_0
7C	VREFB7CND	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	K11	DQ3T	DQ1T		DQ2_7C_1
7C	VREFB7CND	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	F11	DQ3T	DQ1T		DQ2_7C_2
7C	VREFB7CND	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	G11				
7C	VREFB7CND	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	B13	DQ3T	DQ1T		DQ2_7C_3
7C	VREFB7CND	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	B12	DQ3T	DQ1T		DQ2_7C_4
7C	VREFB7CND	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	D12	DQ3T	DQ1T		DQ2_7C_5
7C	VREFB7CND	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	E12				
7C	VREFB7CND	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	J12	DQS3T/CQ3T/CQn3T/QKn3T	DQS1T/CQ1T/CQn1T/QKn1T		DQ2_7C_6
7C	VREFB7CND	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	K12	DQS3T/QK3T	DQS1T/QK1T		DQ2_7C_7C
7C	VREFB7CND	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	G12	DQ3T	DQ1T		DM2_7C
7C	VREFB7CND	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	H12				
7C	VREFB7CND	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	C13	DQ3T	DQ1T		DQ2_7C_8
7C	VREFB7CND	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	D13	DQ3T	DQ1T		DQ2_7C_7
7C	VREFB7CND	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	E13	DQ3T	DQ1T		DQ2_7C_8
7C	VREFB7CND	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	F13				
7C	VREFB7CND	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	J14	DQ4T	DQ1T		DQ1_7C_0
7C	VREFB7CND	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	K14	DQ4T	DQ1T		DQ1_7C_1
7C	VREFB7CND	IO	VREFB7CND				J13	DQ4T	DQ1T		DQ1_7C_2
7C	VREFB7CND	IO					K13				
7C	VREFB7CND	IO			DIFFIO_RX_T24p	DIFFOUT_T24p	A14	DQ4T	DQ1T		DQ1_7C_3
7C	VREFB7CND	IO			DIFFIO_RX_T24n	DIFFOUT_T24n	A13	DQ4T	DQ1T		DQ1_7C_4
7C	VREFB7CND	IO			DIFFIO_TX_T25p	DIFFOUT_T25p	F14	DQ4T	DQ1T		DQ1_7C_5
7C	VREFB7CND	IO			DIFFIO_TX_T25n	DIFFOUT_T25n	G14				
7C	VREFB7CND	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	C14	DQS4T/CQ4T/CQn4T/QKn4T	DQ1T		DQS1_7C
7C	VREFB7CND	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	D14	DQS4T/QK4T	DQ1T		DQS1_7C
7C	VREFB7CND	IO			DIFFIO_TX_T27p	DIFFOUT_T27p	G13	DQ4T	DQ1T		DM1_7C
7C	VREFB7CND	IO			DIFFIO_TX_T27n	DIFFOUT_T27n	H13				
7C	VREFB7CND	IO			DIFFIO_RX_T28p	DIFFOUT_T28p	A15	DQ4T	DQ1T		DQ1_7C_6
7C	VREFB7CND	IO			DIFFIO_RX_T28n	DIFFOUT_T28n	B15	DQ4T	DQ1T		DQ1_7C_7
7C	VREFB7CND	IO			DIFFIO_TX_T29p	DIFFOUT_T29p	D15	DQ4T	DQ1T		DQ1_7C_8
7C	VREFB7CND	IO			DIFFIO_TX_T29n	DIFFOUT_T29n	E15				RESERVE_7D
7D	VREFB7DND	IO			DIFFIO_RX_T30p	DIFFOUT_T30p	F15	DQ5T	DQ2T		CK_7D
7D	VREFB7DND	IO			DIFFIO_RX_T30n	DIFFOUT_T30n	G15	DQ5T	DQ2T		CK#_7D
7D	VREFB7DND	IO			DIFFIO_TX_T31p	DIFFOUT_T31p	J16	DQ5T	DQ2T		CKE_7D_0
7D	VREFB7DND	IO			DIFFIO_TX_T31n	DIFFOUT_T31n	K16				CKE_7D_1
7D	VREFB7DND	IO			DIFFIO_RX_T32p	DIFFOUT_T32p	H15	DQ5T	DQ2T		A_7D_0
7D	VREFB7DND	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	J15	DQ5T	DQ2T		A_7D_1
7D	VREFB7DND	IO			DIFFIO_TX_T33p	DIFFOUT_T33p	D16	DQ5T	DQ2T		A_7D_2
7D	VREFB7DND	IO			DIFFIO_TX_T33n	DIFFOUT_T33n	E16				A_7D_3
7D	VREFB7DND	IO			DIFFIO_RX_T34p	DIFFOUT_T34p	B16	DQS5T/CQ5T/CQn5T/QKn5T	DQS2T/CQ2T/CQn2T/QKn2T		A_7D_4
7D	VREFB7DND	IO			DIFFIO_RX_T34n	DIFFOUT_T34n	C16	DQS5T/QK5T	DQS2T/QK2T		A_7D_5
7D	VREFB7DND	IO			DIFFIO_TX_T35p	DIFFOUT_T35p	G16	DQ5T	DQ2T		A_7D_6
7D	VREFB7DND	IO			DIFFIO_TX_T35n	DIFFOUT_T35n	H16				A_7D_7
7D	VREFB7DND	IO			DIFFIO_RX_T36p	DIFFOUT_T36p	A17	DQ5T	DQ2T		A_7D_8
7D	VREFB7DND	IO			DIFFIO_RX_T36n	DIFFOUT_T36n	A16	DQ5T	DQ2T		A_7D_9
7D	VREFB7DND	IO			DIFFIO_TX_T37p	DIFFOUT_T37p	C17	DQ5T	DQ2T		A_7D_10
7D	VREFB7DND	IO			DIFFIO_TX_T37n	DIFFOUT_T37n	D17				A_7D_11
7D	VREFB7DND	IO			DIFFIO_RX_T38p	DIFFOUT_T38p	J17	DQ6T	DQ2T		A_7D_12
7D	VREFB7DND	IO			DIFFIO_RX_T38n	DIFFOUT_T38n	K17	DQ6T	DQ2T		A_7D_13
7D	VREFB7DND	IO					J18	DQ6T	DQ2T		A_7D_14
7D	VREFB7DND	IO	VREFB7DND				K18				

Table with columns: Bank Number, VREF, PinName/Function (2), Optional Function(s), Configuration Function, Dedicated Tx/Rx Channel, Emulated LVDS Output Channel, F896 (3), (4), DQS for X8/X9 (5), DQS for X16/X18, DDR3/DDR2 Hard Memory PHY (6), Board Connection Requirement for Pin Migration Only. Rows include VREFB7DNN, VREFB8DNN, and VREFB8AND.



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (3), (4)	DQS for X8/X9 (5)	DQS for X16/X18	DDR3/DDR2 Hard Memory PHY (6)	Board Connection Requirement for Pin Migration Only
		GND					AE30				
		GND					E30				
		GND					F27				
		GND					F28				
		GND					G26				
		GND					G29				
		GND					G30				
		GND					H27				
		GND					H28				
		GND					J26				
		GND					J29				
		GND					J30				
		GND					K27				
		GND					K28				
		GND					L25				
		GND					L26				
		GND					L29				
		GND					L30				
		GND					M24				
		GND					M27				
		GND					M28				
		GND					N23				
		GND					N24				
		GND					N26				
		GND					N29				
		GND					N30				
		GND					P23				
		GND					P25				
		GND					P27				
		GND					P28				
		GND					R24				
		GND					R29				
		GND					R30				
		GND					T23				
		GND					T27				
		GND					T28				
		GND					U24				
		GND					U26				
		GND					U29				
		GND					U30				
		GND					V23				
		GND					V25				
		GND					V27				
		GND					V28				
		GND					W24				
		GND					W29				
		GND					W30				
		GND					Y22				
		GND					Y23				
		GND					Y24				
		GND					Y25				
		GND					Y26				
		GND					Y27				
		GND					Y28				
		VCCP					L11				
		VCCP					L15				
		VCCP					L19				
		VCCP					L20				
		VCCP					L9				
		VCCP					W11				
		VCCP					W13				
		VCCP					W17				
		VCCP					W19				
		VCCP					W21				
		VCCA_FP1L					T22				
		VCCA_FP1L					T9				
		VCCA_FP1L					P22				
		VCCA_FP1L					P9				
		VCCBAT					K26				
		VCC_AUX					M12				
		VCC_AUX					M18				
		VCC_AUX					W12				
		VCC_AUX					W18				
		VCCD_FP1L					V22				
		VCCD_FP1L					V9				
		VCCD_FP1L					N22				
		VCCD_FP1L					M8				
		VCCA_GXBL0					V24				
		VCCA_GXBL1					P24				
		VCCD_GXBL0					T24				
		VCCD_GXBL1					N25				
		VCCD_GXBL0					T25				
		VCCD_GXBL0					T26				
		VCCD_GXBL1					M25				
		VCCR_GXBL					M26				
		VCCR_GXBL					R25				
		VCCR_GXBL					R26				
		VCCR_GXBL					W25				
		VCCR_GXBL					W26				
		VCCT_GXBL0					U25				
		VCCT_GXBL0					V26				
		VCCT_GXBL1					P26				
		VCC					M10				
		VCC					M14				
		VCC					N20				
		VCC					N11				
		VCC					N13				
		VCC					N15				
		VCC					N17				
		VCC					N19				
		VCC					N21				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (3), (4)	DQS for X8/X9 (5)	DQS for X16/X18	DDR3/DDR2 Hard Memory PHY (6)	Board Connection Requirement for Pin Migration Only
		VCC					P10				
		VCC					P12				
		VCC					P14				
		VCC					P16				
		VCC					P18				
		VCC					P20				
		VCC					R11				
		VCC					R13				
		VCC					R15				
		VCC					R17				
		VCC					R19				
		VCC					R21				
		VCC					T10				
		VCC					T12				
		VCC					T14				
		VCC					T18				
		VCC					T20				
		VCC					U11				
		VCC					U13				
		VCC					U15				
		VCC					U17				
		VCC					U19				
		VCC					U21				
		VCC					V10				
		VCC					V12				
		VCC					V14				
		VCC					V16				
		VCC					V18				
		VCC					V20				
		VCC					T16				
		VCCIO3A					AD26				
		VCCIO3A					AE24				
		VCCIO3A					AH24				
		VCCIO3A					AH27				
		VCCIO3D					AE19				
		VCCIO3D					AE21				
		VCCIO3D					AH21				
		VCCIO3D					AK23				
		VCCIO4A					AB5				
		VCCIO4A					AD5				
		VCCIO4A					AH3				
		VCCIO4A					AH6				
		VCCIO4B					AE10				
		VCCIO4B					AG9				
		VCCIO4B					AH10				
		VCCIO4B					AK9				
		VCCIO4C					AE12				
		VCCIO4C					AG13				
		VCCIO4C					AK13				
		VCCIO4C					AK15				
		VCCIO4D					AE16				
		VCCIO4D					AG18				
		VCCIO4D					AH16				
		VCCIO4D					AK18				
		VCCIO5A					AA1				DNU
		VCCIO5A					AA4				DNU
		VCCIO5A					AC1				DNU
		VCCIO5A					AE4				VCCIO5A (can combine with VCCIO4A)
		VCCIO5A					U1				DNU
		VCCIO5A					U4				DNU
		VCCIO6A					F1				VCCIO6A (can combine with VCCIO7A)
		VCCIO6A					J1				DNU
		VCCIO6A					K4				DNU
		VCCIO6A					L1				DNU
		VCCIO6A					M4				DNU
		VCCIO6A					N1				DNU
		VCCIO7A					C3				DNU
		VCCIO7A					C6				
		VCCIO7A					F2				
		VCCIO7A					F6				
		VCCIO7B					A9				
		VCCIO7B					C9				
		VCCIO7B					D7				
		VCCIO7B					F9				
		VCCIO7C					A12				
		VCCIO7C					C12				
		VCCIO7C					C15				
		VCCIO7C					F12				
		VCCIO7D					A18				
		VCCIO7D					C18				
		VCCIO7D					F16				
		VCCIO7D					F18				
		VCCIO8A					A25				
		VCCIO8A					C24				
		VCCIO8A					F24				
		VCCIO8A					L23				
		VCCIO8D					A20				
		VCCIO8D					A22				
		VCCIO8D					C21				
		VCCIO8D					F22				
		VCCPD3					AA23				
		VCCPD3					Y21				
		VCCPD4A					AA7				
		VCCPD4BCD					Y10				
		VCCPD4BCD					Y15				
		VCCPD4BCD					Y18				
		VCCPD6					U7				DNU
		VCCPD6					V8				DNU
		VCCPD6					R7				DNU
		VCCPD6					T8				DNU
		VCCPD7A					L8				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (3), (4)	DQS for X8/X9 (5)	DQS for X16/X18	DDR3/DDR2 Hard Memory PHY (6)	Board Connection Requirement for Pin Migration Only
		VCCPD7BCD					L13				
		VCCPD7BCD					L17				
		VCCPD7BCD					M9				
		VCCPD8					M22				
		VCCPD8					M23				
		VCCPGM					K5				
		VCCPGM					AA24				
		GND					AC11				
		GND					AC14				
		GND					AC17				
		GND					AC2				
		GND					AC20				
		GND					AC23				
		GND					AC5				
		GND					AC6				
		GND					AE1				
		GND					AE2				
		GND					AF11				
		GND					AF14				
		GND					AF17				
		GND					AF20				
		GND					AF23				
		GND					AF26				
		GND					AF3				
		GND					AF5				
		GND					AF8				
		GND					AG1				
		GND					AH29				
		GND					AJ11				
		GND					AJ14				
		GND					AJ17				
		GND					AJ2				
		GND					AJ20				
		GND					AJ23				
		GND					AJ26				
		GND					AJ5				
		GND					AJ8				
		GND					B11				
		GND					B14				
		GND					B17				
		GND					B2				
		GND					B20				
		GND					B23				
		GND					B26				
		GND					B29				
		GND					B5				
		GND					B8				
		GND					E11				
		GND					E14				
		GND					E17				
		GND					E2				
		GND					E20				
		GND					E23				
		GND					E26				
		GND					E5				
		GND					E8				
		GND					G6				
		GND					H11				
		GND					H14				
		GND					H17				
		GND					H2				
		GND					H20				
		GND					H23				
		GND					H8				
		GND					J5				
		GND					L10				
		GND					L12				
		GND					L14				
		GND					L16				
		GND					L18				
		GND					L2				
		GND					L21				
		GND					L24				
		GND					L5				
		GND					L7				
		GND					M11				
		GND					M13				
		GND					M17				
		GND					M19				
		GND					M2				
		GND					M12				
		GND					N14				
		GND					N18				
		GND					N20				
		GND					P1				
		GND					P13				
		GND					P15				
		GND					P17				
		GND					P19				
		GND					P2				
		GND					P21				
		GND					P5				
		GND					R12				
		GND					R16				
		GND					R18				
		GND					R20				
		GND					T11				
		GND					T13				
		GND					T15				
		GND					T17				
		GND					T19				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (3), (4)	DQS for X8/X9 (5)	DQS for X16/X18	DDR3/DDR2 Hard Memory PHY (6)	Board Connection Requirement for Pin Migration Only
		GND					T21				
		GND					U12				
		GND					U16				
		GND					U18				
		GND					U2				
		GND					U20				
		GND					U5				
		GND					U8				
		GND					V11				
		GND					V13				
		GND					V15				
		GND					V17				
		GND					V19				
		GND					V21				
		GND					W10				
		GND					W14				
		GND					W20				
		GND					Y11				
		GND					Y14				
		GND					Y17				
		GND					Y19				
		GND					Y2				
		GND					Y5				
		GND					Y8				
		GND					U14				
		GND					P8				
		GND					N16				
		GND					R16				
		NC					F8				
		NC					G8				
		NC					J8				
		NC					B9				
		NC					E7				
		NC					F7				
		NC					G9				
		NC					H9				
		NC					A7				
		NC					A8				
		NC					B7				
		NC					C7				
		NC					C8				
		NC					D8				
		NC					J9				
		VCCPD6					K9				VCCPD6 (can combine with VccPD7A)
		NC					AE9				
		NC					AF9				
		NC					AJ9				
		NC					AK9				
		NC					AC9				
		NC					AD9				
		VCCPD5					AA9				VCCPD5 (can combine with VccPD4A)
		NC					AB8				
		NC					AG8				
		NC					AH8				
		NC					AJ7				
		NC					AK7				
		NC					AC10				
		NC					AE8				
		NC					AG7				
		NC					AH7				
		NC					AH1				
		NC					AH2				
		NC					AC7				
		NC					AK2				
		NC					AJ1				
		NC					AG3				
		NC					AG4				
		NC					AK3				
		NC					AJ3				
		NC					AD6				
		NC					AJ4				
		NC					AH4				
		NC					AH5				
		NC					C4				
		NC					AG5				
		NC					B4				
		NC					B3				
		NC					A3				
		NC					C1				
		NC					C2				
		NC					B1				
		NC					A2				
		NC					D3				
		NC					D4				
		NC					D1				
		NC					D2				
		NC					J7				
		NC					E1				

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).
(2) The GXB_REFCLK pin is not supported in the current Quartus II version, but will be supported in the future Quartus II release version.
(3) Pins with * are with reference to the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).
(4) AF4, E4, and K7 pins do not have LVDS support for pin migration.
(5) The DQ pin for AF4 and E4 pins does not support pin migration.
(6) The RESET pin is only applicable for DDR3 devices.



**Pin Information for the Arria® V 5AGTMC3 Device
Version 1.1**

Version Number	Date	Changes Made
1.0	10/24/2012	Initial release.
1.1	7/31/2015	Removed LPDDR2 hard memory PHY, RLDRAMII hard memory PHY, and QDRII hard memory PHY columns.