Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F780	F572	U358	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16X18 for F780 (Note 3)	DQS for X32X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16X18 for F572 (Note 3)	DQS for X4 for U358	DQS for X8/X9 for U358 (Note 3)	DQS for X16X18 for U358 (Note 3)
QL1			GXB_TX7n					K26	B22											
QL1			GXB_TX7p					K25	B21											
QL1			GXB_RX7n					L28	C24											
QL1			GXB_RX7p					L27	C23											
QL1			GXB_TX6n					M26	D22											
QL1			GXB_TX6p					M25	D21											
QL1			GXB_RX6n					N28	E24											
QL1			GXB_RX6p					N27	E23											
QL1			REFCLK5n					P26	F22											
QL1			REFCLK5p					P25	F21											
QL1			REFCLK1n					R28	G24											
QL1			REFCLK1p					R27	G23											
QL1			GXB_TX5n					T26	H22											
QL1			GXB_TX5p					T25	H21											
QL1			GXB_RX5n					U28	J24											
QL1			GXB_RX5p					U27	J23											
QL1			GXB_TX4n					V26	K22											
QL1			GXB_TX4p					V25	K21											
QL1			GXB_RX4n					W28	L24											
QL1			GXB_RX4p					W27	L23											
QL0			GXB_TX3n					Y26	M22	B20										
QL0			GXB_TX3p					Y25	M21	B19										
QL0			GXB_RX3n					AA28	N24	D20										
QL0			GXB_RX3p					AA27	N23	D19										
QL0			GXB_TX2n					AB26	P22	F20										
QL0			GXB_TX2p					AB25	P21	F19										
QL0			GXB_RX2n					AC28	R24	H20										
QL0			GXB_RX2p					AC27	R23	H19										
QL0			REFCLK4n					AD26	T22	K20										
QL0			REFCLK4p					AD25	T21	K19										
QL0			REFCLK0n					AE28	U24	M20										
QL0			REFCLK0p					AE27	U23	M19										
QL0			GXB_TX1n					AH27	V22	P20										
QL0			GXB_TX1p					AG27	V21	P19										
QL0			GXB_RX1n					AH25	W24	T20										
QL0			GXB_RX1p					AG25	W23	T19										
QL0			GXB_TX0n					AF24	Y22	V20										
QL0			GXB_TX0p					AE24	Y21	V19										
QL0			GXB_RX0n					AH23	AA24	Y17										
QL0			GXB_RX0p					AG23	AA23	W17										
3C			nCONFIG		nCONFIG			AA24	V20	M17										
3C			CONF_DONE		CONF_DONE			AA23	W19	N17										
3C			MSEL3		MSEL3			AB24	T20	U16										
3C			MSEL2		MSEL2			Y24	W20	R16										
3C			MSEL1		MSEL1			Y23	T19	P17										
3C			MSEL0		MSEL0			W24	Y19	R18										
3C			nSTATUS		nSTATUS			W23	U18	V16										
3C			nIO_PULLUP		nIO_PULLUP			AB22	U19	L17										
3C			nCE		nCE			AA22	V18	K18										
3A		VREFB3AN0	IO	PLL4_CLKOUT1n				U24	Y16	W15										
3A		VREFB3AN0	IO	RDN0				AB19	AB20	Y15										
3A		VREFB3AN0	IO	PLL4_CLKOUT1p				V24	W16	V15										
3A		VREFB3AN0	IO	RUP0				AC19	AA20	Y14										
3A	BIO1	VREFB3AN0	IO			DIFFIO_TX_B1n	DIFFIN_B1n*	AD21	AC21	V14	DQ14B	DQ7B			DQ8B	DQ4B	DQ2B	DQ6B	DQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_RX_B1n	DIFFOUT_B1n	AC17	AD21	Y13	DQ14B	DQ7B			DQ8B	DQ4B	DQ2B	DQ6B	DQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFIN_B1p*	AC21	AB21	V13	DQ14B	DQ7B			DQ8B	DQ4B	DQ2B	DQ6B	DQ3B	
3A	BIO1	VREFB3AN0	IO		INIT_DONE	DIFFIO_RX_B1p	DIFFOUT_B1p	AB17	AD20	W13										
3A	BIO1	VREFB3AN0	IO			DIFFIO_TX_B2n	DIFFIN_B2n*	Y22	V16	U15	DQSn14B	DQ7B			DQSn8B	DQ4B	DQ2B	DQSn6B	DQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	AC16	AB19	Y12	DQ14B	DQ7B			DQ8B	DQ4B	DQ2B	DQ6B	DQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_TX_B2p	DIFFIN_B2p*	W21	U16	U14	DQS14B	DQ7B/CQn7B			DQS8B	DQ4B/CQn4B	DQ2B	DQS6B	DQ3B/CQn3B	
3A	BIO1	VREFB3AN0	IO		nCEO	DIFFIO_RX_B2p	DIFFOUT_B2p	AB16	AA19	W12										
3A	BIO1	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFIN_B3n*	AD23	AC18	Y11	DQSn13B	DQSn7B/DQ7B			DQSn7B	DQSn4B/DQ4B	DQ2B	DQSn5B	DQSn3B/DQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B3n	AD18	AB18	V12	DQ13B	DQ7B			DQ7B	DQ4B	DQ2B	DQ5B	DQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFIN_B3p*	AD22	AB17	Y10	DQS13B	DQS7B/CQ7B			DQS7B	DQS4B/CQ4B	DQ2B	DQS5B	DQS3B/CQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B3p	AC18	AA18	U13										
3A	BIO1	VREFB3AN0	IO			DIFFIO_TX_B4n	DIFFIN_B4n*	Y20	W15	U12	DQ13B	DQ7B			DQ7B	DQ4B	DQ2B	DQ5B	DQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	AC23	AA15	Y9	DQ13B	DQ7B			DQ7B	DQ4B	DQ2B	DQ5B	DQ3B	
3A	BIO1	VREFB3AN0	IO			DIFFIO_TX_B4p	DIFFIN_B4p*	Y19	V15	U11										
3A	BIO1	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	AC22	Y15	W10	DQ13B	DQ7B			DQ7B	DQ4B	DQ2B	DQ5B	DQ3B	
3A	BIO2	VREFB3AN0	IO			DIFFIO_TX_B5n	DIFFIN_B5n*	AD24			DQ12B	DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B5n	AE22			DQ12B	DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_TX_B5p	DIFFIN_B5p*	AC24			DQ12B	DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B5p	AE21												
3A	BIO2	VREFB3AN0	IO			DIFFIO_TX_B6n	DIFFIN_B6n*	V23			DQSn12B	DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	AF20			DQ12B	DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_TX_B6p	DIFFIN_B6p*	V22			DQS12B	DQ6B/CQn6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	AE20												
3A	BIO2	VREFB3AN0	IO			DIFFIO_TX_B7n	DIFFIN_B7n*	AF18			DQSn11B	DQSn6B/DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B7n	AF19			DQ11B	DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_TX_B7p	DIFFIN_B7p*	AE18			DQS11B	DQS6B/CQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B7p	AE19												
3A	BIO2	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFIN_B8n*	AA16			DQ11B	DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	AF17			DQ11B	DQ6B	DQ3B							
3A	BIO2	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFIN_B8p*	Y16												
3A	BIO2	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	AE17			DQ11B	DQ6B	DQ3B							
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B9n	DIFFIN_B9n*	AD15	AB16		DQ10B	DQ5B	DQ3B		DQ6B	DQ3B	DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B9n	AF16	AD19		DQ10B	DQ5B	DQ3B		DQ6B	DQ3B	DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B9p	DIFFIN_B9p*	AC15	AA16		DQ10B	DQ5B	DQ3B		DQ6B	DQ3B	DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B9p	AE16	AC19											
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFIN_B10n*	AA19	W14		DQSn10B	DQ5B	DQ3B		DQSn6B	DQ3B	DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AH19	AD18		DQ10B	DQ5B	DQ3B		DQ6B	DQ3B	DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFIN_B10p*	Y18	V14		DQS10B	DQS6B/CQn5B	DQ3B/CQn3B		DQS6B	DQ3B/CQn3B	DQ2B/CQn2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	AG19	AD17											
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B11n	DIFFIN_B11n*	AH17	AB14		DQSn9B	DQSn5B/DQ5B	DQSn3B/DQ3B		DQSn5B	DQSn3B/DQ3B	DQSn2B/DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AH18	AC15		DQ9B	DQ5B	DQ3B		DQ5B	DQ3B	DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B11p	DIFFIN_B11p*	AH16	AA14		DQS9B	DQS5B/CQ5B	DQS3B/CQ3B		DQS5B	DQS3B/CQ3B	DQS2B/CQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AG18	AB15											
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFIN_B12n*	AB15	W13		DQ9B	DQ5B	DQ3B		DQ5B	DQ3B	DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B12n	DIFFOUT_B12n	AH15	AD16		DQ9B	DQ5B	DQ3B		DQ5B	DQ3B	DQ2B			
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFIN_B12p*	AA15	V13											
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B12p	DIFFOUT_B12p	AG15	AD15		DQ9B	DQ5B	DQ3B		DQ5B	DQ3B	DQ2B			
3A		VREFB3AN0	CLK4	DIFFCLK_0n				AF15	AA13	U10										
4A		VREFB4AN0	CLK5	DIFFCLK_1n				AF14	AD14	Y8										
3A		VREFB3AN0	CLK6	DIFFCLK_0p				AE15	Y13	T10										
4A		VREFB4AN0	CLK7	DIFFCLK_1p				AE14	AD13	W9										
4A	BIO4	VREFB4AN0	IO			DIFFIO_TX_B13n	DIFFIN_B13n*	AH14	AC13	V10	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AH12	AC12	Y7	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_TX_B13p	DIFFIN_B13p*	AH13	AB13	V9	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AG12	AB12	W7										
4A	BIO4	VREFB4AN0	IO			DIFFIO_TX_B14n	DIFFIN_B14n*	Y14	W12	V7	DQSn8B	DQ4B	DQ2B	DQ1B	DQSn4B	DQ2B	DQ1B	DQSn4B	DQ2B	DQ1B

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F780	F572	U358	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16X18 for F780 (Note 3)	DQS for X32X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16X18 for F572 (Note 3)	DQS for X4 for U358	DQS for X8/X9 for U358 (Note 3)	DQS for X16X18 for U358 (Note 3)
4A	BIO4	VREFB4AN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AH11	AD12	V6	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_TX_B14p	DIFFIN_B14p*	Y13	V12	U7	DQS8B	DQ4B/CQn4B	DQ2B/CQn2B	DQ1B	DQS4B	DQ2B/CQn2B	DQ1B/CQn1B	DQS4B	DQ2B/CQn2B	DQ1B/CQn1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	AH10	AD11	W6										
4A	BIO4	VREFB4AN0	IO			DIFFIO_TX_B15n	DIFFIN_B15n*	AH8	AB11	Y3	DQSn7B	DQSn4B/DQ4B	DQSn2B/DQ2B	DQ1B	DQSn3B	DQSn2B/DQ2B	DQSn1B/DQ1B	DQSn3B	DQSn2B/DQ2B	DQSn1B/DQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AH9	AA12	Y5	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_TX_B15p	DIFFIN_B15p*	AH7	AA11	Y2	DQS7B	DQS4B/CQ4B	DQS2B/CQ2B	DQ1B	DQS3B	DQS2B/CQ2B	DQS1B/CQ1B	DQS3B	DQS2B/CQ2B	DQS1B/CQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AG9	Y12	Y4										
4A	BIO4	VREFB4AN0	IO			DIFFIO_TX_B16n	DIFFIN_B16n*	AC14	W11	V8	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_RX_B16n	DIFFOUT_B16n	AH6	AD10	V1	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
4A	BIO4	VREFB4AN0	IO			DIFFIO_TX_B16p	DIFFIN_B16p*	AB14	V11	U9										
4A	BIO4	VREFB4AN0	IO			DIFFIO_RX_B16p	DIFFOUT_B16p	AG6	AD9	W1	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
4A	BIO5	VREFB4AN0	IO			DIFFIO_TX_B17n	DIFFIN_B17n*	AH5			DQ6B	DQ3B	DQ2B	DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AF13			DQ6B	DQ3B	DQ2B	DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_TX_B17p	DIFFIN_B17p*	AH4			DQ6B	DQ3B	DQ2B	DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AE13												
4A	BIO5	VREFB4AN0	IO			DIFFIO_TX_B18n	DIFFIN_B18n*	AC13			DQSn6B	DQ3B	DQ2B	DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AF12			DQ6B	DQ3B	DQ2B	DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_TX_B18p	DIFFIN_B18p*	AB13			DQS6B	DQ3B/CQn3B	DQ2B	DQ1B/CQn1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AE12												
4A	BIO5	VREFB4AN0	IO			DIFFIO_TX_B19n	DIFFIN_B19n*	AF10			DQSn5B	DQSn3B/DQ3B	DQ2B	DQSn1B/DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AF11			DQ5B	DQ3B	DQ2B	DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_TX_B19p	DIFFIN_B19p*	AE10			DQS5B	DQS3B/CQ3B	DQ2B	DQS1B/CQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AE11												
4A	BIO5	VREFB4AN0	IO			DIFFIO_TX_B20n	DIFFIN_B20n*	W13			DQ5B	DQ3B	DQ2B	DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_RX_B20n	DIFFOUT_B20n	AF9			DQ5B	DQ3B	DQ2B	DQ1B						
4A	BIO5	VREFB4AN0	IO			DIFFIO_TX_B20p	DIFFIN_B20p*	W12												
4A	BIO5	VREFB4AN0	IO			DIFFIO_RX_B20p	DIFFOUT_B20p	AE9			DQ5B	DQ3B	DQ2B	DQ1B						
4A	BIO6	VREFB4AN0	IO			DIFFIO_TX_B21n	DIFFIN_B21n*	AF8	AB10	V6	DQ4B	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AF7	AC9	W4	DQ4B	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_TX_B21p	DIFFIN_B21p*	AE8	AA10	V5	DQ4B	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AE7	AB9	V4										
4A	BIO6	VREFB4AN0	IO			DIFFIO_TX_B22n	DIFFIN_B22n*	Y12	W10	R6	DQSn4B	DQ2B	DQ1B	DQ1B	DQSn2B	DQ1B	DQ1B	DQSn2B	DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	AF6	AD8	V1	DQ4B	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_TX_B22p	DIFFIN_B22p*	W11	W9	P6	DQS4B	DQ2B/CQn2B	DQ1B/CQn1B	DQ1B	DQS2B	DQ1B/CQn1B	DQ1B	DQS2B	DQ1B/CQn1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	AE6	AD7	V2										
4A	BIO6	VREFB4AN0	IO			DIFFIO_TX_B23n	DIFFIN_B23n*	AD12	AB7	V3	DQSn3B	DQSn2B/DQ2B	DQSn1B/DQ1B	DQ1B	DQSn1B	DQSn1B/DQ1B	DQ1B	DQSn1B	DQSn1B/DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AF5	AB8	U1	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_TX_B23p	DIFFIN_B23p*	AC12	AA7	U3	DQS3B	DQS2B/CQ2B	DQS1B/CQ1B	DQ1B	DQS1B	DQS1B/CQ1B	DQ1B	DQS1B	DQS1B/CQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AE5	AA8	U2										
4A	BIO6	VREFB4AN0	IO			DIFFIO_TX_B24n	DIFFIN_B24n*	AC11	V9	U6	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B24n	AG4	AD6	R3	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
4A	BIO6	VREFB4AN0	IO			DIFFIO_TX_B24p	DIFFIN_B24p*	AB11	U9	T7										
4A	BIO6	VREFB4AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B24p	AG3	AC6	P3	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B25n	DIFFIN_B25n*	AH3			DQ2B	DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AF4			DQ2B	DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFIN_B25p*	AH2			DQ2B	DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AE4												
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B26n	DIFFIN_B26n*	Y11			DQSn2B	DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AF3			DQ2B	DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B26p	DIFFIN_B26p*	W10			DQS2B	DQ1B/CQn1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AF2												
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B27n	DIFFIN_B27n*	AD6			DQSn1B	DQSn1B/DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AG1			DQ1B	DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B27p	DIFFIN_B27p*	AC6			DQS1B	DQS1B/CQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AF1												
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFIN_B28n*	AA10			DQ1B	DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B28n	DIFFOUT_B28n	AD9			DQ1B	DQ1B	DQ1B	DQ1B						
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFIN_B28p*	Y10												
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B28p	DIFFOUT_B28p	AC9			DQ1B	DQ1B	DQ1B	DQ1B						
4A		VREFB4AN0	IO	PLL3_CLKOUT1n				AC10	AA9	U4										
4A		VREFB4AN0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AD7	AB6	R4										
4A		VREFB4AN0	IO	PLL3_CLKOUT1p				AB10	Y9	T4										
4A		VREFB4AN0	IO			DIFFIO_RX_B29p	DIFFOUT_B29p	AC7	AA6	P4										
5A	RIO1	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFIN_R1n*	AA6	AD5	R1	DQ14R	DQ7R	DQ3R	DQ1R	DQ12R	DQ6R		DQ4R	DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	AD4	AB5	P1	DQ14R	DQ7R	DQ3R	DQ1R	DQ12R	DQ6R		DQ4R	DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFIN_R1p*	AB7	AD4	P2	DQ14R	DQ7R	DQ3R	DQ1R	DQ12R	DQ6R		DQ4R	DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	AC5	AA5	N1										
5A	RIO1	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFIN_R2n*	W8	V7	T1	DQSn14R	DQ7R	DQ3R	DQ1R	DQSn12R	DQ6R		DQSn4R	DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	AB5	V4	M1	DQ14R	DQ7R	DQ3R	DQ1R	DQ12R	DQ6R		DQ4R	DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFIN_R2p*	Y9	V6	R2	DQS14R	DQ7R/CQn7R	DQ3R	DQ1R	DQS12R	DQ6R/CQn6R		DQS4R	DQ2R/CQn2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	AB6	V5	M2										
5A	RIO1	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFIN_R3n*	AC4	AB4	M4	DQSn13R	DQSn7R/DQ7R	DQ3R	DQ1R	DQSn11R	DQSn6R/DQ6R		DQSn3R	DQSn2R/DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R3n	Y5	Y4	N3	DQ13R	DQ7R	DQ3R	DQ1R	DQ11R	DQ6R		DQ3R	DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFIN_R3p*	AB4	AA4	L5	DQS13R	DQS7R/CQ7R	DQ3R	DQ1R	DQS11R	DQS6R/CQ6R		DQS3R	DQS2R/CQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R3p	Y6	W4	M3										
5A	RIO1	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFIN_R4n*	W6	U6	N4	DQ13R	DQ7R	DQ3R	DQ1R	DQ11R	DQ6R		DQ3R	DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	AE3	AC4	L3	DQ13R	DQ7R	DQ3R	DQ1R	DQ11R	DQ6R		DQ3R	DQ2R	
5A	RIO1	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFIN_R4p*	V7	T6	M5										
5A	RIO1	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	AD3	AC3	L4	DQ13R	DQ7R	DQ3R	DQ1R	DQ11R	DQ6R		DQ3R	DQ2R	
5A	RIO2	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFIN_R5n*	AC2			DQ12R	DQ6R	DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R5n	AA3			DQ12R	DQ6R	DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFIN_R5p*	AC3			DQ12R	DQ6R	DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R5p	AA4												
5A	RIO2	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFIN_R6n*	V6			DQSn12R	DQ6R	DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	W4			DQ12R	DQ6R	DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFIN_R6p*	U6			DQS12R	DQ6R/CQn6R	DQ3R/CQn3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	W5												
5A	RIO2	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFIN_R7n*	AB2			DQSn11R	DQSn6R/DQ6R	DQSn3R/DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	Y3			DQ11R	DQ6R	DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFIN_R7p*	AB3			DQS11R	DQS6R/CQ6R	DQS3R/CQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	Y4												
5A	RIO2	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFIN_R8n*	T6			DQ11R	DQ6R	DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	AE1			DQ11R	DQ6R	DQ3R	DQ1R						
5A	RIO2	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFIN_R8p*	T7												
5A	RIO2	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	AD1			DQ11R	DQ6R	DQ3R	DQ1R						
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFIN_R9n*	AC1	AD3		DQ10R	DQ5R	DQ2R	DQ1R	DQ10R	DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	AA1	U3		DQ10R	DQ5R	DQ2R	DQ1R	DQ10R	DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFIN_R9p*	AB1	AD2		DQ10R	DQ5R	DQ2R	DQ1R	DQ10R	DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	Y1	U4											
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFIN_R10n*	N4	T4		DQSn10R	DQ5R	DQ2R	DQ1R	DQSn10R	DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	V3	Y3		DQ10R	DQ5R	DQ2R	DQ1R	DQ10R	DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFIN_R10p*	P5	T5		DQS10R	DQ5R/CQn5R	DQ2R	DQ1R/CQn1R	DQS10R	DQ5R/CQn5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	V4	W3											
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFIN_R11n*	W1	W2		DQSn9R	DQSn5R/DQ5R	DQ2R	DQSn1R/DQ1R	DQSn9R	DQSn5R/DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	W2	AB3		DQ9R	DQ5R	DQ2R	DQ1R	DQ9R	DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFIN_R11p*	V1	V3		DQS9R	DQS5R/CQ5R	DQ2R	DQS1R/CQ1R	DQS9R	DQS5R/CQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	W3	AA3											
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFIN_R12n*	R6	R5		DQ9R	DQ5R	DQ2R	DQ1R	DQ9R	DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R12n	U4	AC1		DQ9R	DQ5R	DQ2R	DQ1R	DQ9R	DQ5R	DQ2R			
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFIN_R12p*	P6	R6											

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F780	F572	U358	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16X18 for F780 (Note 3)	DQS for X32X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16X18 for F572 (Note 3)	DQS for X4 for U358	DQS for X8/X9 for U358 (Note 3)	DQS for X16X18 for U358 (Note 3)
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R12p	U5	AB2		DQ9R	DQ5R	DQ2R	DQ1R	DQ9R	DQ5R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R13n	DIFFIN_R13n*	U3	AB1		DQ8R	DQ4R	DQ2R	DQ1R	DQ8R	DQ4R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	T3	T2		DQ8R	DQ4R	DQ2R	DQ1R	DQ8R	DQ4R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R13p	DIFFIN_R13p*	T4	AA1		DQ8R	DQ4R	DQ2R	DQ1R	DQ8R	DQ4R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	R3	T3											
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R14n	DIFFIN_R14n*	N6	R7		DQSn8R	DQ4R	DQ2R	DQ1R	DQSn8R	DQ4R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R14n	DIFFOUT_R14n	U1	R3		DQ8R	DQ4R	DQ2R	DQ1R	DQ8R	DQ4R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R14p	DIFFIN_R14p*	M6	P7		DQS8R	DQ4R/CQn4R	DQ2R/CQn2R	DQ1R	DQS8R	DQ4R/CQn4R	DQ2R/CQn2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R14p	DIFFOUT_R14p	T1	R4											
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R15n	DIFFIN_R15n*	R1	V1		DQSn7R	DQSn4R/DQ4R	DQSn2R/DQ2R	DQ1R	DQSn7R	DQSn4R/DQ4R	DQSn2R/DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	R4	Y1		DQ7R	DQ4R	DQ2R	DQ1R	DQ7R	DQ4R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R15p	DIFFIN_R15p*	P1	U1		DQS7R	DQS4R/CQ4R	DQS2R/CQ2R	DQ1R	DQS7R	DQS4R/CQ4R	DQS2R/CQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	R5	W1											
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R16n	DIFFIN_R16n*	M5	N6		DQ7R	DQ4R	DQ2R	DQ1R	DQ7R	DQ4R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R16n	DIFFOUT_R16n	P3	T1		DQ7R	DQ4R	DQ2R	DQ1R	DQ7R	DQ4R	DQ2R			
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R16p	DIFFIN_R16p*	L6	N7											
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R16p	DIFFOUT_R16p	P4	R1		DQ7R	DQ4R	DQ2R	DQ1R	DQ7R	DQ4R	DQ2R			
5A		VREFB5AN0	CLK8	DIFFCLK_2n				P2	P3	L1										
6A		VREFB6AN0	CLK9	DIFFCLK_3n				N1	N3	K3										
5A		VREFB5AN0	CLK10	DIFFCLK_2p				N3	P4	L2										
6A		VREFB6AN0	CLK11	DIFFCLK_3p				M1	N4	K4										
6A	RIO5	VREFB6AN0	IO			DIFFIO_TX_R17n	DIFFIN_R17n*	L1	P1		DQ6R	DQ3R	DQ1R		DQ6R	DQ3R	DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	M2	M3		DQ6R	DQ3R	DQ1R		DQ6R	DQ3R	DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_TX_R17p	DIFFIN_R17p*	K1	N1		DQ6R	DQ3R	DQ1R		DQ6R	DQ3R	DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	L3	M4											
6A	RIO5	VREFB6AN0	IO			DIFFIO_TX_R18n	DIFFIN_R18n*	K6	M7		DQSn6R	DQ3R	DQ1R		DQSn6R	DQ3R	DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	M3	M1		DQ6R	DQ3R	DQ1R		DQ6R	DQ3R	DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_TX_R18p	DIFFIN_R18p*	L7	L7		DQS6R	DQ3R/CQn3R	DQ1R/CQn1R		DQS6R	DQ3R/CQn3R	DQ1R/CQn1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	M4	N2											
6A	RIO5	VREFB6AN0	IO			DIFFIO_TX_R19n	DIFFIN_R19n*	J2	L1		DQSn5R	DQSn3R/DQ3R	DQSn1R/DQ1R		DQSn5R	DQSn3R/DQ3R	DQSn1R/DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	J1	L3		DQ5R	DQ3R	DQ1R		DQ5R	DQ3R	DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_TX_R19p	DIFFIN_R19p*	J3	K1		DQS5R	DQS3R/CQ3R	DQS1R/CQ1R		DQS5R	DQS3R/CQ3R	DQS1R/CQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	H1	L4											
6A	RIO5	VREFB6AN0	IO			DIFFIO_TX_R20n	DIFFIN_R20n*	J6	K4		DQ5R	DQ3R	DQ1R		DQ5R	DQ3R	DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_RX_R20n	DIFFOUT_R20n	K3	K2		DQ5R	DQ3R	DQ1R		DQ5R	DQ3R	DQ1R			
6A	RIO5	VREFB6AN0	IO			DIFFIO_TX_R20p	DIFFIN_R20p*	J7	K5											
6A	RIO5	VREFB6AN0	IO			DIFFIO_RX_R20p	DIFFOUT_R20p	L4	K3		DQ5R	DQ3R	DQ1R		DQ5R	DQ3R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_TX_R21n	DIFFIN_R21n*	G1	J1		DQ4R	DQ2R	DQ1R		DQ4R	DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	E1	J3		DQ4R	DQ2R	DQ1R		DQ4R	DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_TX_R21p	DIFFIN_R21p*	F1	H1		DQ4R	DQ2R	DQ1R		DQ4R	DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	F2	J4											
6A	RIO6	VREFB6AN0	IO			DIFFIO_TX_R22n	DIFFIN_R22n*	K7	J5		DQSn4R	DQ2R	DQ1R		DQSn4R	DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_RX_R22n	DIFFOUT_R22n	D1	G1		DQ4R	DQ2R	DQ1R		DQ4R	DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_TX_R22p	DIFFIN_R22p*	J8	J6		DQS4R	DQ2R/CQn2R	DQ1R		DQS4R	DQ2R/CQn2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_RX_R22p	DIFFOUT_R22p	C1	G2											
6A	RIO6	VREFB6AN0	IO			DIFFIO_TX_R23n	DIFFIN_R23n*	J4	F1		DQSn3R	DQSn2R/DQ2R	DQ1R		DQSn3R	DQSn2R/DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	H3	H3		DQ3R	DQ2R	DQ1R		DQ3R	DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_TX_R23p	DIFFIN_R23p*	J5	E1		DQS3R	DQS2R/CQ2R	DQ1R		DQS3R	DQS2R/CQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	H4	H4											
6A	RIO6	VREFB6AN0	IO			DIFFIO_TX_R24n	DIFFIN_R24n*	K8	H6		DQ3R	DQ2R	DQ1R		DQ3R	DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_RX_R24n	DIFFOUT_R24n	K4	G3		DQ3R	DQ2R	DQ1R		DQ3R	DQ2R	DQ1R			
6A	RIO6	VREFB6AN0	IO			DIFFIO_TX_R24p	DIFFIN_R24p*	K9	H7											
6A	RIO6	VREFB6AN0	IO			DIFFIO_RX_R24p	DIFFOUT_R24p	K5	F3		DQ3R	DQ2R	DQ1R		DQ3R	DQ2R	DQ1R			
6A	RIO8	VREFB6AN0	IO		DATA7	DIFFIO_TX_R29n	DIFFIN_R29n*	B1	D1	G3	DQ2R	DQ1R			DQ2R	DQ1R		DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO		DATA6	DIFFIO_RX_R29n	DIFFOUT_R29n	C2	E3	J4	DQ2R	DQ1R			DQ2R	DQ1R		DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO		DATA5	DIFFIO_TX_R29p	DIFFIN_R29p*	A2	D2	G4	DQ2R	DQ1R			DQ2R	DQ1R		DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO		DATA4	DIFFIO_RX_R29p	DIFFOUT_R29p	C3	D3	J5										
6A	RIO8	VREFB6AN0	IO		DATA3	DIFFIO_TX_R30n	DIFFIN_R30n*	H6	G5	G6	DQSn2R	DQ1R			DQSn2R	DQ1R		DQSn2R	DQ1R	
6A	RIO8	VREFB6AN0	IO		DATA2	DIFFIO_RX_R30n	DIFFOUT_R30n	G3	G4	J3	DQ2R	DQ1R			DQ2R	DQ1R		DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO		DATA1	DIFFIO_TX_R30p	DIFFIN_R30p*	H7	G6	F6	DQS2R	DQ1R/CQn1R			DQS2R	DQ1R/CQn1R		DQS2R	DQ1R/CQn1R	
6A	RIO8	VREFB6AN0	IO		CLKUSR	DIFFIO_RX_R30p	DIFFOUT_R30p	G4	F4	H3										
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R31n	DIFFIN_R31n*	E3	C2	H1	DQSn1R	DQSn1R/DQ1R			DQSn1R	DQSn1R/DQ1R		DQSn1R	DQSn1R/DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	F3	E4	K1	DQ1R	DQ1R			DQ1R	DQ1R		DQ1R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R31p	DIFFIN_R31p*	D3	C3	J2	DQS1R	DQS1R/CQ1R			DQS1R	DQS1R/CQ1R		DQS1R	DQS1R/CQ1R	
6A	RIO8	VREFB6AN0	IO		DEV_OE	DIFFIO_RX_R31p	DIFFOUT_R31p	F4	D4	J1										
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R32n	DIFFIN_R32n*	G5	G7	F4	DQ1R	DQ1R			DQ1R	DQ1R		DQ1R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R32n	DIFFOUT_R32n	E4	C1	G1	DQ1R	DQ1R			DQ1R	DQ1R		DQ1R	DQ1R	
6A	RIO8	VREFB6AN0	IO		DEV_CLRn	DIFFIO_TX_R32p	DIFFIN_R32p*	G6	F7	F5										
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R32p	DIFFOUT_R32p	F5	B1	G2	DQ1R	DQ1R			DQ1R	DQ1R		DQ1R	DQ1R	
7A		VREFB7AN0	IO	RUP1				F7	E7	D4										
7A		VREFB7AN0	IO	PLL2_CLKOUT1p				K10	G8	F3										
7A		VREFB7AN0	IO	RDN1				G7	D7	E4										
7A		VREFB7AN0	IO	PLL2_CLKOUT1n				J9	F8	F2										
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	F9			DQ14T	DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T1p	DIFFIN_T1p*	H10												
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	F8			DQ14T	DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T1n	DIFFIN_T1n*	G10			DQ14T	DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T2p	F10												
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFIN_T2p*	E8			DQS14T	DQS7T/CQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	E10			DQ14T	DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFIN_T2n*	D5			DQSn14T	DQSn7T/DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	D4												
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T3p	DIFFIN_T3p*	K11			DQS13T	DQ7T/CQn7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	C4			DQ13T	DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T3n	DIFFIN_T3n*	J10			DQSn13T	DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T4p	B3												
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFIN_T4p*	A5			DQ13T	DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	A3			DQ13T	DQ7T	DQ3T	DQ1T						
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFIN_T4n*	A4			DQ13T	DQ7T	DQ3T	DQ1T						
7A	TIO6	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	E7	D6	D2	DQ12T	DQ6T	DQ3T	DQ1T	DQ8T	DQ4T	DQ2T	DQ6T	DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_TX_T5p	DIFFIN_T5p*	G11	H9	E1										
7A	TIO6	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	D7	C6	D1	DQ12T	DQ6T	DQ3T	DQ1T	DQ8T	DQ4T	DQ2T	DQ6T	DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_TX_T5n	DIFFIN_T5n*	F11	G9	F1	DQ12T	DQ6T	DQ3T	DQ1T	DQ8T	DQ4T	DQ2T	DQ6T	DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T6p	D6	B3	C2										
7A	TIO6	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFIN_T6p*	E9	C4	D3	DQS12T	DQS6T/CQ6T	DQS37/CQ3T	DQ1T	DQS8T	DQS4T/CQ4T	DQ2T	DQS6T	DQS37/CQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T6n	C5	A4	C1	DQ12T	DQ6T	DQ3T	DQ1T	DQ8T	DQ4T	DQ2T	DQ6T	DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFIN_T6n*	D9	B4	C3	DQSn12T	DQSn6T/DQ6T	DQSn37/DQ3T	DQ1T	DQSn8T	DQSn4T/DQ4T	DQ2T	DQSn6T	DQSn37/DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	C7	A3	C5										
7A	TIO6	VREFB7AN0	IO			DIFFIO_TX_T7p	DIFFIN_T7p*	J12	F9	E7	DQS11T	DQ6T/CQn6T	DQ3T/CQn3T	DQ1T	DQS7T	DQ4T/CQn4T	DQ2T	DQS5T	DQ3T/CQn3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	C6	A2	C4	DQ11T	DQ6T	DQ3T	DQ1T	DQ7T	DQ4T	DQ2T	DQ5T	DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_TX_T7n	DIFFIN_T7n*	J11	E9	D7	DQSn11T	DQ6T	DQ3T	DQ1T	DQSn7T	DQ4T	DQ2T	DQSn5T	DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	D8	D8	A1										
7A	TIO6	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFIN_T8p*	D10	A6	A3	DQ11T	DQ6T	DQ3T	DQ1T	DQ7T	DQ4T	DQ2T	DQ5T	DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	C8	C7	B1	DQ11T	DQ6T	DQ3T	DQ1T	DQ7T	DQ4T	DQ2T	DQ5T	DQ3T	DQ1T
7A	TIO6	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFIN_T8n*	C10	A5	A2	DQ11T	DQ6T	DQ3T	DQ1T	DQ7T	DQ4T	DQ2T	DQ5T	DQ3T	DQ1T
7A	TIO5	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	E12			DQ10T	DQ5T	DQ2T	DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_TX_T9p	DIFFIN_T9p*	G12												
7A	TIO5	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	D12			DQ10T	DQ5T	DQ2T	DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_TX_T9n	DIFFIN_T9n*	F12			DQ10T	DQ5T	DQ2T	DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	C9												

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F780	F572	U358	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16X18 for F780 (Note 3)	DQS for X32X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16X18 for F572 (Note 3)	DQS for X4 for U358	DQS for X8/X9 for U358 (Note 3)	DQS for X16X18 for U358 (Note 3)
7A	TIO5	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFIN_T10p*	D11			DQS10T	DQS5T/CQ5T	DQ2T	DQS1T/CQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	B9			DQ10T	DQ5T	DQ2T	DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFIN_T10n*	C11			DQSn10T	DQSn5T/DQ5T	DQ2T	DQSn1T/DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	G13												
7A	TIO5	VREFB7AN0	IO			DIFFIO_TX_T11p	DIFFIN_T11p*	K13			DQS9T	DQ5T/CQn5T	DQ2T	DQ1T/CQn1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	F13			DQ9T	DQ5T	DQ2T	DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_TX_T11n	DIFFIN_T11n*	K12			DQSn9T	DQ5T	DQ2T	DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_RX_T12p	DIFFOUT_T12p	E13												
7A	TIO5	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFIN_T12p*	C13			DQ9T	DQ5T	DQ2T	DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_RX_T12n	DIFFOUT_T12n	D13			DQ9T	DQ5T	DQ2T	DQ1T						
7A	TIO5	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFIN_T12n*	C12			DQ9T	DQ5T	DQ2T	DQ1T						
7A	TIO4	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	B6	D9	B4	DQ8T	DQ4T	DQ2T	DQ1T	DQ6T	DQ3T	DQ2T	DQ4T	DQ2T	DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_TX_T13p	DIFFIN_T13p*	K14	G11	C7										
7A	TIO4	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	A6	C9	A4	DQ8T	DQ4T	DQ2T	DQ1T	DQ6T	DQ3T	DQ2T	DQ4T	DQ2T	DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_TX_T13n	DIFFIN_T13n*	J14	G10	C6	DQ8T	DQ4T	DQ2T	DQ1T	DQ6T	DQ3T	DQ2T	DQ4T	DQ2T	DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	A10	A8	A6										
7A	TIO4	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFIN_T14p*	A8	B7	C9	DQS8T	DQS4T/CQ4T	DQS2T/CQ2T	DQ1T	DQS6T	DQS3T/CQ3T	DQS2T/CQ2T	DQS4T	DQS2T/CQ2T	DQS1T/CQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	A9	A7	A5	DQ8T	DQ4T	DQ2T	DQ1T	DQ6T	DQ3T	DQ2T	DQ4T	DQ2T	DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFIN_T14n*	A7	B6	C8	DQSn8T	DQSn4T/DQ4T	DQSn2T/DQ2T	DQ1T	DQSn6T	DQSn3T/DQ3T	DQSn2T/DQ2T	DQSn4T	DQSn2T/DQ2T	DQSn1T/DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	B12	D10	B6										
7A	TIO4	VREFB7AN0	IO			DIFFIO_TX_T15p	DIFFIN_T15p*	G14	F10	B10	DQS7T	DQ4T/CQn4T	DQ2T/CQn2T	DQ1T	DQS5T	DQ3T/CQn3T	DQ2T/CQn2T	DQS3T	DQ2T/CQn2T	DQ1T/CQn1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	A11	C10	A7	DQ7T	DQ4T	DQ2T	DQ1T	DQ5T	DQ3T	DQ2T	DQ3T	DQ2T	DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_TX_T15n	DIFFIN_T15n*	F14	E10	A10	DQSn7T	DQ4T	DQ2T	DQ1T	DQSn5T	DQ3T	DQ2T	DQS3T	DQ2T	DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	A13	B9	B7										
7A	TIO4	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFIN_T16p*	A15	B10	B9	DQ7T	DQ4T	DQ2T	DQ1T	DQ5T	DQ3T	DQ2T	DQ3T	DQ2T	DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	A12	A9	A8	DQ7T	DQ4T	DQ2T	DQ1T	DQ5T	DQ3T	DQ2T	DQ3T	DQ2T	DQ1T
7A	TIO4	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFIN_T16n*	A14	A10	A9	DQ7T	DQ4T	DQ2T	DQ1T	DQ5T	DQ3T	DQ2T	DQ3T	DQ2T	DQ1T
8A		VREFB8AN0	CLK12	DIFFCLK_4p				D15	D11	D10										
7A		VREFB7AN0	CLK13	DIFFCLK_5p				D14	F12	E10										
8A		VREFB8AN0	CLK14	DIFFCLK_4n				C15	C11	C10										
7A		VREFB7AN0	CLK15	DIFFCLK_5n				C14	F11	D9										
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	C16	E12		DQ6T	DQ3T	DQ1T		DQ4T	DQ2T	DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T17p	DIFFIN_T17p*	F16	E13											
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	B15	D12		DQ6T	DQ3T	DQ1T		DQ4T	DQ2T	DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T17n	DIFFIN_T17n*	F15	D13		DQ6T	DQ3T	DQ1T		DQ4T	DQ2T	DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T18p	DIFFOUT_T18p	A18	C12											
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T18p	DIFFIN_T18p*	B16	A12		DQS6T	DQS3T/CQ3T	DQS1T/CQ1T		DQS4T	DQS2T/CQ2T	DQS1T/CQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	A17	B12		DQ6T	DQ3T	DQ1T		DQ4T	DQ2T	DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T18n	DIFFIN_T18n*	A16	A11		DQSn6T	DQSn3T/DQ3T	DQSn1T/DQ1T		DQSn4T	DQSn2T/DQ2T	DQSn1T/DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	E15	B13											
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T19p	DIFFIN_T19p*	H15	G13		DQS5T	DQ3T/CQn3T	DQ1T/CQn1T		DQS3T	DQ2T/CQn2T	DQ1T/CQn1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	D16	A13		DQ5T	DQ3T	DQ1T		DQ3T	DQ2T	DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T19n	DIFFIN_T19n*	G15	F13		DQSn5T	DQ3T	DQ1T		DQSn3T	DQ2T	DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	A20	D14											
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T20p	DIFFIN_T20p*	C19	B15		DQ5T	DQ3T	DQ1T		DQ3T	DQ2T	DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	A19	C13		DQ5T	DQ3T	DQ1T		DQ3T	DQ2T	DQ1T			
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T20n	DIFFIN_T20n*	B19	A14		DQ5T	DQ3T	DQ1T		DQ3T	DQ2T	DQ1T			
8A	TIO2	VREFB8AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	D17			DQ4T	DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_TX_T21p	DIFFIN_T21p*	L15												
8A	TIO2	VREFB8AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	C17			DQ4T	DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_TX_T21n	DIFFIN_T21n*	K15			DQ4T	DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	D18												
8A	TIO2	VREFB8AN0	IO			DIFFIO_TX_T22p	DIFFIN_T22p*	D21			DQS4T	DQS2T/CQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_RX_T22n	DIFFOUT_T22n	C18			DQ4T	DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_TX_T22n	DIFFIN_T22n*	C21			DQSn4T	DQSn2T/DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	D20												
8A	TIO2	VREFB8AN0	IO			DIFFIO_TX_T23p	DIFFIN_T23p*	G17			DQS3T	DQ2T/CQn2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D19			DQ3T	DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_TX_T23n	DIFFIN_T23n*	F17			DQSn3T	DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T24p	L19												
8A	TIO2	VREFB8AN0	IO			DIFFIO_TX_T24p	DIFFIN_T24p*	J21			DQ3T	DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T24n	K20			DQ3T	DQ2T	DQ1T							
8A	TIO2	VREFB8AN0	IO			DIFFIO_TX_T24n	DIFFIN_T24n*	J20			DQ3T	DQ2T	DQ1T							
8A	TIO1	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	F22	D15	B12	DQ2T	DQ1T			DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_TX_T25p	DIFFIN_T25p*	K16	G14	D11										
8A	TIO1	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	E22	C15	A11	DQ2T	DQ1T			DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_TX_T25n	DIFFIN_T25n*	J16	E14	C12	DQ2T	DQ1T			DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	G24	C16	A14										
8A	TIO1	VREFB8AN0	IO			DIFFIO_TX_T26p	DIFFIN_T26p*	F24	A16	B13	DQS2T	DQS1T/CQ1T			DQS2T	DQS1T/CQ1T	DQ1T	DQS2T	DQS1T/CQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	F23	B16	A13	DQ2T	DQ1T			DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_TX_T26n	DIFFIN_T26n*	E24	A15	A12	DQSn2T	DQSn1T/DQ1T			DQSn2T	DQSn1T/DQ1T	DQ1T	DQSn2T	DQSn1T/DQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	F21	A18	C14										
8A	TIO1	VREFB8AN0	IO			DIFFIO_TX_T27p	DIFFIN_T27p*	K18	F15	D13	DQS1T	DQ1T/CQn1T			DQS1T	DQ1T/CQn1T	DQ1T	DQS1T	DQ1T/CQn1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	E21	A17	C13	DQ1T	DQ1T			DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_TX_T27n	DIFFIN_T27n*	J17	E15	D12	DQSn1T	DQ1T			DQSn1T	DQ1T	DQ1T	DQSn1T	DQ1T	
8A	TIO1	VREFB8AN0	IO		CRC_ERROR	DIFFIO_RX_T28p	DIFFOUT_T28p	E19	C19	A16										
8A	TIO1	VREFB8AN0	IO			DIFFIO_TX_T28p	DIFFIN_T28p*	G19	A20	C15	DQ1T	DQ1T			DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_RX_T28n	DIFFOUT_T28n	E18	B18	A15	DQ1T	DQ1T			DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	
8A	TIO1	VREFB8AN0	IO			DIFFIO_TX_T28n	DIFFIN_T28n*	G18	A19	B15	DQ1T	DQ1T			DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	
8A		VREFB8AN0	IO	RUP2				L21	C20	D15										
8A		VREFB8AN0	IO	PLL1_CLKOUT1p				K19	H16	A18										
8A		VREFB8AN0	IO	RDN2				K21	B19	D14										
8A		VREFB8AN0	IO	PLL1_CLKOUT1n				J18	G16	A17										
8C			TDO		TDO			L23	G20	B16										
8C			ASDO		ASDO			J22	J20	C16										
8C			nCSO		nCSO			H22	H19	E18										
8C			DATA0		DATA0			K22	J19	G17										
8C			TDI		TDI			H24	G19	C17										
8C			TMS		TMS			J23	G17	C18										
8C			TCK		TCK			L24	D18	D16										
8C			DCLK		DCLK			K24	F20	K17										
			GND					P14	M12	K10										
			GND					AB21	T18	R17										
			GND					G22	D20	J17										
			GND					K23	D19	H17										
			GND					Y28	Y24	Y20										
			GND					Y27	Y23	Y18										
			GND					W26	W22	Y16										
			GND					W25	W21	W20										
			GND					V28	V24	W19										
			GND					V27	V23	W18										
			GND					U26	U22	W16										
			GND					U25	U21	V17										
			GND					T28	T24	U20										
			GND					T27	T23	U19										
			GND					T24	R22	R20										
			GND					T22	R21	R19										
			GND					R26	R19	N20										
			GND					R25	P24	N19										
			GND					R23	P23	N18										

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F780	F572	U358	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16X18 for F780 (Note 3)	DQS for X32X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16X18 for F572 (Note 3)	DQS for X4 for U358	DQS for X8/X9 for U358 (Note 3)	DQS for X16X18 for U358 (Note 3)
			GND					R21	P20	L20										
			GND					P28	N22	L18										
			GND					P27	N21	J20										
			GND					P24	N19	J19										
			GND					P22	M24	H18										
			GND					N26	M23	G20										
			GND					N25	M20	G19										
			GND					N23	L22	F18										
			GND					N21	L21	E20										
			GND					M28	L19	E19										
			GND					M27	K24	C20										
			GND					M24	K23	C19										
			GND					L26	K20	B18										
			GND					L25	J22	A20										
			GND					K28	J21	A19										
			GND					K27	H24	N13										
			GND					J26	H23	M8										
			GND					J25	G22	M12										
			GND					H28	G21	L9										
			GND					H27	F24	L13										
			GND					G26	F23	K5										
			GND					G25	E22	K14										
			GND					F28	E21	J9										
			GND					F27	D24	J13										
			GND					E26	D23	H8										
			GND					E25	C22	H2										
			GND					D28	C21	H12										
			GND					D27	B24	G11										
			GND					D24	B23	E5										
			GND					D22	AD23	E17										
			GND					C26	AC23	E11										
			GND					C25	AB24	B5										
			GND					C24	AB23	B17										
			GND					C22	AB22	B11										
			GND					B28	AA22	W8										
			GND					B27	AA21	W5										
			GND					B25	A23	W2										
			GND					B23	A22	W14										
			GND					B22	A21	W11										
			GND					B21	Y8	T8										
			GND					AH26	Y5	T5										
			GND					AH24	Y20	T2										
			GND					AH22	Y2	T17										
			GND					AH20	Y17	T14										
			GND					AG28	Y14	T11										
			GND					AG26	Y11	P12										
			GND					AG24	W6	N9										
			GND					AG22	W18	N5										
			GND					AG21	U8	N2										
			GND					AG20	U5	N15										
			GND					AF28	U20	N11										
			GND					AF27	U2	M14										
			GND					AF26	U17	M10										
			GND					AF25	U14	L15										
			GND					AF23	U11	K8										
			GND					AE26	T14	K2										
			GND					AE25	T12	K12										
			GND					AE23	T10	J15										
			GND					AD28	R9	J11										
			GND					AD27	R17	H5										
			GND					AC26	R15	H14										
			GND					AC25	R13	H10										
			GND					AB28	R11	E8										
			GND					AB27	P8	E2										
			GND					AA26	P5	E14										
			GND					AA25	P2	B8										
			GND					A27	P16	B2										
			GND					A25	P14	B14										
			GND					A23	P12											
			GND					A21	N9											
			GND					Y7	N15											
			GND					W9	M8											
			GND					W22	M14											
			GND					W19	L5											
			GND					W17	L15											
			GND					W15	K8											
			GND					V8	K12											
			GND					V5	J15											
			GND					V20	H5											
			GND					V2	H14											
			GND					V18	E8											
			GND					V16	E17											
			GND					V14	B5											
			GND					V12	B14											
			GND					V10	AC20											
			GND					U9	AC11											
			GND					U17	J17											
			GND					U13	H8											
			GND					T8	H17											
			GND					T20	F18											
			GND					T18	E2											
			GND					T14	B8											
			GND					T10	B17											
			GND					R19	AC5											
			GND					R13	AC14											
			GND					P18	P10											
			GND					P12	N17											
			GND					N9	N11											
			GND					N5	M16											
			GND					N19	L9											
			GND					N15	L17											
			GND					N11	L11											
			GND					M16	K14											
			GND					M12	J9											
			GND					L8	J11											
			GND					L20	H2											
			GND					L17	F6											
			GND					L11	E20											
			GND					H5	E11											
			GND					H17	B2											

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F780	F572	U358	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16X18 for F780 (Note 3)	DQS for X32X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16X18 for F572 (Note 3)	DQS for X4 for U358	DQS for X8/X9 for U358 (Note 3)	DQS for X16X18 for U358 (Note 3)
			GND					G9	AC8											
			GND					E20	AC17											
			GND					E11	N13											
			GND					B2	M18											
			GND					AG8	M10											
			GND					AG14	L2											
			GND					AD20	L13											
			GND					AD11	K16											
			GND					AA20	K10											
			GND					AA11	J13											
			GND					U19	H20											
			GND					U15	H11											
			GND					U11	E5											
			GND					T5	E14											
			GND					T2	B20											
			GND					T16	B11											
			GND					T12	AC2											
			GND					R9												
			GND					R17												
			GND					R11												
			GND					P16												
			GND					P10												
			GND					N8												
			GND					N2												
			GND					N17												
			GND					N13												
			GND					M18												
			GND					M14												
			GND					M10												
			GND					L5												
			GND					L2												
			GND					L14												
			GND					H8												
			GND					H2												
			GND					H11												
			GND					E23												
			GND					E14												
			GND					B20												
			GND					B11												
			GND					AG17												
			GND					AD5												
			GND					AD14												
			GND					AA5												
			GND					AA14												
			GND					H20												
			GND					H14												
			GND					E5												
			GND					E17												
			GND					B5												
			GND					B14												
			GND					AG2												
			GND					AD8												
			GND					AD17												
			GND					AA8												
			GND					AA17												
			GND					E8												
			GND					E2												
			GND					B8												
			GND					B17												
			GND					AG5												
			GND					AG11												
			GND					AD2												
			GND					AB23												
			GND					AA2												
			VCC					P15	M13	L10										
			VCC					W20	U12	P11										
			VCC					W18	T9	N8										
			VCC					W16	T17	N14										
			VCC					W14	T15	N12										
			VCC					V9	T13	N10										
			VCC					V21	T11	M9										
			VCC					V19	R8	M15										
			VCC					V17	R16	M13										
			VCC					V15	R14	M11										
			VCC					V13	R12	L8										
			VCC					V11	R10	L14										
			VCC					U20	P9	L12										
			VCC					U18	P17	K9										
			VCC					U16	P15	K15										
			VCC					U14	P13	K13										
			VCC					U12	P11	K11										
			VCC					U10	N8	J8										
			VCC					T9	N18	J14										
			VCC					T19	N16	J12										
			VCC					T17	N14	J10										
			VCC					T15	N10	H9										
			VCC					T13	M9	H15										
			VCC					T11	M15	H13										
			VCC					R18	M11	H11										
			VCC					R16	L8											
			VCC					R14	L16											
			VCC					R12	L14											
			VCC					R10	L12											
			VCC					P9	L10											
			VCC					P19	K9											
			VCC					P17	K17											
			VCC					P13	K15											
			VCC					P11	K13											
			VCC					N20	K11											
			VCC					N18	J8											
			VCC					N16	J18											
			VCC					N14	J16											
			VCC					N12	J14											
			VCC					N10	J12											
			VCC					M9	J10											
			VCC					M20	H15											
			VCC					M19												
			VCC					M17												
			VCC					M15												
			VCC					M13												

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F780	F572	U358	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16X18 for F780 (Note 3)	DQS for X32X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16X18 for F572 (Note 3)	DQS for X4 for U358	DQS for X8/X9 for U358 (Note 3)	DQS for X16X18 for U358 (Note 3)
			VCC					M11												
			VCC					L18												
			VCC					L16												
			VCC					L13												
			VCC					L12												
			VCC					L10												
			VCC					K17												
			DNU					H23	G18	F17										
			DNU					R15	N12	L11										
			DNU					F6	D5	D6										
			VCCBAT					J24	F19	F16										
			VCCA_PLL_1					G20	F17	D17										
			VCCA_PLL_2					H9	E6	D5										
			VCCA_PLL_3					Y8	Y6	U5										
			VCCA_PLL_4					AB20	W17	U17										
			VCCD_PLL_1					H21	E18	E16										
			VCCD_PLL_2					G8	F5	E6										
			VCCD_PLL_3					AA7	W5	T6										
			VCCD_PLL_4					AA21	Y18	T16										
			VCCIO3A					AG16	AC16	V11										
			VCCIO3A					AD19	AA17	T12										
			VCCIO3A					AD16												
			VCCIO3C					AC20	V19	T15										
			VCCIO4A					AG7	Y10	W3										
			VCCIO4A					AG13	AC7	U8										
			VCCIO4A					AG10	AC10	T3										
			VCCIO4A					AD13												
			VCCIO4A					AD10												
			VCCIO5A					Y2	V2	P5										
			VCCIO5A					U2	R2											
			VCCIO5A					R2	AA2											
			VCCIO5A					AE2												
			VCCIO6A					K2	M2	H4										
			VCCIO6A					G2	J2											
			VCCIO6A					D2	F2											
			VCCIO7A					B7	C8	D8										
			VCCIO7A					B4	C5	B3										
			VCCIO7A					B13		E3										
			VCCIO7A					B10												
			VCCIO8A					F18	D16	E12										
			VCCIO8A					E16	C17	C11										
			VCCIO8A					C20	C14											
			VCCIO8A					B18												
			VCCIO8C					G23	E19	E15										
			VCCPD3A					AB18	U15	R12										
			VCCPD3A					AA18												
			VCCPD3C					Y21	V17	R14										
			VCCPD4A					AA13	U10	R8										
			VCCPD4A					AA12												
			VCCPD5A					U8	T8	N6										
			VCCPD5A					U7	T7											
			VCCPD6A					M8	K7	H6										
			VCCPD6A					M7	K6											
			VCCPD7A					J13	H10	F8										
			VCCPD7A					H13												
			VCCPD8A					H16	H13	F12										
			VCCPD8A					G16												
			VCCPD8C					G21	H18	F14										
3A		VREFB3AN0	VREFB3AN0	VREFB3AN0				Y17	T16	T13										
4A		VREFB4AN0	VREFB4AN0	VREFB4AN0				AB12	V10	T9										
5A		VREFB5AN0	VREFB5AN0	VREFB5AN0				W7	U7	R5										
6A		VREFB6AN0	VREFB6AN0	VREFB6AN0				L9	J7	G5										
7A		VREFB7AN0	VREFB7AN0	VREFB7AN0				H12	H12	E9										
8A		VREFB8AN0	VREFB8AN0	VREFB8AN0				H18	G15	E13										
			NC					AF21	AD22	U18										
			NC					AF22	AC22	V18										
			NC					U21	P6											
			NC					AB8	N5											
			NC					AA9	L6											
			NC					R24	M5											
			NC					H19	W7											
			NC					AC8	V8											
			NC					T21	E16											
			NC					F19	Y7											
			NC					AB9	C18											
			NC					T23	W8											
			NC					J19	F16											
			NC					F20	D17											
			NC					R7	M17											
			NC					R8												
			NC					P8												
			NC					P7												
			NC					P20												
			NC					E27												
			NC					E28												
			NC					D25												
			NC					D26												
			NC					G27												
			NC					G28												
			NC					F25												
			NC					F26												
			NC					J27												
			NC					J28												
			NC					H25												
			NC					H26												
			NC					B24												
			NC					A24												
			NC					D23												
			NC					C23												
			NC					C27												
			NC					C28												
			NC					B26												
			NC					A26												
			NC					A22												
			VCCL_GXB					R22	M19	M18										
			VCCL_GXB					P23	L20	L19										
			VCCL_GXB					P21	K19	J18										
			VCCL_GXB					N24	R20											
			VCCL_GXB					N22	P19											
			VCCL_GXB					M23	N20											

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F780	F572	U358	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16X18 for F780 (Note 3)	DQS for X32X36 for F780 (Note 3)	DQS for X4 for F572	DQS for X8/X9 for F572 (Note 3)	DQS for X16X18 for F572 (Note 3)	DQS for X4 for U358	DQS for X8/X9 for U358 (Note 3)	DQS for X16X18 for U358 (Note 3)
			VCCCB					Y15	U13	R11										
			VCCCB					N7	M6	K6										
			VCCCB					J15	G12	F11										
			RREF0					AH21	AC24	Y19										
			VCCA					R20	P18	P18										
			VCCA					M21	L18	G18										
			VCCH_GXB					U23	R18	T18										
			VCCH_GXB					U22	K18	D18										
			VCCH_GXB					M22												
			VCCH_GXB					L22												

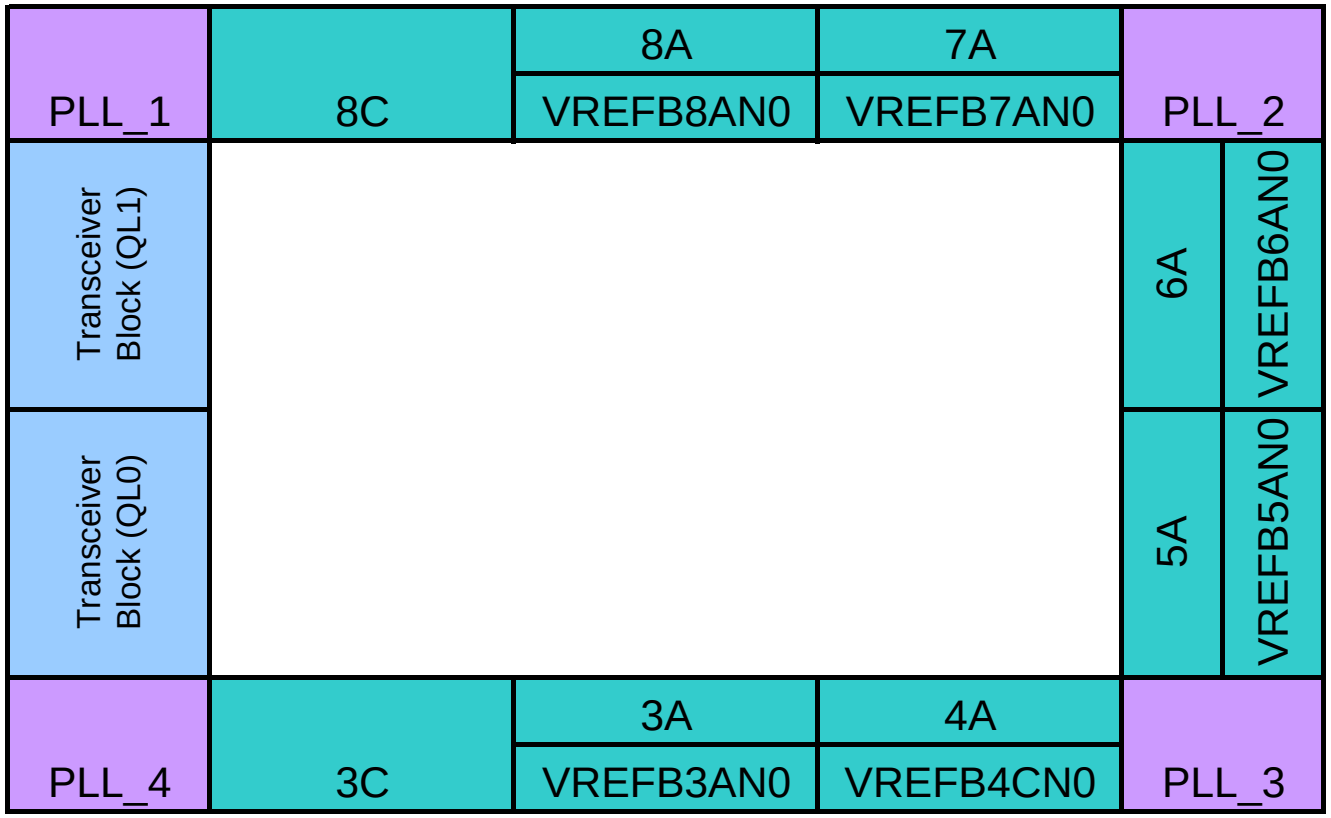
Notes:
(1) An I/O module is a group of 16 I/O pins.
(2) When not used as DIFFIN or DIFFIO_TX, all pins marked with * (DIFFIN_[#/#]p/n) can be configured as emulated LVDS output channels (DIFFOUT).
Only DIFFIN pins of the same index group (e.g DIFFIN_B1p and DIFFIN_B1n) can be used to form an emulated LVDS output channel.
(3) When not used as clocks, the CQn and DQSn pins can be used as DQ pins.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Clock and PLL Pins		
CLK[4:15]	Clock, Input	Single ended clock input pin.
DIFFCLK[0:5]p	Clock, Input	Clock input pin for differential clock input. OCT Rd is not supported.
DIFFCLK[0:5]n	Clock, Input	Negative clock input for differential clock input. OCT Rd is not supported
PLL_[1:4]_CLKOUT1p	I/O, Clock	PLL[1:4]_CLKOUT1 (except PLL1 and PLL3 in EP2AGX125 and EP2AGX260) supports 2 clock I/O pins, configured either as one single ended I/O or one differential I/O pair. PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1:4]_CLKOUT1n	I/O, Clock	
PLL_[1.3]_CLKOUT[2:3]p (Note 4)	I/O, Clock	PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1.3]_CLKOUT[2:3]n (Note 4)	I/O, Clock	
Dedicated Configuration/JTAG Pins		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5V, 1.8V, 2.5V, 3.0V or3.3V) turns off the weak pull-up, while a logic low turns them on.
MSEL[0:3]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as an user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
Optional/Dual-Purpose Configuration Pins		
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	I/O (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	Input	DATA[0] is a dedicated pin that is used for both the passive and active configuration modes
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration. DATA[1:7] pins can also be used as user I/O pins after configuration, but not DATA0.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX_[T,B,R][##]p, DIFFIO_RX_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels with OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX_[T,B,R][##]p, DIFFIO_TX_[T,B,R][##]n	I/O, TX channel	These are true LVDS transmitter channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS transmitter channels, these pins can be configured as true LVDS receiver channels without OCT Rd support (DIFFIN_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pins.
DIFFIN_[T,B,R][##]p, DIFFIN_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels without OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS receiver channels without OCT Rd support, these pins can be configured as true LVDS transmitter channels (DIFFIO_TX_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pin.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, {DIFFIO_RX_[T,B,R][##][p,n] , DIFFIN_[T,B,R][##][p,n]} can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[##][T,B,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B,R] (Note 5)	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[##][T,B,R] (Note 5)	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[0:2]	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[0:2]	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do Not Use (DNU).
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[1:6]	Power	Digital power for PLL[1:6]. All of these pins must be connected even if the PLL is not used
VCCCB	Power	Configuration RAM bits power supply.
VCCA_PLL_[1:6]	Power	Analog power for PLL [1:6]. All of these pins must be connected even if the PLL is not used
VCCIO[3:8][A,B]	Power	These are I/O supply voltage pins for banks 3 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V,3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), 3.0V PCI/PCI-X and LVTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards.
VCCIO[3,8]C	Power	These are configuration and JTAG supply voltage pins for banks 3C and 8C. Each bank can support a different voltage level. For AS/PP/FPP configuration schemes, VCCIO8C supports 1.8V, 2.5V, 3.0V or 3.3V. JTAG can support 1.5V, 1.8V, 2.5V, 3.0V or 3.3V.
VCCPD[3:8][A,B], VCCPD[3,8]C	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the input buffers for HSTL/SSTL input buffers. This can be connected to 3.3V, 3.0V or 2.5V. For 3.3V I/O standard connect VCCPD to 3.3V, for 3.0V I/O standard connect VCCPD to 3.0V and for 2.5V/1.8V/1.2V I/O standards connect VCCPD to 2.5V
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[3:8][A,B]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. These pins cannot be used as regular I/Os.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Transceiver Pins		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA	Power	Supplies power to the transceiver PMA regulator.
GXB_RX[0:15]p (Note 6)	Input	High speed positive differential receiver channels.
GXB_RX[0:15]n (Note 6)	Input	High speed negative differential receiver channels.
GXB_TX[0:15]p (Note 6)	Output	High speed positive differential transmitter channels.
GXB_TX[0:15]n (Note 6)	Output	High speed negative differential transmitter channels.
REFCLK[0:7]p	Input	High speed differential reference clock positive.
REFCLK[0:7]n	Input	High speed differential reference clock complement.
RREF[0:1]	Input	Reference resistor for transceiver.

Notes:

1. Refer to the Arria II GX Device Datasheet and Pin Connection Guidelines for the recommended operating conditions.
2. This pin definition is prepared based on the EP2AGX260.
3. Some of the pull-up /pull down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
   The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
   Refer to the Configuring Arria II GX Devices chapter in the Arria II GX Device Handbook for more information.
4. PLL[1,3]_CLKOUT[2..3][p,n] are only available in PLL1 and PLL3 in EP2AGX125 and EP2AGX260.
5. When not used as clocks, the CQn and DQSn pins can be used as DQ pin.
6. Transceiver signals GXB_RX[15..0] and GXB_TX[15..0] are device specific.



This is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Version Number	Date	Changes Made
1.0	2/27/2009	Initial release.
1.1	5/29/2009	Added DNU in Pin List and Pin Definitions.