Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
QL3			GXB_TX15n					B32									
QL3			GXB_TX15p					B31									
QL3			GXB_RX15n					C34									
QL3			GXB_RX15p					C33									
QL3			GXB_TX14n					D32									
QL3			GXB_TX14p					D31									
QL3			GXB_RX14n					E34									
QL3			GXB_RX14p					E33									
QL3			REFCLK7n					L30									
QL3			REFCLK7p					L29									
QL3			REFCLK3n					N30									
QL3			REFCLK3p					N29									
QL3			GXB_TX13n					F32									
QL3			GXB_TX13p					F31									
QL3			GXB_RX13n					G34									
QL3			GXB_RX13p					G33									
QL3			GXB_TX12n					H32									
QL3			GXB_TX12p					H31									
QL3			GXB_RX12n					J34									
QL3			GXB_RX12p					J33									
QL2			GXB_TX11n					K32	C23								
QL2			GXB_TX11p					K31	D23								
QL2			GXB_RX11n					L34	A24								
QL2			GXB_RX11p					L33	B24								
QL2			GXB_TX10n					M32	A26								
QL2			GXB_TX10p					M31	B26								
QL2			GXB_RX10n					N34	C28								
QL2			GXB_RX10p					N33	C27								
QL2			REFCLK6n					R30	D26								
QL2			REFCLK6p					R29	D25								
QL2			REFCLK2n					U30	E28								
QL2			REFCLK2p					U29	E27								
QL2			GXB_TX9n					P32	F26								
QL2			GXB_TX9p					P31	F25								
QL2			GXB_RX9n					R34	G28								
QL2			GXB_RX9p					R33	G27								
QL2			GXB_TX8n					T32	H26								
QL2			GXB_TX8p					T31	H25								
QL2			GXB_RX8n					U34	J28								
QL2			GXB_RX8p					U33	J27								
QL1			GXB_TX7n					V32	K26								
QL1			GXB_TX7p					V31	K25								
QL1			GXB_RX7n					W34	L28								
QL1			GXB_RX7p					W33	L27								
QL1			GXB_TX6n					Y32	M26								
QL1			GXB_TX6p					Y31	M25								
QL1			GXB_RX6n					AA34	N28								
QL1			GXB_RX6p					AA33	N27								
QL1			REFCLK5n					W30	P26								
QL1			REFCLK5p					W29	P25								
QL1			REFCLK1n					AA30	R28								
QL1			REFCLK1p					AA29	R27								
QL1			GXB_TX5n					AB32	T26								
QL1			GXB_TX5p					AB31	T25								
QL1			GXB_RX5n					AC34	U28								
QL1			GXB_RX5p					AC33	U27								
QL1			GXB_TX4n					AD32	V26								
QL1			GXB_TX4p					AD31	Y25								
QL1			GXB_RX4n					AE34	W28								
QL1			GXB_RX4p					AE33	W27								
QL0			GXB_TX3n					AF32	Y26								
QL0			GXB_TX3p					AF31	Y25								
QL0			GXB_RX3n					AG34	AA28								
QL0			GXB_RX3p					AG33	AA27								
QL0			GXB_TX2n					AH32	AB26								
QL0			GXB_TX2p					AH31	AB25								
QL0			GXB_RX2n					AJ34	AC28								
QL0			GXB_RX2p					AJ33	AC27								
QL0			REFCLK4n					AC30	AD26								
QL0			REFCLK4p					AC29	AD25								
QL0			REFCLK0n					AE30	AE28								
QL0			REFCLK0p					AE29	AE27								
QL0			GXB_TX1n					AK32	AH27								
QL0			GXB_TX1p					AK31	AG27								
QL0			GXB_RX1n					AL34	AH25								
QL0			GXB_RX1p					AL33	AG25								
QL0			GXB_TX0n					AM32	AF24								
QL0			GXB_TX0p					AM31	AE24								
QL0			GXB_RX0n					AN34	AH23								
QL0			GXB_RX0p					AN33	AG23								
3C			nCONFIG		nCONFIG			AC26	AA24								
3C			CONF_DONE		CONF_DONE			AE25	AA23								
3C			MSEL3		MSEL3			AB26	AB24								
3C			MSEL2		MSEL2			AD24	Y24								
3C			MSEL1		MSEL1			AC25	Y23								
3C			MSEL0		MSEL0			AC27	W24								
3C			nSTATUS		nSTATUS			AD28	W23								
3C			nIO_PULLUP		nIO_PULLUP			AC28	AB22								
3C			nCE		nCE			AB25	AA22								
3B	BIO1	VREFB3BN0	IO			DIFFIO_TX_B1n	DIFFIN_B1n*	AH26		DQ24B	DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_RX_B1n	DIFFOUT_B1n	AG24		DQ24B	DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_TX_B1p	DIFFIN_B1p*	AG27		DQ24B	DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_RX_B1p	DIFFOUT_B1p	AF25									
3B	BIO1	VREFB3BN0	IO			DIFFIO_TX_B2n	DIFFIN_B2n*	AD22		DQSn24B	DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	AF27		DQ24B	DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_TX_B2p	DIFFIN_B2p*	AC22		DQS24B	DQ12B/CQn12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	AE28									
3B	BIO1	VREFB3BN0	IO			DIFFIO_TX_B3n	DIFFIN_B3n*	AH29		DQSn23B	DQSn12B/DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_RX_B3n	DIFFOUT_B3n	AE27		DQ23B	DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_TX_B3p	DIFFIN_B3p*	AH28		DQS23B	DQS12B/CQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_RX_B3p	DIFFOUT_B3p	AE26									
3B	BIO1	VREFB3BN0	IO			DIFFIO_TX_B4n	DIFFIN_B4n*	AF24		DQ23B	DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	AG28		DQ23B	DQ12B	DQ6B					
3B	BIO1	VREFB3BN0	IO			DIFFIO_TX_B4p	DIFFIN_B4p*	AE24									
3B	BIO1	VREFB3BN0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	AF28		DQ23B	DQ12B	DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_TX_B5n	DIFFIN_B5n*	AJ29		DQ22B	DQ11B	DQ6B					

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
3B	BIO2	VREFB3BN0	IO			DIFFIO_RX_B5n	DIFFOUT_B5n	AJ27		DQ22B	DQ11B	DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_TX_B5p	DIFFIN_B5p*	AJ28		DQ22B	DQ11B	DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_RX_B5p	DIFFOUT_B5p	AH27									
3B	BIO2	VREFB3BN0	IO			DIFFIO_TX_B6n	DIFFIN_B6n*	AF23		DQSn22B	DQ11B	DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	AL28		DQ22B	DQ11B	DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_TX_B6p	DIFFIN_B6p*	AE23		DQS22B	DQ11B/CQn11B	DQ6B/CQn6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	AK28									
3B	BIO2	VREFB3BN0	IO			DIFFIO_TX_B7n	DIFFIN_B7n*	AK30		DQSn21B	DQSn11B/DQ11B	DQSn6B/DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_RX_B7n	DIFFOUT_B7n	AK27		DQ21B	DQ11B	DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_TX_B7p	DIFFIN_B7p*	AJ30		DQS21B	DQS11B/CQ11B	DQS6B/CQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_RX_B7p	DIFFOUT_B7p	AJ26									
3B	BIO2	VREFB3BN0	IO			DIFFIO_TX_B8n	DIFFIN_B8n*	AE21		DQ21B	DQ11B	DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	AH30		DQ21B	DQ11B	DQ6B					
3B	BIO2	VREFB3BN0	IO			DIFFIO_TX_B8p	DIFFIN_B8p*	AD21									
3B	BIO2	VREFB3BN0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	AG30		DQ21B	DQ11B	DQ6B					
3A		VREFB3AN0	IO	PLL4_CLKOUT1n				AH25	U24								
3A		VREFB3AN0	IO	RDN0				AL27	AB19								
3A		VREFB3AN0	IO	PLL4_CLKOUT1p				AH24	V24								
3A		VREFB3AN0	IO	RUP0				AL26	AC19								
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B9n	DIFFIN_B9n*	AM29		DQ20B	DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B9n	AM28		DQ20B	DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B9p	DIFFIN_B9p*	AL29		DQ20B	DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B9p	AM27									
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFIN_B10n*	AJ25		DQSn20B	DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AN28		DQ20B	DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFIN_B10p*	AJ24		DQS20B	DQ10B/CQn10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	AN27									
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B11n	DIFFIN_B11n*	AM26		DQSn19B	DQSn10B/DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AK22		DQ19B	DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B11p	DIFFIN_B11p*	AM25		DQS19B	DQS10B/CQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AJ22									
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFIN_B12n*	AG21		DQ19B	DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B12n	DIFFOUT_B12n	AP29		DQ19B	DQ10B	DQ5B	DQ2B				
3A	BIO3	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFIN_B12p*	AF20									
3A	BIO3	VREFB3AN0	IO			DIFFIO_RX_B12p	DIFFOUT_B12p	AP28		DQ19B	DQ10B	DQ5B	DQ2B				
3A	BIO4	VREFB3AN0	IO			DIFFIO_TX_B13n	DIFFIN_B13n*	AM24	AD21	DQ18B	DQ9B	DQ5B	DQ2B	DQ14B	DQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AM23	AC17	DQ18B	DQ9B	DQ5B	DQ2B	DQ14B	DQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_TX_B13p	DIFFIN_B13p*	AL24	AC21	DQ18B	DQ9B	DQ5B	DQ2B	DQ14B	DQ7B		
3A	BIO4	VREFB3AN0	IO		INIT_DONE	DIFFIO_RX_B13p	DIFFOUT_B13p	AL23	AB17								
3A	BIO4	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFIN_B14n*	AH21	Y22	DQSn18B	DQ9B	DQ5B	DQ2B	DQSn14B	DQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AP27	AC16	DQ18B	DQ9B	DQ5B	DQ2B	DQ14B	DQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFIN_B14p*	AG22	W21	DQS18B	DQ9B/CQn9B	DQ5B/CQn5B	DQ2B	DQS14B	DQ7B/CQn7B		
3A	BIO4	VREFB3AN0	IO		nCEO	DIFFIO_RX_B14p	DIFFOUT_B14p	AP26	AB16								
3A	BIO4	VREFB3AN0	IO			DIFFIO_TX_B15n	DIFFIN_B15n*	AP24	AD23	DQSn17B	DQSn9B/DQ9B	DQSn5B/DQ5B	DQ2B	DQSn13B	DQSn7B/DQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AP25	AD18	DQ17B	DQ9B	DQ5B	DQ2B	DQ13B	DQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_TX_B15p	DIFFIN_B15p*	AN24	AD22	DQS17B	DQS9B/CQ9B	DQS5B/CQ5B	DQ2B	DQS13B	DQS7B/CQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AN25	AC18								
3A	BIO4	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFIN_B16n*	AE19	Y20	DQ17B	DQ9B	DQ5B	DQ2B	DQ13B	DQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_RX_B16n	DIFFOUT_B16n	AJ23	AC23	DQ17B	DQ9B	DQ5B	DQ2B	DQ13B	DQ7B		
3A	BIO4	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFIN_B16p*	AD19	Y19								
3A	BIO4	VREFB3AN0	IO			DIFFIO_RX_B16p	DIFFOUT_B16p	AH23	AC22	DQ17B	DQ9B	DQ5B	DQ2B	DQ13B	DQ7B		
3A	BIO5	VREFB3AN0	IO			DIFFIO_TX_B17n	DIFFIN_B17n*	AL25	AD24	DQ16B	DQ8B	DQ4B	DQ2B	DQ12B	DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AM22	AE22	DQ16B	DQ8B	DQ4B	DQ2B	DQ12B	DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_TX_B17p	DIFFIN_B17p*	AK25	AC24	DQ16B	DQ8B	DQ4B	DQ2B	DQ12B	DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AL22	AE21								
3A	BIO5	VREFB3AN0	IO			DIFFIO_TX_B18n	DIFFIN_B18n*	AJ21	V23	DQSn16B	DQ8B	DQ4B	DQ2B	DQSn12B	DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AL21	AF20	DQ16B	DQ8B	DQ4B	DQ2B	DQ12B	DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_TX_B18p	DIFFIN_B18p*	AH20	V22	DQS16B	DQ8B/CQn8B	DQ4B	DQ2B/CQn2B	DQS12B	DQ6B/CQn6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AK21	AE20								
3A	BIO5	VREFB3AN0	IO			DIFFIO_TX_B19n	DIFFIN_B19n*	AP22	AF18	DQSn15B	DQSn8B/DQ8B	DQ4B	DQSn2B/DQ2B	DQSn11B	DQSn6B/DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AP23	AF19	DQ15B	DQ8B	DQ4B	DQ2B	DQ11B	DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_TX_B19p	DIFFIN_B19p*	AP21	AE18	DQS15B	DQS8B/CQ8B	DQ4B	DQS2B/CQ2B	DQS11B	DQS6B/CQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AN22	AE19								
3A	BIO5	VREFB3AN0	IO			DIFFIO_TX_B20n	DIFFIN_B20n*	AG19	AA16	DQ15B	DQ8B	DQ4B	DQ2B	DQ11B	DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_RX_B20n	DIFFOUT_B20n	AL20	AF17	DQ15B	DQ8B	DQ4B	DQ2B	DQ11B	DQ6B	DQ3B	
3A	BIO5	VREFB3AN0	IO			DIFFIO_TX_B20p	DIFFIN_B20p*	AF19	Y16								
3A	BIO5	VREFB3AN0	IO			DIFFIO_RX_B20p	DIFFOUT_B20p	AL19	AE17	DQ15B	DQ8B	DQ4B	DQ2B	DQ11B	DQ6B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_TX_B21n	DIFFIN_B21n*	AN21	AD15	DQ14B	DQ7B	DQ4B	DQ2B	DQ10B	DQ5B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AP20	AF16	DQ14B	DQ7B	DQ4B	DQ2B	DQ10B	DQ5B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_TX_B21p	DIFFIN_B21p*	AM21	AC15	DQ14B	DQ7B	DQ4B	DQ2B	DQ10B	DQ5B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AP19	AE16								
3A	BIO6	VREFB3AN0	IO			DIFFIO_TX_B22n	DIFFIN_B22n*	AF18	AA19	DQSn14B	DQ7B	DQ4B	DQ2B	DQSn10B	DQ5B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	AN19	AH19	DQ14B	DQ7B	DQ4B	DQ2B	DQ10B	DQ5B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_TX_B22p	DIFFIN_B22p*	AE18	Y18	DQS14B	DQ7B/CQn7B	DQ4B/CQn4B	DQ2B	DQS10B	DQ5B/CQn5B	DQ3B/CQn3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	AM19	AG19								
3A	BIO6	VREFB3AN0	IO			DIFFIO_TX_B23n	DIFFIN_B23n*	AM18	AH17	DQSn13B	DQSn7B/DQ7B	DQSn4B/DQ4B	DQ2B	DQSn9B	DQSn5B/DQ5B	DQSn3B/DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AP18	AH18	DQ13B	DQ7B	DQ4B	DQ2B	DQ9B	DQ5B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_TX_B23p	DIFFIN_B23p*	AL18	AH16	DQS13B	DQS7B/CQ7B	DQS4B/CQ4B	DQ2B	DQS9B	DQS5B/CQ5B	DQS3B/CQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AN18	AG18								
3A	BIO6	VREFB3AN0	IO			DIFFIO_TX_B24n	DIFFIN_B24n*	AH19	AB15	DQ13B	DQ7B	DQ4B	DQ2B	DQ9B	DQ5B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B24n	AK18	AH15	DQ13B	DQ7B	DQ4B	DQ2B	DQ9B	DQ5B	DQ3B	
3A	BIO6	VREFB3AN0	IO			DIFFIO_TX_B24p	DIFFIN_B24p*	AG18	AA15								
3A	BIO6	VREFB3AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B24p	AJ18	AG15	DQ13B	DQ7B	DQ4B	DQ2B	DQ9B	DQ5B	DQ3B	
3A		VREFB3AN0	CLK4	DIFFCLK_0n				AK19	AF15								
4A		VREFB4AN0	CLK5	DIFFCLK_1n				AP17	AF14								
3A		VREFB3AN0	CLK6	DIFFCLK_0p				AJ19	AE15								
4A		VREFB4AN0	CLK7	DIFFCLK_1p				AP16	AE14								
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B25n	DIFFIN_B25n*	AH18	AH14	DQ12B	DQ6B	DQ3B	DQ1B	DQ8B	DQ4B	DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AP15	AH12	DQ12B	DQ6B	DQ3B	DQ1B	DQ8B	DQ4B	DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFIN_B25p*	AH17	AH13	DQ12B	DQ6B	DQ3B	DQ1B	DQ8B	DQ4B	DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AN16	AG12								
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B26n	DIFFIN_B26n*	AF17	Y14	DQSn12B	DQ6B	DQ3B	DQ1B	DQSn8B	DQ4B	DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AP14	AH11	DQ12B	DQ6B	DQ3B	DQ1B	DQ8B	DQ4B	DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B26p	DIFFIN_B26p*	AE17	Y13	DQS12B	DQ6B/CQn6B	DQ3B/CQn3B	DQ1B	DQS8B	DQ4B/CQn4B	DQ2B/CQn2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AP13	AH10								
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B27n	DIFFIN_B27n*	AM17	AH8	DQSn11B	DQSn6B/DQ6B	DQSn3B/DQ3B	DQ1B	DQSn7B	DQSn4B/DQ4B	DQSn2B/DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AN15	AH9	DQ11B	DQ6B	DQ3B	DQ1B	DQ7B	DQ4B	DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B27p	DIFFIN_B27p*	AM16	AH7	DQS11B	DQS6B/CQ6B	DQS3B/CQ3B	DQ1B	DQS7B	DQS4B/CQ4B	DQS2B/CQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AM15	AG9								
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFIN_B28n*	AC18	AC14	DQ11B	DQ6B	DQ3B	DQ1B	DQ7B	DQ4B	DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B28n	DIFFOUT_B28n	AN13	AH6	DQ11B	DQ6B	DQ3B	DQ1B	DQ7B	DQ4B	DQ2B	DQ1B
4A	BIO7	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFIN_B28p*	AC17	AB14								
4A	BIO7	VREFB4AN0	IO			DIFFIO_RX_B28p	DIFFOUT_B28p	AM13	AG6	DQ11B	DQ6B	DQ3B	DQ1B	DQ7B	DQ4B	DQ2B	DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFIN_B29n*	AL16	AH5	DQ10B	DQ5B	DQ3B	DQ1B	DQ6B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AP12	AF13	DQ10B	DQ5B	DQ3B	DQ1B	DQ6B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFIN_B29p*	AK16	AH4	DQ10B	DQ5B	DQ3B	DQ1B	DQ6B	DQ3B	DQ2B	DQ1B

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
4A	BIO8	VREFB4AN0	IO			DIFFIO_RX_B29p	DIFFOUT_B29p	AP11	AE13								
4A	BIO8	VREFB4AN0	IO			DIFFIO_TX_B30n	DIFFIN_B30n*	AH16	AC13	DQSn10B	DQ5B	DQ3B	DQ1B	DQSn6B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AN12	AF12	DQ10B	DQ5B	DQ3B	DQ1B	DQ6B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_TX_B30p	DIFFIN_B30p*	AG16	AB13	DQS10B	DQS8/CQn5B	DQ3B	DQ1B/CQn1B	DQS6B	DQ3B/CQn3B	DQ2B	DQ1B/CQn1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AM12	AE12								
4A	BIO8	VREFB4AN0	IO			DIFFIO_TX_B31n	DIFFIN_B31n*	AL15	AF10	DQSn9B	DQSn5B/DQ5B	DQ3B	DQSn1B/DQ1B	DQSn5B	DQSn3B/DQ3B	DQ2B	DQSn1B/DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_RX_B31n	DIFFOUT_B31n	AP10	AF11	DQ9B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_TX_B31p	DIFFIN_B31p*	AK15	AE10	DQS9B	DQS5B/CQ5B	DQ3B	DQS1B/CQ1B	DQS5B	DQS3B/CQ3B	DQ2B	DQS1B/CQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_RX_B31p	DIFFOUT_B31p	AN10	AE11								
4A	BIO8	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFIN_B32n*	AH15	W13	DQ9B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AP9	AF9	DQ9B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	DQ2B	DQ1B
4A	BIO8	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFIN_B32p*	AG15	W12								
4A	BIO8	VREFB4AN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AP8	AE9	DQ9B	DQ5B	DQ3B	DQ1B	DQ5B	DQ3B	DQ2B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFIN_B33n*	AP7	AF8	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_RX_B33n	DIFFOUT_B33n	AL14	AF7	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFIN_B33p*	AN7	AE8	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_RX_B33p	DIFFOUT_B33p	AL13	AE7								
4A	BIO9	VREFB4AN0	IO			DIFFIO_TX_B34n	DIFFIN_B34n*	AF16	Y12	DQSn8B	DQ4B	DQ2B	DQ1B	DQSn4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AP6	AF6	DQ8B	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_TX_B34p	DIFFIN_B34p*	AE16	W11	DQS8B	DQ4B/CQn4B	DQ2B/CQn2B	DQ1B	DQS4B	DQ2B/CQn2B	DQ1B/CQn1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AN6	AE6								
4A	BIO9	VREFB4AN0	IO			DIFFIO_TX_B35n	DIFFIN_B35n*	AL12	AD12	DQSn7B	DQSn4B/DQ4B	DQSn2B/DQ2B	DQ1B	DQSn3B	DQSn2B/DQ2B	DQSn1B/DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AP5	AF5	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_TX_B35p	DIFFIN_B35p*	AK13	AC12	DQS7B	DQS4B/CQ4B	DQS2B/CQ2B	DQ1B	DQS3B	DQS2B/CQ2B	DQS1B/CQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	AP4	AE5								
4A	BIO9	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFIN_B36n*	AC15	AC11	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AL11	AC4	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO9	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFIN_B36p*	AC14	AB11								
4A	BIO9	VREFB4AN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AK12	AG3	DQ7B	DQ4B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFIN_B37n*	AP3	AH3	DQ6B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_RX_B37n	DIFFOUT_B37n	AN9	AF4	DQ6B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFIN_B37p*	AP2	AH2	DQ6B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_RX_B37p	DIFFOUT_B37p	AM9	AE4								
4A	BIO10	VREFB4AN0	IO			DIFFIO_TX_B38n	DIFFIN_B38n*	AF15	Y11	DQSn6B	DQ3B	DQ2B	DQ1B	DQSn2B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AM10	AF3	DQ6B	DQ3B	DQ2B	DQ1B	DQ2B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_TX_B38p	DIFFIN_B38p*	AE15	W10	DQS6B	DQ3B/CQn3B	DQ2B	DQ1B	DQS2B	DQ1B/CQn1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AL10	AF2								
4A	BIO10	VREFB4AN0	IO			DIFFIO_TX_B39n	DIFFIN_B39n*	AM8	AD6	DQSn5B	DQSn3B/DQ3B	DQ2B	DQ1B	DQSn1B	DQSn1B/DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_RX_B39n	DIFFOUT_B39n	AN4	AG1	DQ5B	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_TX_B39p	DIFFIN_B39p*	AM7	AC6	DQS5B	DQS3B/CQ3B	DQ2B	DQ1B	DQS1B	DQS1B/CQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_RX_B39p	DIFFOUT_B39p	AN3	AF1								
4A	BIO10	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFIN_B40n*	AJ16	AA10	DQ5B	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AJ12	AD9	DQ5B	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
4A	BIO10	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFIN_B40p*	AJ15	Y10								
4A	BIO10	VREFB4AN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AJ11	AC9	DQ5B	DQ3B	DQ2B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
4A		VREFB4AN0	IO	PLL3_CLKOUT1n				AJ13	AC10								
4A		VREFB4AN0	IO			DIFFIO_RX_B41n	DIFFOUT_B41n	AH13	AD7								
4A		VREFB4AN0	IO	PLL3_CLKOUT1p				AH14	AB10								
4A		VREFB4AN0	IO			DIFFIO_RX_B41p	DIFFOUT_B41p	AG13	AC7								
4A		VREFB4AN0	IO	PLL3_CLKOUT2n				AF14	AB9								
4A		VREFB4AN0	IO	PLL3_CLKOUT3n				AH12	AC8								
4A		VREFB4AN0	IO	PLL3_CLKOUT2p				AE14	AA9								
4A		VREFB4AN0	IO	PLL3_CLKOUT3p				AG12	AB8								
4B	BIO11	VREFB4BN0	IO			DIFFIO_TX_B41n	DIFFIN_B41n*	AK10		DQ4B	DQ2B	DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AL9		DQ4B	DQ2B	DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_TX_B41p	DIFFIN_B41p*	AJ10		DQ4B	DQ2B	DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AK9									
4B	BIO11	VREFB4BN0	IO			DIFFIO_TX_B42n	DIFFIN_B42n*	AF13		DQSn4B	DQ2B	DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AL8		DQ4B	DQ2B	DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_TX_B42p	DIFFIN_B42p*	AE13		DQS4B	DQ2B/CQn2B	DQ1B/CQn1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	AL7									
4B	BIO11	VREFB4BN0	IO			DIFFIO_TX_B43n	DIFFIN_B43n*	AL6		DQSn3B	DQSn2B/DQ2B	DQSn1B/DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AM6		DQ3B	DQ2B	DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_TX_B43p	DIFFIN_B43p*	AK6		DQS3B	DQS2B/CQ2B	DQS1B/CQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AM5									
4B	BIO11	VREFB4BN0	IO			DIFFIO_TX_B44n	DIFFIN_B44n*	AF12		DQ3B	DQ2B	DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_RX_B45n	DIFFOUT_B45n	AK7		DQ3B	DQ2B	DQ1B					
4B	BIO11	VREFB4BN0	IO			DIFFIO_TX_B44p	DIFFIN_B44p*	AE12									
4B	BIO11	VREFB4BN0	IO			DIFFIO_RX_B45p	DIFFOUT_B45p	AJ7		DQ3B	DQ2B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_TX_B45n	DIFFIN_B45n*	AM4		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AJ9		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_TX_B45p	DIFFIN_B45p*	AL5		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AH9									
4B	BIO12	VREFB4BN0	IO			DIFFIO_TX_B46n	DIFFIN_B46n*	AE11		DQSn2B	DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	AH10		DQ2B	DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_TX_B46p	DIFFIN_B46p*	AD12		DQS2B	DQ1B/CQn1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	AG9									
4B	BIO12	VREFB4BN0	IO			DIFFIO_TX_B47n	DIFFIN_B47n*	AM2		DQSn1B	DQSn1B/DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AM3		DQ1B	DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_TX_B47p	DIFFIN_B47p*	AL3		DQS1B	DQS1B/CQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AL4									
4B	BIO12	VREFB4BN0	IO			DIFFIO_TX_B48n	DIFFIN_B48n*	AG10		DQ1B	DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_RX_B49n	DIFFOUT_B49n	AN1		DQ1B	DQ1B	DQ1B					
4B	BIO12	VREFB4BN0	IO			DIFFIO_TX_B48p	DIFFIN_B48p*	AF11									
4B	BIO12	VREFB4BN0	IO			DIFFIO_RX_B49p	DIFFOUT_B49p	AM1		DQ1B	DQ1B	DQ1B					
5B	RIO1	VREFB5BN0	IO			DIFFIO_TX_R1n	DIFFIN_R1n*	AJ6		DQ24R	DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	AF7		DQ24R	DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_TX_R1p	DIFFIN_R1p*	AH7		DQ24R	DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	AF8									
5B	RIO1	VREFB5BN0	IO			DIFFIO_TX_R2n	DIFFIN_R2n*	AD9		DQSn24R	DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	AK3		DQ24R	DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_TX_R2p	DIFFIN_R2p*	AD10		DQS24R	DQ12R/CQn12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	AK4									
5B	RIO1	VREFB5BN0	IO			DIFFIO_TX_R3n	DIFFIN_R3n*	AH5		DQSn23R	DQSn12R/DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_RX_R3n	DIFFOUT_R3n	AG6		DQ23R	DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_TX_R3p	DIFFIN_R3p*	AH6		DQS23R	DQS12R/CQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_RX_R3p	DIFFOUT_R3p	AG7									
5B	RIO1	VREFB5BN0	IO			DIFFIO_TX_R4n	DIFFIN_R4n*	AE7		DQ23R	DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	AL1		DQ23R	DQ12R	DQ6R					
5B	RIO1	VREFB5BN0	IO			DIFFIO_TX_R4p	DIFFIN_R4p*	AE8									
5B	RIO1	VREFB5BN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	AL2		DQ23R	DQ12R	DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_TX_R5n	DIFFIN_R5n*	AK1		DQ22R	DQ11R	DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_RX_R5n	DIFFOUT_R5n	AJ3		DQ22R	DQ11R	DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_TX_R5p	DIFFIN_R5p*	AJ1		DQ22R	DQ11R	DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_RX_R5p	DIFFOUT_R5p	AJ4									
5B	RIO2	VREFB5BN0	IO			DIFFIO_TX_R6n	DIFFIN_R6n*	AC10		DQSn22R	DQ11R	DQ6R					

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
5B	RIO2	VREFB5BN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	AJ2		DQ22R	DQ11R	DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_TX_R6p	DIFFIN_R6p*	AC11		DQS22R	DQ11R/CQn11R	DQ6R/CQn6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	AH3									
5B	RIO2	VREFB5BN0	IO			DIFFIO_TX_R7n	DIFFIN_R7n*	AF5		DQSn21R	DQSn11R/DQ11R	DQSn6R/DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	AH4		DQ21R	DQ11R	DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_TX_R7p	DIFFIN_R7p*	AF6		DQS21R	DQS11R/CQ11R	DQS6R/CQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	AG4									
5B	RIO2	VREFB5BN0	IO			DIFFIO_TX_R8n	DIFFIN_R8n*	AC8		DQ21R	DQ11R	DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	AE5		DQ21R	DQ11R	DQ6R					
5B	RIO2	VREFB5BN0	IO			DIFFIO_TX_R8p	DIFFIN_R8p*	AC9									
5B	RIO2	VREFB5BN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	AE6		DQ21R	DQ11R	DQ6R					
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFIN_R9n*	AD6	AA6	DQ20R	DQ10R	DQ5R	DQ2R	DQ14R	DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	AC5	AD4	DQ20R	DQ10R	DQ5R	DQ2R	DQ14R	DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFIN_R9p*	AD7	AB7	DQ20R	DQ10R	DQ5R	DQ2R	DQ14R	DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	AC7	AC5								
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFIN_R10n*	AB9	W8	DQSn20R	DQ10R	DQ5R	DQ2R	DQSn14R	DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	AB7	AB5	DQ20R	DQ10R	DQ5R	DQ2R	DQ14R	DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFIN_R10p*	AB10	Y9	DQS20R	DQ10R/CQn10R	DQ5R	DQ2R	DQS14R	DQ7R/CQn7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	AB8	AB6								
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFIN_R11n*	AH1	AC4	DQSn19R	DQSn10R/DQ10R	DQ5R	DQ2R	DQSn13R	DQSn7R/DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	AF4	Y5	DQ19R	DQ10R	DQ5R	DQ2R	DQ13R	DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFIN_R11p*	AH2	AB4	DQS19R	DQS10R/CQ10R	DQ5R	DQ2R	DQS13R	DQS7R/CQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	AE4	Y6								
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFIN_R12n*	Y6	W6	DQ19R	DQ10R	DQ5R	DQ2R	DQ13R	DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R12n	AG1	AE3	DQ19R	DQ10R	DQ5R	DQ2R	DQ13R	DQ7R	DQ3R	DQ1R
5A	RIO3	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFIN_R12p*	AA7	V7								
5A	RIO3	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R12p	AF1	AD3	DQ19R	DQ10R	DQ5R	DQ2R	DQ13R	DQ7R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R13n	DIFFIN_R13n*	AF2	AC2	DQ18R	DQ9R	DQ5R	DQ2R	DQ12R	DQ6R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	AE1	AA3	DQ18R	DQ9R	DQ5R	DQ2R	DQ12R	DQ6R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R13p	DIFFIN_R13p*	AF3	AC3	DQ18R	DQ9R	DQ5R	DQ2R	DQ12R	DQ6R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	AE2	AA4								
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R14n	DIFFIN_R14n*	AA9	V6	DQSn18R	DQ9R	DQ5R	DQ2R	DQSn12R	DQ6R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R14n	DIFFOUT_R14n	AB5	W4	DQ18R	DQ9R	DQ5R	DQ2R	DQ12R	DQ6R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R14p	DIFFIN_R14p*	AA10	U6	DQS18R	DQ9R/CQn9R	DQ5R/CQn5R	DQ2R	DQS12R	DQ6R/CQn6R	DQ3R/CQn3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R14p	DIFFOUT_R14p	AB6	W5								
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R15n	DIFFIN_R15n*	AE3	AB2	DQSn17R	DQSn9R/DQ9R	DQSn5R/DQ5R	DQ2R	DQSn11R	DQSn6R/DQ6R	DQSn3R/DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	AC4	Y3	DQ17R	DQ9R	DQ5R	DQ2R	DQ11R	DQ6R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R15p	DIFFIN_R15p*	AD4	AB3	DQS17R	DQS9R/CQ9R	DQS5R/CQ5R	DQ2R	DQS11R	DQS6R/CQ6R	DQS3R/CQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	AC5	Y4								
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R16n	DIFFIN_R16n*	Y7	T6	DQ17R	DQ9R	DQ5R	DQ2R	DQ11R	DQ6R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R16n	DIFFOUT_R16n	AD1	AE1	DQ17R	DQ9R	DQ5R	DQ2R	DQ11R	DQ6R	DQ3R	DQ1R
5A	RIO4	VREFB5AN0	IO			DIFFIO_TX_R16p	DIFFIN_R16p*	Y8	T7								
5A	RIO4	VREFB5AN0	IO			DIFFIO_RX_R16p	DIFFOUT_R16p	AC1	AD1	DQ17R	DQ9R	DQ5R	DQ2R	DQ11R	DQ6R	DQ3R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_TX_R17n	DIFFIN_R17n*	AC2	AC1	DQ16R	DQ8R	DQ4R	DQ2R	DQ10R	DQ5R	DQ2R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	AB3	AA1	DQ16R	DQ8R	DQ4R	DQ2R	DQ10R	DQ5R	DQ2R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_TX_R17p	DIFFIN_R17p*	AC3	AB1	DQ16R	DQ8R	DQ4R	DQ2R	DQ10R	DQ5R	DQ2R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	AB4	Y1								
5A	RIO5	VREFB5AN0	IO			DIFFIO_TX_R18n	DIFFIN_R18n*	Y10	N4	DQSn16R	DQ8R	DQ4R	DQ2R	DQSn10R	DQ5R	DQ2R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	AB1	V3	DQ16R	DQ8R	DQ4R	DQ2R	DQ10R	DQ5R	DQ2R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_TX_R18p	DIFFIN_R18p*	Y11	P5	DQS16R	DQ8R/CQn8R	DQ4R	DQ2R/CQn2R	DQS10R	DQ5R/CQn5R	DQ2R	DQ1R/CQn1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	AB2	V4								
5A	RIO5	VREFB5AN0	IO			DIFFIO_TX_R19n	DIFFIN_R19n*	AA4	W1	DQSn15R	DQSn8R/DQ8R	DQ4R	DQSn2R/DQ2R	DQSn9R	DQSn5R/DQ5R	DQ2R	DQSn1R/DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	AA1	W2	DQ15R	DQ8R	DQ4R	DQ2R	DQ9R	DQ5R	DQ2R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_TX_R19p	DIFFIN_R19p*	Y5	V1	DQS15R	DQS8R/CQ8R	DQ4R	DQS2R/CQ2R	DQS9R	DQS5R/CQ5R	DQ2R	DQS1R/CQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	Y1	W3								
5A	RIO5	VREFB5AN0	IO			DIFFIO_TX_R20n	DIFFIN_R20n*	Y9	R6	DQ15R	DQ8R	DQ4R	DQ2R	DQ9R	DQ5R	DQ2R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_RX_R20n	DIFFOUT_R20n	Y3	U4	DQ15R	DQ8R	DQ4R	DQ2R	DQ9R	DQ5R	DQ2R	DQ1R
5A	RIO5	VREFB5AN0	IO			DIFFIO_TX_R20p	DIFFIN_R20p*	W10	P6								
5A	RIO5	VREFB5AN0	IO			DIFFIO_RX_R20p	DIFFOUT_R20p	Y4	U5	DQ15R	DQ8R	DQ4R	DQ2R	DQ9R	DQ5R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_TX_R21n	DIFFIN_R21n*	W6	U3	DQ14R	DQ7R	DQ4R	DQ2R	DQ8R	DQ4R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	W1	T3	DQ14R	DQ7R	DQ4R	DQ2R	DQ8R	DQ4R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_TX_R21p	DIFFIN_R21p*	W7	T4	DQ14R	DQ7R	DQ4R	DQ2R	DQ8R	DQ4R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	Y2	R3								
5A	RIO6	VREFB5AN0	IO			DIFFIO_TX_R22n	DIFFIN_R22n*	V10	N6	DQSn14R	DQ7R	DQ4R	DQ2R	DQSn8R	DQ4R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_RX_R22n	DIFFOUT_R22n	W3	U1	DQ14R	DQ7R	DQ4R	DQ2R	DQ8R	DQ4R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_TX_R22p	DIFFIN_R22p*	V11	M6	DQS14R	DQ7R/CQn7R	DQ4R/CQn4R	DQ2R	DQS8R	DQ4R/CQn4R	DQ2R/CQn2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_RX_R22p	DIFFOUT_R22p	W4	T1								
5A	RIO6	VREFB5AN0	IO			DIFFIO_TX_R23n	DIFFIN_R23n*	V3	R1	DQSn13R	DQSn7R/DQ7R	DQSn4R/DQ4R	DQ2R	DQSn7R	DQSn4R/DQ4R	DQSn2R/DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	V1	R4	DQ13R	DQ7R	DQ4R	DQ2R	DQ7R	DQ4R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_TX_R23p	DIFFIN_R23p*	V4	P1	DQS13R	DQS7R/CQ7R	DQS4R/CQ4R	DQ2R	DQS7R	DQS4R/CQ4R	DQS2R/CQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	V2	R5								
5A	RIO6	VREFB5AN0	IO			DIFFIO_TX_R24n	DIFFIN_R24n*	W12	M5	DQ13R	DQ7R	DQ4R	DQ2R	DQ7R	DQ4R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_RX_R24n	DIFFOUT_R24n	V7	P3	DQ13R	DQ7R	DQ4R	DQ2R	DQ7R	DQ4R	DQ2R	DQ1R
5A	RIO6	VREFB5AN0	IO			DIFFIO_TX_R24p	DIFFIN_R24p*	V12	L6								
5A	RIO6	VREFB5AN0	IO			DIFFIO_RX_R24p	DIFFOUT_R24p	U7	P4	DQ13R	DQ7R	DQ4R	DQ2R	DQ7R	DQ4R	DQ2R	DQ1R
5A		VREFB5AN0	CLK8	DIFFCLK_2n				V5	P2								
5A		VREFB5AN0	CLK10	DIFFCLK_2p				V6	N3								
6A		VREFB6AN0	CLK9	DIFFCLK_3n				U5	N1								
6A		VREFB6AN0	CLK11	DIFFCLK_3p				U6	M1								
6A	RIO7	VREFB6AN0	IO			DIFFIO_TX_R25n	DIFFIN_R25n*	T7	L1	DQ12R	DQ6R	DQ3R	DQ1R	DQ6R	DQ3R	DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_RX_R25n	DIFFOUT_R25n	U1	M2	DQ12R	DQ6R	DQ3R	DQ1R	DQ6R	DQ3R	DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_TX_R25p	DIFFIN_R25p*	R7	K1	DQ12R	DQ6R	DQ3R	DQ1R	DQ6R	DQ3R	DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_RX_R25p	DIFFOUT_R25p	U2	L3								
6A	RIO7	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFIN_R26n*	U10	K6	DQSn12R	DQ6R	DQ3R	DQ1R	DQSn6R	DQ3R	DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_RX_R26n	DIFFOUT_R26n	T1	M3	DQ12R	DQ6R	DQ3R	DQ1R	DQ6R	DQ3R	DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFIN_R26p*	U11	L7	DQS12R	DQ6R/CQn6R	DQ3R/CQn3R	DQ1R	DQS6R	DQ3R/CQn3R	DQ1R/CQn1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_RX_R26p	DIFFOUT_R26p	R1	M4								
6A	RIO7	VREFB6AN0	IO			DIFFIO_TX_R27n	DIFFIN_R27n*	P1	J2	DQSn11R	DQSn6R/DQ6R	DQSn3R/DQ3R	DQ1R	DQSn5R	DQSn3R/DQ3R	DQSn1R/DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	U3	J1	DQ11R	DQ6R	DQ3R	DQ1R	DQ5R	DQ3R	DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_TX_R27p	DIFFIN_R27p*	R2	J3	DQS11R	DQS6R/CQ6R	DQS3R/CQ3R	DQ1R	DQS5R	DQS3R/CQ3R	DQS1R/CQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	U4	H1								
6A	RIO7	VREFB6AN0	IO			DIFFIO_TX_R28n	DIFFIN_R28n*	V9	J6	DQ11R	DQ6R	DQ3R	DQ1R	DQ5R	DQ3R	DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	N1	K3	DQ11R	DQ6R	DQ3R	DQ1R	DQ5R	DQ3R	DQ1R	
6A	RIO7	VREFB6AN0	IO			DIFFIO_TX_R28p	DIFFIN_R28p*	U9	J7								
6A	RIO7	VREFB6AN0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	N2	L4	DQ11R	DQ6R	DQ3R	DQ1R	DQ5R	DQ3R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R29n	DIFFIN_R29n*	T4	G1	DQ10R	DQ5R	DQ3R	DQ1R	DQ4R	DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	R5	E1	DQ10R	DQ5R	DQ3R	DQ1R	DQ4R	DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R29p	DIFFIN_R29p*	R4	F1	DQ10R	DQ5R	DQ3R	DQ1R	DQ4R	DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	R6	F2								
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R30n	DIFFIN_R30n*	R10	K7	DQSn10R	DQ5R	DQ3R	DQ1R	DQSn4R	DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R30n	DIFFOUT_R30n	M1	D1	DQ10R	DQ5R	DQ3R	DQ1R	DQ4R	DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R30p	DIFFIN_R30p*	R11	J8	DQS10R	DQ5R/CQn5R	DQ3R	DQ1R/CQn1R	DQS4R	DQ2R/CQn2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R30p	DIFFOUT_R30p	M2	C1								
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R31n	DIFFIN_R31n*	L1	J4	DQSn9R	DQSn5R/DQ5R	DQ3R	DQSn1R/DQ1R	DQSn3R	DQSn2R/DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	R3	H3	DQ9R	DQ5R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R31p	DIFFIN_R31p*	K1	J5	DQS9R	DQS5R/CQ5R	DQ3R	DQS1R/CQ1R	DQS3R	DQS2R/CQ2R	DQ1R	

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	P4	H4								
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R32n	DIFFIN_R32n*	R9	K8	DQ9R	DQ5R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R32n	DIFFOUT_R32n	J1	K4	DQ9R	DQ5R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R	
6A	RIO8	VREFB6AN0	IO			DIFFIO_TX_R32p	DIFFIN_R32p*	T10	K9								
6A	RIO8	VREFB6AN0	IO			DIFFIO_RX_R32p	DIFFOUT_R32p	J2	K5	DQ9R	DQ5R	DQ3R	DQ1R	DQ3R	DQ2R	DQ1R	
6A	RIO9	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFIN_R33n*	H1		DQ8R	DQ4R	DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	F1		DQ8R	DQ4R	DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFIN_R33p*	G1		DQ8R	DQ4R	DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	E1									
6A	RIO9	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFIN_R34n*	P7		DQSn8R	DQ4R	DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R34n	D1		DQ8R	DQ4R	DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFIN_R34p*	R8		DQS8R	DQ4R/CQn4R	DQ2R/CQn2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R34p	D2									
6A	RIO9	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFIN_R35n*	N3		DQSn7R	DQSn4R/DQ4R	DQSn2R/DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	N4		DQ7R	DQ4R	DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFIN_R35p*	M3		DQS7R	DQS4R/CQ4R	DQS2R/CQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	N5									
6A	RIO9	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFIN_R36n*	P9		DQ7R	DQ4R	DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R36n	C1		DQ7R	DQ4R	DQ2R	DQ1R				
6A	RIO9	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFIN_R36p*	P10									
6A	RIO9	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R36p	C2		DQ7R	DQ4R	DQ2R	DQ1R				
6A	RIO10	VREFB6AN0	IO		DATA7	DIFFIO_TX_R37n	DIFFIN_R37n*	K2	B1	DQ6R	DQ3R	DQ2R	DQ1R	DQ2R	DQ1R		
6A	RIO10	VREFB6AN0	IO		DATA6	DIFFIO_RX_R37n	DIFFOUT_R37n	M4	C2	DQ6R	DQ3R	DQ2R	DQ1R	DQ2R	DQ1R		
6A	RIO10	VREFB6AN0	IO		DATA5	DIFFIO_TX_R37p	DIFFIN_R37p*	K3	A2	DQ6R	DQ3R	DQ2R	DQ1R	DQ2R	DQ1R		
6A	RIO10	VREFB6AN0	IO		DATA4	DIFFIO_RX_R37p	DIFFOUT_R37p	L4	C3								
6A	RIO10	VREFB6AN0	IO		DATA3	DIFFIO_TX_R38n	DIFFIN_R38n*	P6	H6	DQSn6R	DQ3R	DQ2R	DQ1R	DQSn2R	DQ1R		
6A	RIO10	VREFB6AN0	IO		DATA2	DIFFIO_RX_R38n	DIFFOUT_R38n	G2	G3	DQ6R	DQ3R	DQ2R	DQ1R	DQ2R	DQ1R		
6A	RIO10	VREFB6AN0	IO		DATA1	DIFFIO_TX_R38p	DIFFIN_R38p*	N6	H7	DQS6R	DQ3R/CQn3R	DQ2R	DQ1R	DQS2R	DQ1R/CQn1R		
6A	RIO10	VREFB6AN0	IO		CLKUSR	DIFFIO_RX_R38p	DIFFOUT_R38p	F2	G4								
6A	RIO10	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFIN_R39n*	J4	E3	DQSn5R	DQSn3R/DQ3R	DQ2R	DQ1R	DQSn1R	DQSn1R/DQ1R		
6A	RIO10	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	J3	F3	DQ5R	DQ3R	DQ2R	DQ1R	DQ1R	DQ1R		
6A	RIO10	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFIN_R39p*	J5	D3	DQS5R	DQS3R/CQ3R	DQ2R	DQ1R	DQS1R	DQS1R/CQ1R		
6A	RIO10	VREFB6AN0	IO		DEV_OE	DIFFIO_RX_R39p	DIFFOUT_R39p	H3	F4								
6A	RIO10	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFIN_R40n*	N9	G5	DQ5R	DQ3R	DQ2R	DQ1R	DQ1R	DQ1R		
6A	RIO10	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R40n	K4	E4	DQ5R	DQ3R	DQ2R	DQ1R	DQ1R	DQ1R		
6A	RIO10	VREFB6AN0	IO		DEV_CLRn	DIFFIO_TX_R40p	DIFFIN_R40p*	N10	G6								
6A	RIO10	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R40p	K5	F5	DQ5R	DQ3R	DQ2R	DQ1R	DQ1R	DQ1R		
6B	RIO11	VREFB6BN0	IO			DIFFIO_TX_R41n	DIFFIN_R41n*	M5		DQ4R	DQ2R	DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_RX_R41n	DIFFOUT_R41n	G3		DQ4R	DQ2R	DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_TX_R41p	DIFFIN_R41p*	M6		DQ4R	DQ2R	DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_RX_R41p	DIFFOUT_R41p	H4									
6B	RIO11	VREFB6BN0	IO			DIFFIO_TX_R42n	DIFFIN_R42n*	N7		DQSn4R	DQ2R	DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_RX_R42n	DIFFOUT_R42n	F3		DQ4R	DQ2R	DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_TX_R42p	DIFFIN_R42p*	N8		DQS4R	DQ2R/CQn2R	DQ1R/CQn1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_RX_R42p	DIFFOUT_R42p	F4									
6B	RIO11	VREFB6BN0	IO			DIFFIO_TX_R43n	DIFFIN_R43n*	D3		DQSn3R	DQSn2R/DQ2R	DQSn1R/DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	E3		DQ3R	DQ2R	DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_TX_R43p	DIFFIN_R43p*	D4		DQS3R	DQS2R/CQ2R	DQS1R/CQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	E4									
6B	RIO11	VREFB6BN0	IO			DIFFIO_TX_R44n	DIFFIN_R44n*	M9		DQ3R	DQ2R	DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_RX_R44n	DIFFOUT_R44n	K6		DQ3R	DQ2R	DQ1R					
6B	RIO11	VREFB6BN0	IO			DIFFIO_TX_R44p	DIFFIN_R44p*	M10									
6B	RIO11	VREFB6BN0	IO			DIFFIO_RX_R44p	DIFFOUT_R44p	K7		DQ3R	DQ2R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_TX_R45n	DIFFIN_R45n*	J6		DQ2R	DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	G4		DQ2R	DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_TX_R45p	DIFFIN_R45p*	J7		DQ2R	DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	G5									
6B	RIO12	VREFB6BN0	IO			DIFFIO_TX_R46n	DIFFIN_R46n*	M7		DQSn2R	DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_RX_R46n	DIFFOUT_R46n	C5		DQ2R	DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_TX_R46p	DIFFIN_R46p*	M8		DQS2R	DQ1R/CQn1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_RX_R46p	DIFFOUT_R46p	D5									
6B	RIO12	VREFB6BN0	IO			DIFFIO_TX_R47n	DIFFIN_R47n*	F5		DQSn1R	DQSn1R/DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	C6		DQ1R	DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_TX_R47p	DIFFIN_R47p*	G6		DQS1R	DQS1R/CQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	D6									
6B	RIO12	VREFB6BN0	IO			DIFFIO_TX_R48n	DIFFIN_R48n*	L7		DQ1R	DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_RX_R48n	DIFFOUT_R48n	H7		DQ1R	DQ1R	DQ1R					
6B	RIO12	VREFB6BN0	IO			DIFFIO_TX_R48p	DIFFIN_R48p*	K8									
6B	RIO12	VREFB6BN0	IO			DIFFIO_RX_R48p	DIFFOUT_R48p	J8		DQ1R	DQ1R	DQ1R					
7B	TIO12	VREFB7BN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	F6		DQ24T	DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_TX_T1p	DIFFIN_T1p*	L11									
7B	TIO12	VREFB7BN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	E6		DQ24T	DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_TX_T1n	DIFFIN_T1n*	K11		DQ24T	DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_RX_T2p	DIFFOUT_T2p	G7									
7B	TIO12	VREFB7BN0	IO			DIFFIO_TX_T2p	DIFFIN_T2p*	H9		DQS24T	DQS12T/CQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	F7		DQ24T	DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_TX_T2n	DIFFIN_T2n*	G9		DQSn24T	DQSn12T/DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	E7									
7B	TIO12	VREFB7BN0	IO			DIFFIO_TX_T3p	DIFFIN_T3p*	L10		DQS23T	DQ12T/CQn12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	D7		DQ23T	DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_TX_T3n	DIFFIN_T3n*	L9		DQSn23T	DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_RX_T4p	DIFFOUT_T4p	H10									
7B	TIO12	VREFB7BN0	IO			DIFFIO_TX_T4p	DIFFIN_T4p*	F9		DQ23T	DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	G10		DQ23T	DQ12T	DQ6T					
7B	TIO12	VREFB7BN0	IO			DIFFIO_TX_T4n	DIFFIN_T4n*	F8		DQ23T	DQ12T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	C8		DQ22T	DQ11T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_TX_T5p	DIFFIN_T5p*	K12									
7B	TIO11	VREFB7BN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	C7		DQ22T	DQ11T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_TX_T5n	DIFFIN_T5n*	J11		DQ22T	DQ11T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_RX_T6p	DIFFOUT_T6p	F10									
7B	TIO11	VREFB7BN0	IO			DIFFIO_TX_T6p	DIFFIN_T6p*	J12		DQS22T	DQS11T/CQ11T	DQS6T/CQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_RX_T6n	DIFFOUT_T6n	E9		DQ22T	DQ11T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_TX_T6n	DIFFIN_T6n*	H12		DQSn22T	DQSn11T/DQ11T	DQSn6T/DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	E10									
7B	TIO11	VREFB7BN0	IO			DIFFIO_TX_T7p	DIFFIN_T7p*	M13		DQS21T	DQ11T/CQn11T	DQ6T/CQn6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	D9		DQ21T	DQ11T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_TX_T7n	DIFFIN_T7n*	L13		DQSn21T	DQ11T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	D10									
7B	TIO11	VREFB7BN0	IO			DIFFIO_TX_T8p	DIFFIN_T8p*	J13		DQ21T	DQ11T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	C10		DQ21T	DQ11T	DQ6T					
7B	TIO11	VREFB7BN0	IO			DIFFIO_TX_T8n	DIFFIN_T8n*	H13		DQ21T	DQ11T	DQ6T					
7A		VREFB7AN0	IO	RUP1				G12	F7								
7A		VREFB7AN0	IO	PLL2_CLKOUT1p				K14	K10								
7A		VREFB7AN0	IO	RDN1				G11	G7								
7A		VREFB7AN0	IO	PLL2_CLKOUT1n				J14	J9								
7A	TIO10	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	G13	F9	DQ20T	DQ10T	DQ5T	DQ2T	DQ14T	DQ7T	DQ3T	DQ1T

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
7A	TIO10	VREFB7AN0	IO			DIFFIO_TX_T9p	DIFFIN_T9p*	H15	H10								
7A	TIO10	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	F13	F8	DQ20T	DQ10T	DQ5T	DQ2T	DQ14T	DQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_TX_T9n	DIFFIN_T9n*	G15	G10	DQ20T	DQ10T	DQ5T	DQ2T	DQ14T	DQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	B1	F10								
7A	TIO10	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFIN_T10p*	F12	E6	DQS20T	DQS10T/CQ10T	DQ5T	DQ2T	DQS14T	DQS7T/CQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	A2	E10	DQ20T	DQ10T	DQ5T	DQ2T	DQ14T	DQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFIN_T10n*	E12	D5	DQSn20T	DQSn10T/DQ10T	DQ5T	DQ2T	DQSn14T	DQSn7T/DQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	C3	D4								
7A	TIO10	VREFB7AN0	IO			DIFFIO_TX_T11p	DIFFIN_T11p*	K15	K11	DQS19T	DQ10T/CQn10T	DQ5T	DQ2T	DQS13T	DQ7T/CQn7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	B4	C4	DQ19T	DQ10T	DQ5T	DQ2T	DQ13T	DQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_TX_T11n	DIFFIN_T11n*	J15	J10	DQSn19T	DQ10T	DQ5T	DQ2T	DQSn13T	DQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_RX_T12p	DIFFOUT_T12p	E13	B3								
7A	TIO10	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFIN_T12p*	D12	A5	DQ19T	DQ10T	DQ5T	DQ2T	DQ13T	DQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_RX_T12n	DIFFOUT_T12n	D13	A3	DQ19T	DQ10T	DQ5T	DQ2T	DQ13T	DQ7T	DQ3T	DQ1T
7A	TIO10	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFIN_T12n*	D11	A4	DQ19T	DQ10T	DQ5T	DQ2T	DQ13T	DQ7T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	B3	E7	DQ18T	DQ9T	DQ5T	DQ2T	DQ12T	DQ6T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_TX_T13p	DIFFIN_T13p*	K16	G11								
7A	TIO9	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	A3	D7	DQ18T	DQ9T	DQ5T	DQ2T	DQ12T	DQ6T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_TX_T13n	DIFFIN_T13n*	J16	F11	DQ18T	DQ9T	DQ5T	DQ2T	DQ12T	DQ6T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	A5	D6								
7A	TIO9	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFIN_T14p*	G14	E9	DQS18T	DQS9T/CQ9T	DQS5T/CQ5T	DQ2T	DQS12T	DQS6T/CQ6T	DQS3T/CQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	A4	C5	DQ18T	DQ9T	DQ5T	DQ2T	DQ12T	DQ6T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFIN_T14n*	F15	D9	DQSn18T	DQSn9T/DQ9T	DQSn5T/DQ5T	DQ2T	DQSn12T	DQSn6T/DQ6T	DQSn3T/DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	C9	C7								
7A	TIO9	VREFB7AN0	IO			DIFFIO_TX_T15p	DIFFIN_T15p*	L16	J12	DQS17T	DQ9T/CQn9T	DQ5T/CQn5T	DQ2T	DQS11T	DQ6T/CQn6T	DQ3T/CQn3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	B9	C6	DQ17T	DQ9T	DQ5T	DQ2T	DQ11T	DQ6T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_TX_T15n	DIFFIN_T15n*	K17	J11	DQSn17T	DQ9T	DQ5T	DQ2T	DQSn11T	DQ6T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	B6	D8								
7A	TIO9	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFIN_T16p*	B7	D10	DQ17T	DQ9T	DQ5T	DQ2T	DQ11T	DQ6T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	A6	C8	DQ17T	DQ9T	DQ5T	DQ2T	DQ11T	DQ6T	DQ3T	DQ1T
7A	TIO9	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFIN_T16n*	A7	C10	DQ17T	DQ9T	DQ5T	DQ2T	DQ11T	DQ6T	DQ3T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	D14	E12	DQ16T	DQ8T	DQ4T	DQ2T	DQ10T	DQ5T	DQ2T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_TX_T17p	DIFFIN_T17p*	J17	G12								
7A	TIO8	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	C15	D12	DQ16T	DQ8T	DQ4T	DQ2T	DQ10T	DQ5T	DQ2T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_TX_T17n	DIFFIN_T17n*	H16	F12	DQ16T	DQ8T	DQ4T	DQ2T	DQ10T	DQ5T	DQ2T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_RX_T18p	DIFFOUT_T18p	A9	C9								
7A	TIO8	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFIN_T18p*	E15	D11	DQS16T	DQS8T/CQ8T	DQ4T	DQS2T/CQ2T	DQS10T	DQS5T/CQ5T	DQ2T	DQS1T/CQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	A8	B9	DQ16T	DQ8T	DQ4T	DQ2T	DQ10T	DQ5T	DQ2T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFIN_T18n*	D15	C11	DQSn16T	DQSn8T/DQ8T	DQ4T	DQSn2T/DQ2T	DQSn10T	DQSn5T/DQ5T	DQ2T	DQSn1T/DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	C13	G13								
7A	TIO8	VREFB7AN0	IO			DIFFIO_TX_T19p	DIFFIN_T19p*	H18	K13	DQS15T	DQ8T/CQn8T	DQ4T	DQ2T/CQn2T	DQS9T	DQ5T/CQn5T	DQ2T	DQ1T/CQn1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	C12	F13	DQ15T	DQ8T	DQ4T	DQ2T	DQ9T	DQ5T	DQ2T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_TX_T19n	DIFFIN_T19n*	G18	K12	DQSn15T	DQ8T	DQ4T	DQ2T	DQSn9T	DQ5T	DQ2T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	F16	E13								
7A	TIO8	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFIN_T20p*	D16	C13	DQ15T	DQ8T	DQ4T	DQ2T	DQ9T	DQ5T	DQ2T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	E16	D13	DQ15T	DQ8T	DQ4T	DQ2T	DQ9T	DQ5T	DQ2T	DQ1T
7A	TIO8	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFIN_T20n*	C16	C12	DQ15T	DQ8T	DQ4T	DQ2T	DQ9T	DQ5T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	B13	B6	DQ14T	DQ7T	DQ4T	DQ2T	DQ8T	DQ4T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T21p	DIFFIN_T21p*	G17	K14								
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	B12	A6	DQ14T	DQ7T	DQ4T	DQ2T	DQ8T	DQ4T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T21n	DIFFIN_T21n*	G16	J14	DQ14T	DQ7T	DQ4T	DQ2T	DQ8T	DQ4T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	A12	A10								
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFIN_T22p*	B10	A8	DQS14T	DQS7T/CQ7T	DQS4T/CQ4T	DQ2T	DQS8T	DQS4T/CQ4T	DQS2T/CQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T22n	DIFFOUT_T22n	A11	A9	DQ14T	DQ7T	DQ4T	DQ2T	DQ8T	DQ4T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFIN_T22n*	A10	A7	DQSn14T	DQSn7T/DQ7T	DQSn4T/DQ4T	DQ2T	DQSn8T	DQSn4T/DQ4T	DQSn2T/DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	A14	B12								
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T23p	DIFFIN_T23p*	M17	G14	DQS13T	DQ7T/CQn7T	DQ4T/CQn4T	DQ2T	DQS7T	DQ4T/CQn4T	DQ2T/CQn2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	A13	A11	DQ13T	DQ7T	DQ4T	DQ2T	DQ7T	DQ4T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T23n	DIFFIN_T23n*	M16	F14	DQSn13T	DQ7T	DQ4T	DQ2T	DQSn7T	DQ4T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T24p	B15	A13								
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFIN_T24p*	B16	A15	DQ13T	DQ7T	DQ4T	DQ2T	DQ7T	DQ4T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T24n	A15	A12	DQ13T	DQ7T	DQ4T	DQ2T	DQ7T	DQ4T	DQ2T	DQ1T
7A	TIO7	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFIN_T24n*	A16	A14	DQ13T	DQ7T	DQ4T	DQ2T	DQ7T	DQ4T	DQ2T	DQ1T
8A		VREFB8AN0	CLK12	DIFFCLK_4p				F18	D15								
7A		VREFB7AN0	CLK13	DIFFCLK_5p				K18	D14								
8A		VREFB8AN0	CLK14	DIFFCLK_4n				F17	C15								
7A		VREFB7AN0	CLK15	DIFFCLK_5n				J18	C14								
8A	TIO6	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	D18	C16	DQ12T	DQ6T	DQ3T	DQ1T	DQ6T	DQ3T	DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_TX_T25p	DIFFIN_T25p*	N19	F16								
8A	TIO6	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	D17	B15	DQ12T	DQ6T	DQ3T	DQ1T	DQ6T	DQ3T	DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_TX_T25n	DIFFIN_T25n*	M18	E15	DQ12T	DQ6T	DQ3T	DQ1T	DQ6T	DQ3T	DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	C18	A18								
8A	TIO6	VREFB8AN0	IO			DIFFIO_TX_T26p	DIFFIN_T26p*	A18	B16	DQS12T	DQS6T/CQ6T	DQS3T/CQ3T	DQ1T	DQS6T	DQS3T/CQ3T	DQS1T/CQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	B18	A17	DQ12T	DQ6T	DQ3T	DQ1T	DQ6T	DQ3T	DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_TX_T26n	DIFFIN_T26n*	A17	A16	DQSn12T	DQSn6T/DQ6T	DQSn3T/DQ3T	DQ1T	DQSn6T	DQSn3T/DQ3T	DQSn1T/DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	B19	E15								
8A	TIO6	VREFB8AN0	IO			DIFFIO_TX_T27p	DIFFIN_T27p*	G19	H15	DQS11T	DQ6T/CQn6T	DQ3T/CQn3T	DQ1T	DQS5T	DQ3T/CQn3T	DQ1T/CQn1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	A19	D16	DQ11T	DQ6T	DQ3T	DQ1T	DQ5T	DQ3T	DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_TX_T27n	DIFFIN_T27n*	F19	G15	DQSn11T	DQ6T	DQ3T	DQ1T	DQSn5T	DQ3T	DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_RX_T28p	DIFFOUT_T28p	D19	A20								
8A	TIO6	VREFB8AN0	IO			DIFFIO_TX_T28p	DIFFIN_T28p*	A21	C19	DQ11T	DQ6T	DQ3T	DQ1T	DQ5T	DQ3T	DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_RX_T28n	DIFFOUT_T28n	C19	A19	DQ11T	DQ6T	DQ3T	DQ1T	DQ5T	DQ3T	DQ1T	
8A	TIO6	VREFB8AN0	IO			DIFFIO_TX_T28n	DIFFIN_T28n*	A20	B19	DQ11T	DQ6T	DQ3T	DQ1T	DQ5T	DQ3T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	C21	D17	DQ10T	DQ5T	DQ3T	DQ1T	DQ4T	DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_TX_T29p	DIFFIN_T29p*	K20	L15								
8A	TIO5	VREFB8AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	B21	C17	DQ10T	DQ5T	DQ3T	DQ1T	DQ4T	DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_TX_T29n	DIFFIN_T29n*	J20	K15	DQ10T	DQ5T	DQ3T	DQ1T	DQ4T	DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_RX_T30p	DIFFOUT_T30p	E19	D18								
8A	TIO5	VREFB8AN0	IO			DIFFIO_TX_T30p	DIFFIN_T30p*	A23	D21	DQS10T	DQS5T/CQ5T	DQ3T	DQS1T/CQ1T	DQS4T	DQS2T/CQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_RX_T30n	DIFFOUT_T30n	E18	C18	DQ10T	DQ5T	DQ3T	DQ1T	DQ4T	DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_TX_T30n	DIFFIN_T30n*	A22	C21	DQSn10T	DQSn5T/DQ5T	DQ3T	DQSn1T/DQ1T	DQSn4T	DQSn2T/DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	C22	D20								
8A	TIO5	VREFB8AN0	IO			DIFFIO_TX_T31p	DIFFIN_T31p*	J19	G17	DQS9T	DQ5T/CQn5T	DQ3T	DQ1T/CQn1T	DQS3T	DQ2T/CQn2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	B22	D19	DQ9T	DQ5T	DQ3T	DQ1T	DQ3T	DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_TX_T31n	DIFFIN_T31n*	H19	F17	DQSn9T	DQ5T	DQ3T	DQ1T	DQSn3T	DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_RX_T32p	DIFFOUT_T32p	B24	L19								
8A	TIO5	VREFB8AN0	IO			DIFFIO_TX_T32p	DIFFIN_T32p*	B25	J21	DQ9T	DQ5T	DQ3T	DQ1T	DQ3T	DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	A24	K20	DQ9T	DQ5T	DQ3T	DQ1T	DQ3T	DQ2T	DQ1T	
8A	TIO5	VREFB8AN0	IO			DIFFIO_TX_T32n	DIFFIN_T32n*	A25	J20	DQ9T	DQ5T	DQ3T	DQ1T	DQ3T	DQ2T	DQ1T	
8A	TIO4	VREFB8AN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	A27	F22	DQ8T	DQ4T	DQ2T	DQ1T	DQ2T	DQ1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_TX_T33p	DIFFIN_T33p*	G21	K16								
8A	TIO4	VREFB8AN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	A26	E22	DQ8T	DQ4T	DQ2T	DQ1T	DQ2T	DQ1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_TX_T33n	DIFFIN_T33n*	G20	J16	DQ8T	DQ4T	DQ2T	DQ1T	DQ2T	DQ1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_RX_T34p	DIFFOUT_T34p	D21	G24								
8A	TIO4	VREFB8AN0	IO			DIFFIO_RX_T34p	DIFFIN_T34p*	C28	F24	DQS8T	DQS4T/CQ4T	DQS2T/CQ2T	DQ1T	DQS2T	DQS1T/CQ1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_RX_T34n	DIFFOUT_T34n	D20	F23	DQ8T	DQ4T	DQ2T	DQ1T	DQ2T	DQ1T		

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
8A	TIO4	VREFB8AN0	IO			DIFFIO_TX_T34n	DIFFIN_T34n*	B27	E24	DQSn8T	DQSn4T/DQ4T	DQSn2T/DQ2T	DQ1T	DQSn2T	DQSn1T/DQ1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D23	F21								
8A	TIO4	VREFB8AN0	IO			DIFFIO_TX_T35p	DIFFIN_T35p*	G23	K18	DQS7T	DQ4T/CQn4T	DQ2T/CQn2T	DQ1T	DQS1T	DQ1T/CQn1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C24	E21	DQ7T	DQ4T	DQ2T	DQ1T	DQ1T	DQ1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_TX_T35n	DIFFIN_T35n*	F23	J17	DQSn7T	DQ4T	DQ2T	DQ1T	DQSn1T	DQ1T		
8A	TIO4	VREFB8AN0	IO		CRC_ERROR	DIFFIO_RX_T36p	DIFFOUT_T36p	F24	E19								
8A	TIO4	VREFB8AN0	IO			DIFFIO_TX_T36p	DIFFIN_T36p*	D24	G19	DQ7T	DQ4T	DQ2T	DQ1T	DQ1T	DQ1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_RX_T36n	DIFFOUT_T36n	E24	E18	DQ7T	DQ4T	DQ2T	DQ1T	DQ1T	DQ1T		
8A	TIO4	VREFB8AN0	IO			DIFFIO_TX_T36n	DIFFIN_T36n*	C25	G18	DQ7T	DQ4T	DQ2T	DQ1T	DQ1T	DQ1T		
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	F21		DQ6T	DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T37p	DIFFIN_T37p*	N20									
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	E21		DQ6T	DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T37n	DIFFIN_T37n*	M20		DQ6T	DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T38p	DIFFOUT_T38p	D27									
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T38p	DIFFIN_T38p*	D25		DQS6T	DQS3T/CQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T38n	DIFFOUT_T38n	C27		DQ6T	DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T38n	DIFFIN_T38n*	C26		DQSn6T	DQSn3T/DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E22									
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T39p	DIFFIN_T39p*	H21		DQS5T	DQ3T/CQn3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	D22		DQ5T	DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T39n	DIFFIN_T39n*	G22		DQSn5T	DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	D29									
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T40p	DIFFIN_T40p*	C30		DQ5T	DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	D28		DQ5T	DQ3T	DQ2T	DQ1T				
8A	TIO3	VREFB8AN0	IO			DIFFIO_TX_T40n	DIFFIN_T40n*	C29		DQ5T	DQ3T	DQ2T	DQ1T				
8A		VREFB8AN0	IO	RUP2				E25	L21								
8A		VREFB8AN0	IO	PLL1_CLKOUT1p				M21	K19								
8A		VREFB8AN0	IO	RDN2				D26	K21								
8A		VREFB8AN0	IO	PLL1_CLKOUT1n				L21	J18								
8A		VREFB8AN0	IO	PLL1_CLKOUT2p				F26	F20								
8A		VREFB8AN0	IO	PLL1_CLKOUT3p				K21	J19								
8A		VREFB8AN0	IO	PLL1_CLKOUT2n				F25	F19								
8A		VREFB8AN0	IO	PLL1_CLKOUT3n				J21	H19								
8B	TIO2	VREFB8BN0	IO			DIFFIO_RX_T41p	DIFFOUT_T41p	G25		DQ4T	DQ2T	DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_TX_T41p	DIFFIN_T41p*	K23									
8B	TIO2	VREFB8BN0	IO			DIFFIO_RX_T41n	DIFFOUT_T41n	G24		DQ4T	DQ2T	DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_TX_T41n	DIFFIN_T41n*	J22		DQ4T	DQ2T	DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	J27									
8B	TIO2	VREFB8BN0	IO			DIFFIO_TX_T42p	DIFFIN_T42p*	H27		DQS4T	DQS2T/CQ2T	DQS1T/CQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	J28		DQ4T	DQ2T	DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_TX_T42n	DIFFIN_T42n*	G26		DQSn4T	DQSn2T/DQ2T	DQSn1T/DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	G28									
8B	TIO2	VREFB8BN0	IO			DIFFIO_TX_T43p	DIFFIN_T43p*	L22		DQS3T	DQ2T/CQn2T	DQ1T/CQn1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	G27		DQ3T	DQ2T	DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_TX_T43n	DIFFIN_T43n*	K22		DQSn3T	DQ2T	DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	L28									
8B	TIO2	VREFB8BN0	IO			DIFFIO_TX_T44p	DIFFIN_T44p*	F27		DQ3T	DQ2T	DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	K28		DQ3T	DQ2T	DQ1T					
8B	TIO2	VREFB8BN0	IO			DIFFIO_TX_T44n	DIFFIN_T44n*	E27		DQ3T	DQ2T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J29		DQ2T	DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_TX_T45p	DIFFIN_T45p*	K24									
8B	TIO1	VREFB8BN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	H28		DQ2T	DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_TX_T45n	DIFFIN_T45n*	J24		DQ2T	DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	G30									
8B	TIO1	VREFB8BN0	IO			DIFFIO_TX_T46p	DIFFIN_T46p*	J30		DQS2T	DQS1T/CQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	F30		DQ2T	DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_TX_T46n	DIFFIN_T46n*	H30		DQSn2T	DQSn1T/DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	F28									
8B	TIO1	VREFB8BN0	IO			DIFFIO_TX_T47p	DIFFIN_T47p*	J25		DQS1T	DQ1T/CQn1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	E28		DQ1T	DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_TX_T47n	DIFFIN_T47n*	H24		DQSn1T	DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	G29									
8B	TIO1	VREFB8BN0	IO			DIFFIO_TX_T48p	DIFFIN_T48p*	E30		DQ1T	DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	F29		DQ1T	DQ1T	DQ1T					
8B	TIO1	VREFB8BN0	IO			DIFFIO_TX_T48n	DIFFIN_T48n*	D30		DQ1T	DQ1T	DQ1T					
8C			TDO		TDO			M27	L23								
8C			ASDO		ASDO			K27	J22								
8C			nCSO		nCSO			M26	H22								
8C			DATA0		DATA0			N26	K22								
8C			TDI		TDI			M25	H24								
8C			TMS		TMS			N25	J23								
8C			TCK		TCK			L24	L24								
8C			DCLK		DCLK			L25	K24								
			GND					U17	P14								
			GND					AD27	AB21								
			GND					M28	G22								
			GND					N27	K23								
			GND					Y34	Y28								
			GND					Y33	Y27								
			GND					Y30	W26								
			GND					Y29	W25								
			GND					Y27	V28								
			GND					Y25	V27								
			GND					W32	U26								
			GND					W31	U25								
			GND					W28	T28								
			GND					W26	T27								
			GND					V34	T24								
			GND					V33	T22								
			GND					V30	R26								
			GND					V29	R25								
			GND					V27	R23								
			GND					V25	R21								
			GND					U32	P28								
			GND					U31	P27								
			GND					U28	P24								
			GND					U26	P22								
			GND					T34	N26								
			GND					T33	N25								
			GND					T30	N23								
			GND					T29	N21								
			GND					T27	M28								
			GND					T25	M27								
			GND					R32	M24								
			GND					R31	L26								
			GND					R28	L25								

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			GND					R26	K28								
			GND					P34	K27								
			GND					P33	J26								
			GND					P30	J25								
			GND					P29	H28								
			GND					P28	H27								
			GND					P26	G26								
			GND					N32	G25								
			GND					N31	F28								
			GND					M34	F27								
			GND					M33	E26								
			GND					M30	E25								
			GND					M29	D28								
			GND					L32	D27								
			GND					L31	D24								
			GND					K34	D22								
			GND					K33	C26								
			GND					K30	C25								
			GND					K29	C24								
			GND					J32	C22								
			GND					J31	B28								
			GND					H34	B27								
			GND					H33	B25								
			GND					G32	B23								
			GND					G31	B22								
			GND					F34	B21								
			GND					F33	AH26								
			GND					E32	AH24								
			GND					E31	AH22								
			GND					D34	AH20								
			GND					D33	AG28								
			GND					C32	AG26								
			GND					C31	AG24								
			GND					B34	AG22								
			GND					B33	AG21								
			GND					B30	AG20								
			GND					B29	AF28								
			GND					B28	AF27								
			GND					AP33	AF26								
			GND					AP32	AF25								
			GND					AP30	AF23								
			GND					AN32	AE26								
			GND					AN31	AE25								
			GND					AN30	AE23								
			GND					AM34	AD28								
			GND					AM33	AD27								
			GND					AL32	AC26								
			GND					AL31	AC25								
			GND					AK34	AB28								
			GND					AK33	AB27								
			GND					AJ32	AA26								
			GND					AJ31	AA25								
			GND					AH34	A27								
			GND					AH33	A25								
			GND					AG32	A23								
			GND					AG31	A21								
			GND					AF34	Y7								
			GND					AF33	W9								
			GND					AF30	W22								
			GND					AF29	W19								
			GND					AE32	W17								
			GND					AE31	W15								
			GND					AD34	V8								
			GND					AD33	V5								
			GND					AD30	V20								
			GND					AD29	V2								
			GND					AC32	V18								
			GND					AC31	V16								
			GND					AB34	V14								
			GND					AB33	V12								
			GND					AB30	V10								
			GND					AB29	U9								
			GND					AB27	U17								
			GND					AA32	U13								
			GND					AA31	T8								
			GND					AA28	T20								
			GND					AA26	T18								
			GND					A33	T14								
			GND					A32	T10								
			GND					A31	R19								
			GND					A30	R13								
			GND					A28	P18								
			GND					Y23	P12								
			GND					Y21	N9								
			GND					Y19	N5								
			GND					Y17	N19								
			GND					Y15	N15								
			GND					Y13	N11								
			GND					W8	M16								
			GND					W5	M12								
			GND					W22	L8								
			GND					W20	L20								
			GND					W2	L17								
			GND					W18	L11								
			GND					W16	H5								
			GND					W14	H17								
			GND					W11	G9								
			GND					V23	E20								
			GND					V21	E11								
			GND					V19	B2								
			GND					V15	AG8								
			GND					V13	AG14								
			GND					U22	AD20								
			GND					U20	AD11								
			GND					U18	AA20								
			GND					U16	AA11								

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			GND					U14	U19								
			GND					T8	U15								
			GND					T5	U11								
			GND					T23	T5								
			GND					T21	T2								
			GND					T2	T16								
			GND					T19	T12								
			GND					T17	R9								
			GND					T15	R17								
			GND					T13	R11								
			GND					T11	P16								
			GND					R22	P10								
			GND					R20	N8								
			GND					R18	N2								
			GND					R16	N17								
			GND					R14	N13								
			GND					P8	M18								
			GND					P5	M14								
			GND					P25	M10								
			GND					P23	L5								
			GND					P21	L2								
			GND					P2	L14								
			GND					P19	H8								
			GND					P17	H2								
			GND					P15	H11								
			GND					P13	E23								
			GND					P11	E14								
			GND					N24	B20								
			GND					N22	B11								
			GND					N18	AG17								
			GND					N16	AD5								
			GND					N14	AD14								
			GND					N12	AA5								
			GND					L8	AA14								
			GND					L5	H20								
			GND					L26	H14								
			GND					L23	E5								
			GND					L20	E17								
			GND					L2	B5								
			GND					L17	B14								
			GND					L14	AG2								
			GND					K10	AD8								
			GND					J9	AD17								
			GND					H8	AA8								
			GND					H5	AA17								
			GND					H29	E8								
			GND					H26	E2								
			GND					H23	B8								
			GND					H20	B17								
			GND					H2	AG5								
			GND					H17	AG11								
			GND					H14	AD2								
			GND					H11	AB23								
			GND					E8	AA2								
			GND					E5									
			GND					E29									
			GND					E26									
			GND					E23									
			GND					E20									
			GND					E2									
			GND					E17									
			GND					E14									
			GND					E11									
			GND					B8									
			GND					B5									
			GND					B26									
			GND					B23									
			GND					B20									
			GND					B2									
			GND					B17									
			GND					B11									
			GND					AN5									
			GND					AN26									
			GND					AN20									
			GND					AN17									
			GND					AN11									
			GND					AK5									
			GND					AK26									
			GND					AK20									
			GND					AK17									
			GND					AK11									
			GND					AG5									
			GND					AG26									
			GND					AG20									
			GND					AG17									
			GND					AG11									
			GND					AE10									
			GND					AD5									
			GND					AD23									
			GND					AD2									
			GND					AD14									
			GND					AB21									
			GND					AB17									
			GND					AB13									
			GND					AA25									
			GND					AA2									
			GND					AA11									
			GND					B14									
			GND					AN8									
			GND					AN29									
			GND					AN23									
			GND					AN2									
			GND					AN14									
			GND					AK8									
			GND					AK29									
			GND					AK23									

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			GND					AK2									
			GND					AK14									
			GND					AG8									
			GND					AG29									
			GND					AG23									
			GND					AG2									
			GND					AG14									
			GND					AF9									
			GND					AD8									
			GND					AD26									
			GND					AD20									
			GND					AD17									
			GND					AB23									
			GND					AB19									
			GND					AB15									
			GND					AA5									
			GND					AA20									
			GND					AA14									
			GND					AA8									
			GND					AA22									
			GND					AA16									
			GND					AA18									
			VCC					V16	P15								
			VCC					Y24	W20								
			VCC					Y22	W18								
			VCC					Y20	W16								
			VCC					Y18	W14								
			VCC					Y16	V9								
			VCC					Y14	V21								
			VCC					W23	V19								
			VCC					W21	V17								
			VCC					W19	V15								
			VCC					W17	V13								
			VCC					W15	V11								
			VCC					W13	U20								
			VCC					V24	U18								
			VCC					V22	U16								
			VCC					V20	U14								
			VCC					V18	U12								
			VCC					V14	U10								
			VCC					U21	T9								
			VCC					U19	T19								
			VCC					U15	T17								
			VCC					U13	T15								
			VCC					T24	T13								
			VCC					T22	T11								
			VCC					T20	R18								
			VCC					T18	R16								
			VCC					T16	R14								
			VCC					T14	R12								
			VCC					R23	R10								
			VCC					R21	P9								
			VCC					R19	P19								
			VCC					R17	P17								
			VCC					R15	P13								
			VCC					R13	P11								
			VCC					P24	N20								
			VCC					P22	N18								
			VCC					P20	N16								
			VCC					P18	N14								
			VCC					P16	N12								
			VCC					P14	N10								
			VCC					P12	M9								
			VCC					N23	M20								
			VCC					N21	M19								
			VCC					N17	M17								
			VCC					N15	M15								
			VCC					N13	M13								
			VCC					AC23	M11								
			VCC					AB24	L18								
			VCC					AB22	L16								
			VCC					AB20	L13								
			VCC					AB18	L12								
			VCC					AB16	L10								
			VCC					AB14	K17								
			VCC					AB12									
			VCC					AA23									
			VCC					AA21									
			VCC					AA19									
			VCC					AA17									
			VCC					AA15									
			VCC					AA13									
			DNU					K25	H23								
			DNU					V17	R15								
			DNU					C4	F6								
			VCCBAT					L27	J24								
			VCCA_PLL_1					H25	G20								
			VCCA_PLL_2					J10	H9								
			VCCA_PLL_3					AF10	Y8								
			VCCA_PLL_4					AG25	AB20								
			VCCA_PLL_5					T9	P8								
			VCCA_PLL_6					W9	R7								
			VCCD_PLL_1					J26	H21								
			VCCD_PLL_2					K9	G8								
			VCCD_PLL_3					AE9	AA7								
			VCCD_PLL_4					AF26	AA21								
			VCCD_PLL_5					U8	P7								
			VCCD_PLL_6					V8	R8								
			VCCIO3A					AM20	AG16								
			VCCIO3A					AK24	AD19								
			VCCIO3A					AJ20	AD16								
			VCCIO3A					AH22									
			VCCIO3B					AF22									
			VCCIO3B					AF21									
			VCCIO3C					AD25	AC20								
			VCCIO4A					AM14	AG7								

Bank number	I/O Module (Note 1)	VREF	Pin Function	Optional Function	Configuration Function	Dedicated Tx/Rx Channel with OCT Rd	Emulated LVDS Output Channel/ Dedicated LVDS Input Channel with no OCT Rd (Note 2)	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 3)	DQS for X16/X18 for F1152 (Note 3)	DQS for X32/X36 for F1152 (Note 3)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 3)	DQS for X16/X18 for F780 (Note 3)	DQS for X32/X36 for F780 (Note 3)
			VCCIO4A					AM11	AG13								
			VCCIO4A					AL17	AG10								
			VCCIO4A					AJ17	AD13								
			VCCIO4A					AJ14	AD10								
			VCCIO4B					AH11									
			VCCIO4B					AJ8									
			VCCIO5A					AG3	Y2								
			VCCIO5A					AD3	U2								
			VCCIO5A					AA6	R2								
			VCCIO5A					AA3	AE2								
			VCCIO5B					AJ5									
			VCCIO5B					AH8									
			VCCIO6A					T6	K2								
			VCCIO6A					T3	G2								
			VCCIO6A					P3	D2								
			VCCIO6A					L3									
			VCCIO6B					L6									
			VCCIO6B					H6									
			VCCIO7A					F14	B7								
			VCCIO7A					F11	B4								
			VCCIO7A					C14	B13								
			VCCIO7A					C11	B10								
			VCCIO7B					D8									
			VCCIO7B					G8									
			VCCIO8A					F22	F18								
			VCCIO8A					F20	E16								
			VCCIO8A					C23	C20								
			VCCIO8A					C20	B18								
			VCCIO8A					C17									
			VCCIO8B					J23									
			VCCIO8B					H22									
			VCCIO8C					K26	G23								
			VCCPD3A					AC20	AB18								
			VCCPD3A					AC19	AA18								
			VCCPD3B					AC21									
			VCCPD3C					AC24	Y21								
			VCCPD4A					AD16	AA13								
			VCCPD4A					AC16	AA12								
			VCCPD4B					AC13									
			VCCPD5A					Y12	U8								
			VCCPD5A					AA12	U7								
			VCCPD5B					AC12									
			VCCPD6A					T12	M8								
			VCCPD6A					R12	M7								
			VCCPD6B					M11									
			VCCPD7A					M15	J13								
			VCCPD7A					M14	H13								
			VCCPD7B					L12									
			VCCPD8A					M19	H16								
			VCCPD8A					L19	G16								
			VCCPD8B					M22									
			VCCPD8C					M24	G21								
3A		VREFB3AN0	VREFB3AN0	VREFB3AN0				AE20	Y17								
3B		VREFB3BN0	VREFB3BN0	VREFB3BN0				AE22									
4A		VREFB4AN0	VREFB4AN0	VREFB4AN0				AD15	AB12								
4B		VREFB4BN0	VREFB4BN0	VREFB4BN0				AD13									
5A		VREFB5AN0	VREFB5AN0	VREFB5AN0				AB11	W7								
5B		VREFB5BN0	VREFB5BN0	VREFB5BN0				AD11									
6A		VREFB6AN0	VREFB6AN0	VREFB6AN0				N11	L9								
6B		VREFB6BN0	VREFB6BN0	VREFB6BN0				M12									
7A		VREFB7AN0	VREFB7AN0	VREFB7AN0				L15	H12								
7B		VREFB7BN0	VREFB7BN0	VREFB7BN0				K13									
8A		VREFB8AN0	VREFB8AN0	VREFB8AN0				K19	H18								
8B		VREFB8BN0	VREFB8BN0	VREFB8BN0				M23									
			NC					AL30	AF21								
			NC					AM30	AF22								
			VCCL_GXB					W25	R22								
			VCCL_GXB					V28	P23								
			VCCL_GXB					V26	P21								
			VCCL_GXB					U27	N24								
			VCCL_GXB					U25	N22								
			VCCL_GXB					T28	M23								
			VCCL_GXB					T26	T23								
			VCCL_GXB					R27	T21								
			VCCL_GXB					R25	R24								
			VCCL_GXB					Y28									
			VCCL_GXB					Y26									
			VCCL_GXB					W27									
			VCCCB					U23	Y15								
			VCCCB					U12	N7								
			VCCCB					L18	J15								
			VCCCB					AD18	P20								
			RREF0					AP31	AH21								
			RREF1					A29	A22								
			VCCA					U24	R20								
			VCCA					R24	M21								
			VCCA					AA24	U21								
			VCCA					W24									
			VCCH_GXB					P27	U23								
			VCCH_GXB					N28	U22								
			VCCH_GXB					AB28	M22								
			VCCH_GXB					AA27	L22								

Notes:

(1) An I/O module is a group of 16 I/O pins.

(2) When not used as DIFFIN or DIFFIO_TX, all pins marked with * (DIFFIN_[##]p/n) can be configured as emulated LVDS output channels (DIFFOUT).
Only DIFFIN pins of the same index group (e.g DIFFIN_B1p and DIFFIN_B1n) can be used to form an emulated LVDS output channel.

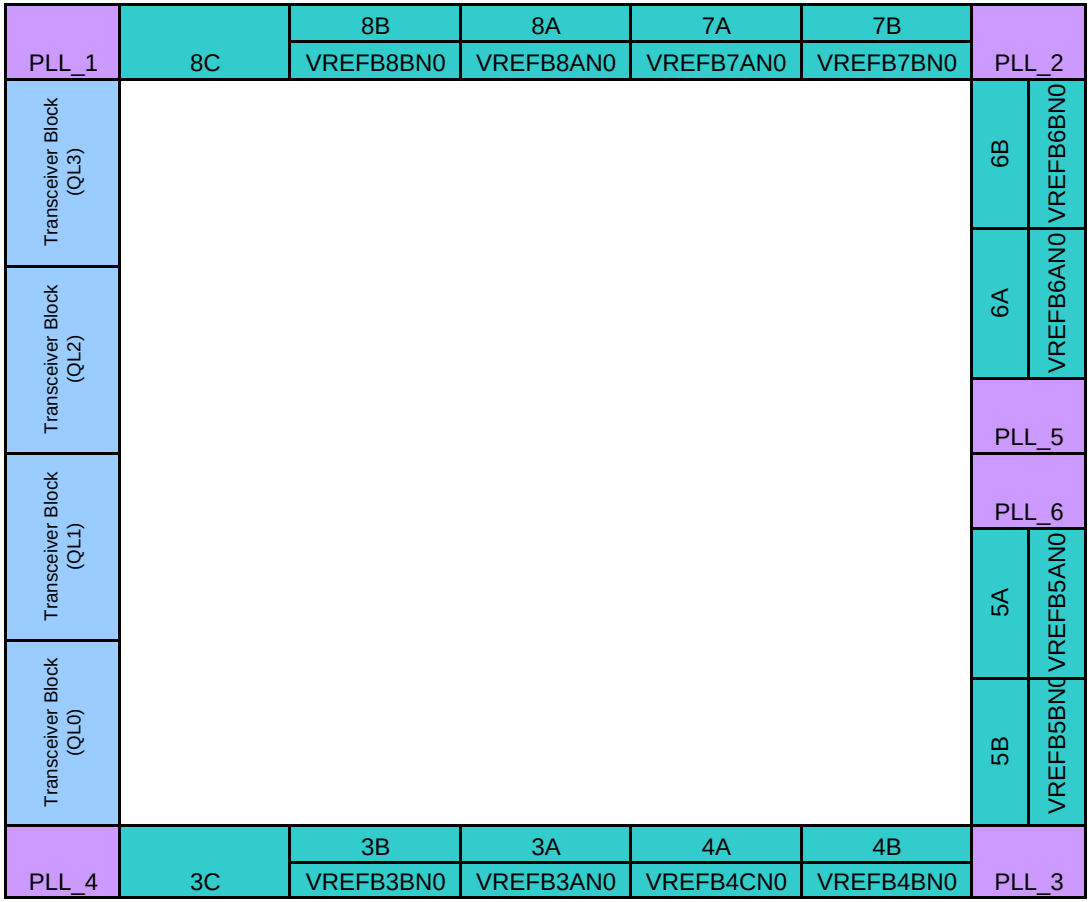
(3) When not used as clocks, the CQn and DQSn pins can be used as DQ pins.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
Clock and PLL Pins		
CLK[4:15]	Clock, Input	Single ended clock input pin.
DIFFCLK[0:5]p	Clock, Input	Clock input pin for differential clock input. OCT Rd is not supported.
DIFFCLK[0:5]n	Clock, Input	Negative clock input for differential clock input. OCT Rd is not supported
PLL_[1:4]_CLKOUT1p	I/O, Clock	PLL[1:4]_CLKOUT1 (except PLL1 and PLL3 in EP2AGX125 and EP2AGX260) supports 2 clock I/O pins, configured either as one single ended I/O or one differential I/O pair. PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1:4]_CLKOUT1n	I/O, Clock	
PLL_[1,3]_CLKOUT[2:3]p (Note 4)	I/O, Clock	PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.
PLL_[1,3]_CLKOUT[2:3]n (Note 4)	I/O, Clock	
Dedicated Configuration/JTAG Pins		
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5V, 1.8V, 2.5V, 3.0V o8.3V) turns off the weak pull-up, while a logic low turns them on.
MSEL[0:3]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be usedas a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as an user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
Optional/Dual-Purpose Configuration Pins		
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	I/O (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	Input	DATA[0] is a dedicated pin that is used for both the passive and active configuration modes
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration. DATA[1:7] pins can also be used as user I/O pins after configuration, but not DATA0.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX_[T,B,R][##]p, DIFFIO_RX_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels with OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX_[T,B,R][##]p, DIFFIO_TX_[T,B,R][##]n	I/O, TX channel	These are true LVDS transmitter channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS transmitter channels, these pins can be configured as true LVDS receiver channels without OCT Rd support (DIFFIN_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pins.
DIFFIN_[T,B,R][##]p, DIFFIN_[T,B,R][##]n	I/O, RX channel	These are true LVDS receiver channels without OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS receiver channels without OCT Rd support, these pins can be configure as true LVDS transmitter channels (DIFFIO_TX_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pin.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, (DIFFIO_RX_[T,B,R][##][p,n] , DIFFIN_[T,B,R][##][p,n]) can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[##][T,B,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B,R] (Note 5)	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[##][T,B,R] (Note 5)	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[0:2]	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[0:2]	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do Not Use (DNU).
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[1:6]	Power	Digital power for PLL[1:6]. All of these pins must be connected even if the PLL is not used
VCCCB	Power	Configuration RAM bits power supply.
VCCA_PLL_[1:6]	Power	Analog power for PLL [1:6]. All of these pins must be connected even if the PLL is not used
VCCIO[3:8][A,B]	Power	These are I/O supply voltage pins for banks 3 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V,3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V), 3.0V PCI/PCI-X and LVTTL (1.8V, 2.5V, 3.0V, 3.3V) I/O standards.
VCCIO[3,8]C	Power	These are configuration and JTAG supply voltage pins for banks 3C and 8C. Each bank can support a different voltage level. For AS/PP/FPP configuration schemes, VCCIO8C supports 1.8V, 2.5V, 3.0V or 3.3V. JTAG can support 1.5V, 1.8V, 2.5V, 3.0V or 3.3V.
VCCPD[3:8][A,B], VCCPD[3,8]C	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the input buffers for HSTL/SSTL input buffers. This can be connected to 3.3V, 3.0V or 2.5V. For 3.3V I/O standard connect VCCPD to 3.3V, for 3.0V I/O standard connect VCCPD to 3.0V and for 2.5V/1.8V/1.2V I/O standards connect VCCPD to 2.5V
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[3:8][A,B]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. These pins cannot be used as regular I/Os.
Transceiver Pins		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX and clocking.
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA	Power	Supplies power to the transceiver PMA regulator.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
GXB_RX[0:15]p (Note 6)	Input	High speed positive differential receiver channels.
GXB_RX[0:15]n (Note 6)	Input	High speed negative differential receiver channels.
GXB_TX[0:15]p (Note 6)	Output	High speed positive differential transmitter channels.
GXB_TX[0:15]n (Note 6)	Output	High speed negative differential transmitter channels.
REFCLK[0:7]p	Input	High speed differential reference clock positive.
REFCLK[0:7]n	Input	High speed differential reference clock complement.
RREF[0:1]	Input	Reference resistor for transceiver.

Notes:

1. Refer to the Arria II GX Device Datasheet and Pin Connection Guidelines for the recommended operating conditions.
2. This pin definition is prepared based on the EP2AGX260.
3. Some of the pull-up /pull down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
   The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
   Refer to the Configuring Arria II GX Devices chapter in the Arria II GX Device Handbook for more information.
4. PLL[1,3]_CLKOUT[2..3][p,n] are only available in PLL1 and PLL3 in EP2AGX125 and EP2AGX260.
5. When not used as clocks, the CQn and DQSn pins can be used as DQ pin.
6. Transceiver signals GXB_RX[15..0] and GXB_TX[15..0] are device specific.



This is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Version Number	Date	Changes Made
1.0	2/27/2009	Initial release.
1.1	5/29/2009	Added DNU in Pin List and Pin Definitions.