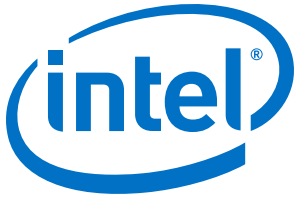

Intel® Arria® 10 GX, GT, and SX Device Family Pin Connection Guidelines

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Disclaimer

Intel® Arria® 10 GX and GT Pin Connection Guidelines

Clock and PLL Pins

Note: Intel® recommends that you create a Intel Quartus® Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 1. Clock and PLL Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK_[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_[0,1]p	I/O, Clock Input	Dedicated high speed clock input pins that can be used for data inputs or outputs. Differential input OCT R_D, single-ended input OCT R_T, and single-ended output OCT R_S are supported on these pins.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND. If you are using the Early I/O Release feature in the Intel Arria® 10 SX devices, ensure that the input clock to the HPS SDRAM IP is located within the active HPS I/O banks. For more information, refer to the *HPS EMIF Design Consideration* chapter of the *Intel Arria 10 SoC Design Guidelines*.
CLK_[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_[0,1]n	I/O, Clock Input	Dedicated high speed clock input pins that can be used for data inputs or outputs. Differential input OCT R_D, single-ended input OCT R_T, and single-ended output OCT R_S are supported on these pins.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND. If you are using the Early I/O Release feature in the Intel Arria 10 SX devices, ensure that the input clock to the HPS SDRAM IP is located within the active HPS I/O banks. For more information, refer to the *HPS EMIF Design Consideration* chapter of the *Intel Arria 10 SoC Design Guidelines*.
PLL_[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_FB[0,1]	I/O, Clock	Dual-purpose I/O pins that can be used as single-ended inputs, single-ended outputs, or external feedback input pin. For more information about the supported pins, refer to the device pinout file.	Tie the unused pins to GND or leave them unconnected.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_CLKOUT[0:1], PLL_[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_CLKOUT[0:1]p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair. For more information about the supported pins, refer to the device pinout file.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_CLKOUT[0:1]n	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair. For more information about the supported pins, refer to the device pinout file.	Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.

Dedicated Configuration/JTAG Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 2. Dedicated Configuration/JTAG Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
nIO_PULLUP	Input	Dedicated input pin that determines the internal pull-ups on user I/O pins and dual-purpose I/O pins (DATA[0:31], CLKUSR, INIT_DONE, DEV_OE, and DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns on the weak pull-up.	Tie the nIO-PULLUP pin directly to VCC using a 1 kΩ pull-up resistor, or directly to GND. This pin has an internal 25-kΩ pull-down. If you tie this pin to VCC, ensure all user I/O pins and dual-purpose I/O pins are at logic–0 before and during configuration.
TEMPDIODEp	Input	Pin used for temperature sensing diode (bias-high input) inside the FPGA.	If you do not use the temperature sensing diode with an external temperature sensing device, connect this pin to GND.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
TEMPDIODEn	Input	Pin used for temperature sensing diode (bias-low input) inside the FPGA.	If you do not use the temperature sensing diode with an external temperature sensing device, connect this pin to GND.
MSEL[0:2]	Input	Configuration input pins that set the configuration scheme for the FPGA device.	These pins are internally connected through a 25-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused, connect them to GND. Depending on the configuration scheme used, tie these pins to VCCPGM or GND. For more information about the configuration scheme options, refer to the *Configuration, Design Security, and Remote System Upgrades for Intel Arria 10 Devices* chapter. If you use JTAG configuration scheme, connect these pins to GND.
nCE	Input	Dedicated active-low chip enable pin. When the nCE pin is low, the device is enabled. When the nCE pin is high, the device is disabled.	In multi-device configuration, the nCE pin of the first device is tied low while its nCEO pin drives the nCE pin of the next device in the chain. In single-device configuration and JTAG programming, connect the nCE pin to GND.
nCONFIG	Input	Dedicated configuration control input pin. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level initiates reconfiguration.	Connect the nCONFIG pin directly to the configuration controller when the FPGA uses a passive configuration scheme. Connect the nCONFIG pin through a 10-kΩ resistor tied to VCCPGM when the FPGA uses an active serial (AS) configuration scheme. If you do not use this pin, connect the pin directly or through a 10-kΩ resistor to VCCPGM.
CONF_DONE	Bidirectional (open-drain)	Dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. After all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, the CONF_DONE pin goes high after all data is received. Then the device initializes and enters user mode. This pin is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistors to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host. When you use passive configuration schemes, the configuration controller monitors this pin.
nCEO	I/O, Output (open-drain)	When device configuration is complete, the nCEO pin drives low. If you do not use this pin as a configuration pin, you can use this pin as a user I/O pin.	In multi-device configuration, the nCEO pin feeds the nCE pin of a subsequent FPGA. Connect this pin through an external 10-kΩ pull-up resistor to VCCPGM.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			In single-device configuration, you can leave this pin floating.
nSTATUS	Bidirectional (open-drain)	Dedicated configuration status pin. The FPGA drives the nSTATUS pin low immediately after power-up, and releases the pin after power-on reset (POR) time. As a status output, the nSTATUS pin is pulled low if an error occurs during configuration. As a status input, the device enters an error state when the nSTATUS pin is driven low by an external source during configuration or initialization. This pin is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistors to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host. When you use passive configuration schemes, the configuration controller monitors this pin.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin through a 1-kΩ pull-down resistor to GND. This pin has an internal 25-kΩ pull-down. Do not drive voltage higher than 1.8-, 1.5-, or 1.2-V VCCPGM supply for the TCK pin. The TCK input pin is powered by the VCCPGM supply.
TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 1–10-kΩ pull-up resistor to VCCPGM. If the JTAG interface is not used, connect the TMS pin to VCCPGM using a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up. Do not drive voltage higher than 1.8-, 1.5-, or 1.2-V VCCPGM supply for the TMS pin. The TMS input pin is powered by the VCCPGM supply.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 1–10-kΩ pull-up resistor to VCCPGM. If the JTAG interface is not used, connect the TDI pin to VCCPGM using a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up. Do not drive voltage higher than 1.8-, 1.5-, or 1.2-V VCCPGM supply for the TDI pin. The TDI input pin is powered by the VCCPGM supply.
TDO	Output	Dedicated JTAG test data output pin.	If the JTAG interface is not used, leave the TDO pin unconnected.
TRST	Input	Dedicated active low JTAG test reset input pin. The TRST pin is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of the TRST pin is optional. If you do not use this pin, tie this pin through a 1-kΩ pull-up resistor to VCCPGM.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			When you use this pin, ensure that the TMS pin is held high or the TCK pin is static when the TRST pin is changing from low to high. To disable the JTAG circuitry, tie this pin to GND. This pin has an internal 25-kΩ pull-up. Do not drive voltage higher than 1.8-, 1.5-, or 1.2-V VCCPGM supply for the TRST pin. The TRST input pin is powered by the VCCPGM supply.
nCSO[0:2]	Output	Dedicated output control signal from the FPGA to the EPCQ-L device in AS configuration scheme that enables the EPCQ-L device.	When you are not programming the FPGA in the AS configuration scheme, the nCSO pin is not used. When you do not use this pin as an output pin, leave this pin unconnected.

Optional/Dual-Purpose Configuration Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 3. Optional/Dual-Purpose Configuration Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DCLK	Input (PS, FPP); Output (AS)	Dedicated configuration clock pin. In passive serial (PS) and fast passive parallel (FPP) configuration schemes, DCLK is used to clock configuration data from an external source into the FPGA. In the AS configuration scheme, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	I/O, Output (open-drain)	Active high signal indicates the error detection circuit has detected errors in the configuration RAM (CRAM) bits. Falling edge of this signal indicates the information about the error location and type are available in the error message register (EMR). This dual-purpose pin is only used when you enable error detection in user mode. This pin can be used as a user I/O pin.	When you use the open-drain output dedicated CRC_ERROR pin as an optional pin, connect this pin through an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the open-drain output dual-purpose CRC_ERROR pin as an optional pin, and the CRC_ERROR pin is not used as an I/O pin, connect this pin as defined in the Intel Quartus Prime software.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared. When this pin is driven high (VCCPGM), all registers behave as programmed.	When you do not use the dual-purpose DEV_CLRn pin and when this pin is not used as an I/O pin, tie this pin to GND.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated. When this pin is driven high (VCCPGM), all I/O pins behave as programmed.	When you do not use the dual-purpose DEV_OE pin and when this pin is not used as an I/O pin, tie this pin to GND.
DATA0	I/O, Input	Dual-purpose configuration data input pin. You can use the DATA0 pin for PS or FPP configuration scheme, or as an I/O pin after configuration is complete.	When you do not use the dedicated input DATA0 pin and when this pin is not used as an I/O pin, leave this pin unconnected.
DATA[1:31]	I/O, Input	Dual-purpose configuration data input pins. Use DATA [1:7] pins for FPP x8, DATA [1:15] pins for FPP x16, and DATA [1:31] pins for FPP x32 configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When you do not use the dual-purpose DATA[1:31] pins and when these pins are not used as I/O pins, leave these pins unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as the INIT_DONE pin. When you enable this pin, a transition from low to high at the pin indicates the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	When you use the optionally open-drain output dedicated INIT_DONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you use this pin in an AS or PS multi-device configuration mode, ensure you enable the INIT_DONE pin in the Intel Quartus Prime designs. When you do not use the dedicated INIT_DONE optionally open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Intel Quartus Prime software.
nPERST[L,R][0:1]	I/O, Input	Dual-purpose fundamental reset pin that is only available when you use together with PCI Express* (PCIe*) hard IP (HIP). When the pin is low, the transceivers are in reset. When the pin is high, the transceivers are out of reset. When you do not use this pin as the fundamental reset, you can use this pin as a user I/O pin.	Connect this pin as defined in the Intel Quartus Prime software. This pin is powered by 1.8V VCCIO supply and must be driven by 1.8V compatible I/O standards. Connect the PCIe nPERST pin to a level translator to shift down the voltage from 3.3V LVTTL to 1.8V to interface with this pin. When this pin is not used for configuration purpose, you have the option to select 1.2V, 1.5V, or 1.8V compatible I/O standard. However, you must shift down the 3.3V LVTTL voltage from the PCIe nPERST pin to the selected Intel Arria 10 nPERST I/O standard voltage level.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			Only one nPERST pin is used per PCIe HIP. The Intel Arria 10 components always have all four pins listed even when the specific component might only have 1 or 2 PCIe HIPs. • nPERSTL0 = Bottom Left PCIe HIP & CvP • nPERSTL1 = Top Left PCIe HIP (When available) • nPERSTR0 = Bottom Right PCIe HIP (When available) • nPERSTR1 = Top Right PCIe HIP (When available) For maximum compatibility, always use the bottom left PCIe HIP first, as this is the only location that supports Configuration via Protocol (CvP) using the PCIe link.
AS_DATA0/ASDO	Bidirectional	Dedicated AS configuration pin. When using an EPCQ-L device (x1 mode), this is the ASDO pin and is used to send address and control signals between the FPGA device and the EPCQ-L device.	When you do not program the device in the AS configuration mode, the ASDO pin is not used. When you do not use this pin, leave the pin unconnected.
AS_DATA[1:3]	Bidirectional	Dedicated AS configuration data pins. Configuration data is transported on these pins when connected to the EPCQ-L devices.	When you do not use this pin, leave the pin unconnected.

Partial Reconfiguration Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 4. Partial Reconfiguration Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
PR_REQUEST	I/O, Input	Partial reconfiguration request pin. Drive this pin high to start partial reconfiguration. Drive this pin low to end reconfiguration.	When you do not use the dedicated input PR_REQUEST pin, and when this pin is not used as an I/O pin, tie this pin to GND.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		You can only use this pin in partial reconfiguration using an external host mode in FPP x16 configuration scheme.	
PR_READY	I/O, Output or Output (open-drain)	The partial reconfiguration ready pin is driven low until the device is ready to begin partial reconfiguration. When the device is ready to start reconfiguration, this signal is released and pulled high by an external pull-up resistor.	When you use as optionally open-drain output dedicated PR_READY pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use as the dedicated PR_READY optionally open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Intel Quartus Prime software.
PR_ERROR	I/O, Output or Output (open-drain)	The partial reconfiguration error pin is driven low during partial reconfiguration unless the device detects an error. If an error is detected, this signal is released and pulled high by an external pull-up resistor.	When you use as optionally open-drain output dedicated PR_ERROR pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use as the dedicated PR_ERROR optionally open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Intel Quartus Prime software.
PR_DONE	I/O, Output or Output (open-drain)	The partial reconfiguration done pin is driven low until the partial reconfiguration is complete. When the reconfiguration is complete, this signal is released and pulled high by an external pull-up resistor.	When you use as optionally open-drain output dedicated PR_DONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use as the dedicated PR_DONE optionally open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Intel Quartus Prime software.
CvP_CONFDONE	I/O, Output (open-drain)	CvP done pin is driven low during configuration. When the CvP configuration is complete, this signal is released and pulled high by an external pull-up resistor. Status of this pin is only valid if the CONF_DONE pin is high.	When you use as optionally open-drain output dedicated CvP_CONFDONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use as the dedicated CvP_CONFDONE optionally open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Intel Quartus Prime software.

Differential I/O Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 5. Differential I/O Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
LVDS[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_[1:24]p, LVDS[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_[1:24]n	I/O, TX/RX channel	These are true LVDS receiver/transmitter channels on column I/O banks. Each I/O pair can be configured as LVDS receiver or LVDS transmitter. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Intel Quartus Prime software.

External Memory Interface and Hard Memory PHY Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 6. External Memory Interface and Hard Memory PHY Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DQS[#]	I/O,bi-directional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.
DQSn[#]	I/O,bi-directional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.
DQ[#]	I/O,bi-directional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, if you plan on migrating to a different memory interface that has a different DQ bus width, you will need to reevaluate your pin assignments. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in the Intel Quartus Prime software.
CQ[#]	I/O, Input	Optional data strobe signal for use in QDRII/II+/II+ Xtreme SRAM. These are the pins for echo clocks.	Connect unused pins as defined in the Intel Quartus Prime software.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
CQn[#]	I/O, Input	Optional complementary data strobe signal for use in QDRII/II+/II+ Xtreme SRAM. These are the pins for echo clocks.	Connect unused pins as defined in the Intel Quartus Prime software.
DQS[#]_[#]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in the Intel Quartus Prime software.
DQSn[#]_[#]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.
DQ[#]_[#]_[#]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, if you plan on migrating to a different memory interface that has a different DQ bus width, you will need to reevaluate your pin assignments. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in the Intel Quartus Prime software.
CQ[#]_[#]/CQn[#]_[#]	I/O, Input	Optional data strobe signal for use in QDRII/II+/II+ Xtreme SRAM. These are the pins for echo clocks.	Connect unused pins as defined in the Intel Quartus Prime software.
QK[#]_[#]	I/O, Input	Optional data strobe signal for use in RLDRAM 3.	Connect unused pins as defined in the Intel Quartus Prime software.
QKn[#]_[#]	I/O, Input	Optional complementary data strobe signal for use in RLDRAM 3.	Connect unused pins as defined in the Intel Quartus Prime software.
DM[#]_[#]	I/O, Output	Optional write data mask, edge-aligned to DQ during write.	Connect unused pins as defined in the Intel Quartus Prime software.
RESET_N_0	I/O, Output	Active low reset signal.	Connect unused pins as defined in the Intel Quartus Prime software.
A_[#]	I/O, Output	Address input for DDR3, DDR4, QDRII/II+/II+ Xtreme SRAM, and RLDRAM3.	Connect unused pins as defined in the Intel Quartus Prime software.
BA_[#]	I/O, Output	Bank address input for DDR2, DDR3, and RLDRAM 3.	Connect unused pins as defined in the Intel Quartus Prime software.
CK_[#]	I/O, Output	Input clock for external memory devices.	Connect unused pins as defined in the Intel Quartus Prime software.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
CK_N_[#]	I/O, Output	Input clock for external memory devices, inverted CK.	Connect unused pins as defined in the Intel Quartus Prime software.
CKE_[#]	I/O, Output	High signal enables clock, low signal disables clock.	Connect unused pins as defined in the Intel Quartus Prime software.
CS_N_[#]	I/O, Output	Active low chip select.	Connect unused pins as defined in the Intel Quartus Prime software.
REF#	I/O, Output	Auto-refresh control input for RLDRAM 3.	Connect unused pins as defined in the Intel Quartus Prime software.
ODT_[#]	I/O, Output	On die termination signal to set the termination resistors to each pin.	Connect unused pins as defined in the Intel Quartus Prime software.
WE_N_0	I/O, Output	Write-enable input for DDR3 SDRAM, RLDRAM 3, and all supported protocols.	Connect unused pins as defined in the Intel Quartus Prime software.
CAS_N_0	I/O, Output	Column address strobe for DDR3 SDRAM.	Connect unused pins as defined in the Intel Quartus Prime software.
RAS_N_0	I/O, Output	Row address strobe for DDR3 SDRAM.	Connect unused pins as defined in the Intel Quartus Prime software.
RPS_N_0	I/O, Output	Read signal to QDRII/II+/II+ Xtreme memory. Active low and reset in the inactive state.	Connect unused pins as defined in the Intel Quartus Prime software.
WPS_N_0	I/O, Output	Write signal to QDRII/II+/II+ Xtreme memory. Active low and reset in the inactive state.	Connect unused pins as defined in the Intel Quartus Prime software.
ALERT_N_0	I/O, Input	Alert input that indicate to the system's memory controller that a specific alert or event has occurred.	Connect unused pins as defined in the Intel Quartus Prime software. If you are using the Early I/O Release feature in the Intel Arria 10 SX devices, ensure that this pin is located within the active HPS I/O banks. For more information, refer to the *HPS EMIF Design Consideration* chapter of the *Intel Arria 10 SoC Design Guidelines*.
PAR_0	I/O, Output	Command and Address Parity Output: DDR4 supports even parity check in DRAMs with MR setting. Once PAR is enabled via Register in MR5, then DRAM calculates parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Output parity should maintain at the rising edge of the clock and at the same time with command and address with CS_n low.	Connect unused pins as defined in the Intel Quartus Prime software.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
ACT_N_0	I/O, Output	Command output that indicates an ACTIVATE command. Applies for DDR4.	Connect unused pins as defined in the Intel Quartus Prime software.
BG_[#]	I/O, Output	Bank group address outputs that define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Applies for DDR4.	Connect unused pins as defined in the Intel Quartus Prime software.
C_[#]	I/O, Output	Stack address inputs that are used when devices are stacked. Applies for DDR4.	Connect unused pins as defined in the Intel Quartus Prime software.
RM_[1,0]	I/O, Output	Rank multiplication.	Connect unused pins as defined in the Intel Quartus Prime software.
PE_N_0	I/O, Input	Address parity error.	Connect unused pins as defined in the Intel Quartus Prime software.
AP_0	I/O, Output	Address parity.	Connect unused pins as defined in the Intel Quartus Prime software.
AINV_0	I/O, Output	Address inversion state for address bus.	Connect unused pins as defined in the Intel Quartus Prime software.
RW[A,B]_N_0	I/O, Output	Synchronous read/write input.	Connect unused pins as defined in the Intel Quartus Prime software.
DOFF_N_0	I/O, Output	Phase-locked loop (PLL) turn off for QDR II/ II + SDRAM.	Connect unused pins as defined in the Intel Quartus Prime software.
LD[A,B]_N_0	I/O, Output	Synchronous load input.	Connect unused pins as defined in the Intel Quartus Prime software.
REF_N_0	I/O, Output	Auto-refresh control input for RLDRAM 3.	Connect unused pins as defined in the Intel Quartus Prime software.
CFG_N_0	I/O, Output	Configuration bit.	Connect unused pins as defined in the Intel Quartus Prime software.
LBK[#]_N_0	I/O, Output	Loop-back mode.	Connect unused pins as defined in the Intel Quartus Prime software.

Reference Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 7. Reference Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RZQ_[#], VID_EN	I/O	Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located. Connect the external precision resistor to the designated pin within the bank. If not required, this pin is a regular I/O pin.	When using OCT tie these pins to GND through either a 240-Ω or 100-Ω resistor, depending on the desired OCT impedence. Refer to the *Intel Arria 10 Device Handbook* for the OCT impedence options for the desired OCT scheme. If you are using the Early I/O Release feature in the Intel Arria 10 SX devices, ensure that this pin is located within the active HPS I/O banks. For more information, refer to the *HPS EMIF Design Consideration* chapter of the *Intel Arria 10 SoC Design Guidelines*.
		The VID_EN pin is not a physical pin. The VID_EN pin is a multi-function shared pin with the RZQ_2A pin.	If you are using the SmartVID feature, you have the option to enable the VID_EN function using the RZQ_2A pin. If you use the RZQ_2A pin as the VID_EN pin, you cannot use the RZQ_2A pin for OCT calibration. If you are using the RZQ_2A pin for OCT calibration, you have the option to use other available general-purpose I/O pins for the VID_EN function.
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, GND, or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration, you have the option to connect these pins to either power, GND, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.

Voltage Sensor Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 8. Voltage Sensor Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VREFP_ADC	Input	Dedicated precision analog voltage reference.	Tie VREFP_ADC to an external 1.25V accurate reference source (+/- 0.2%) for better ADC performance. Treat VREFP_ADC as an analog signal that together with the VREFN_ADC signal provides a differential 1.25V voltage. If no external reference is supplied, always connect VREFP_ADC to GND. An on-chip reference source (+/-10%) is activated by connecting this pin to GND. VREFP_ADC must be equal to or lower than VCCA_PLL to prevent damage.
VREFN_ADC	Input		Tie VREFN_ADC to the GND pin of an external 1.25V accurate reference source (+/- 0.2%) for better ADC performance. Treat VREFN_ADC as an analog signal that together with the VREFP_ADC signal provides a differential 1.25V voltage. If no external reference is supplied, always connect VREFN_ADC to GND.
VSIGP_[0,1]	Input	2 pairs of analog differential inputs pins used with the voltage sensor inside the FPGA to monitor external analog voltages.	Tie these pins to GND of the voltage sensor feature if not used. For details on the usage of these pins, refer to the *Power Management in Intel Arria 10 Devices* chapter. Do not drive VSIGP and VSIGN pins until the VCCA_PLL power rail has reached 1.62V to prevent damage.
VSIGN_[0,1]	Input		

Supply Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 9. Supply Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCP	Power	VCCP supplies power to the periphery.	VCC, VCCP, and VCCERAM must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator unless the SmartVID feature is used, as described below. You can operate -1 and -2 speed grade devices at 0.9V or 0.95V typical value. You can operate -3 speed grade device only at 0.9V typical value. Operating at 0.95V results in higher core performance and higher power consumption. For more information about the performance and power consumption, refer to the Intel Quartus Prime software timing reports and Intel Arria 10 Early Power Estimator (EPE). For details about the recommended operating conditions, refer to the Electrical Characteristics in the device datasheet. Use the Intel Arria 10 Early Power Estimator (EPE) to determine the current requirements for VCCP and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board. See Notes 2, 3, 4, 5, 6, and 10.
VCC	Power	VCC supplies power to the core. VCC also supplies power to the Hard IP for PCI Express cores.	VCC, VCCP, and VCCERAM must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator unless the SmartVID feature is used, as described below. You can operate -1 and -2 speed grade devices at 0.9V or 0.95V typical value. You can operate -3 speed grade device only at 0.9V typical value. Operating at 0.95V results in higher core performance and higher power consumption. For more information about the performance and power consumption, refer to the Intel Quartus Prime software timing reports and Intel Arria 10 Early Power Estimator (EPE). For details about the recommended operating conditions, refer to the Electrical Characteristics in the device datasheet. Use the Intel Arria 10 Early Power Estimator (EPE) to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board. See Notes 2, 3, 4, 5, 6, and 10.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCPT	Power	Power supply for the programmable power technology and I/O pre-drivers.	Connect VCCPT to a 1.8V low noise switching regulator. You have the option to source the following from the same regulator as VCCPT: • VCCH_GXB, VCCA_PLL, VCCPLL_HPS with proper isolation filtering • VCCIOREF_HPS • VCCBAT if it is using the same voltage level and the design security key feature is not required If you are not using HPS, do not share VCCPLL_HPS and VCCIOREF_HPS with VCCPT. Provide a minimum decoupling of 1uF for the VCCPT power rail near the VCCPT pin. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Arria 10 Devices*. See Notes 2, 3, 4, 7, and 10.
VCCA_PLL	Power	PLL analog power.	Connect VCCA_PLL to a 1.8V low noise switching regulator. With proper isolation filtering, you have the option to source VCCA_PLL from the same regulator as VCCPT. See Notes 2, 3, 4, 7, and 10.
VCCIO([2][A, F,G,H,I,J,K, L, AF, KL], [3][A, B,C,D,E,F,G, H, AB, GH])	Power	These are I/O supply voltage pins for banks 1 through 12. Each bank can support a different voltage level. Supports VCCIO standards that include Diff HSTL/HSTL(12, 15, 18), Diff SSTL/SSTL(12, 125, 135, 15, 18), Diff HSUL/HSUL(12), Diff POD 12, LVDS/Mini_LVDS/RSDS, 1.2V, 1.5V, 1.8V, 2.5V, 3.0V I/O standards.	Connect these pins to 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V, or 3.0V supplies, depending on the I/O standard required by the specified bank. When these pins require the same voltage level as VCCPGM, you have the option to tie them to the same regulator as VCCPGM. Not all I/O banks support 2.5V or 3.0V supplies. Not all devices support 3.0V I/O standard. For more details, refer to the *I/O and High Speed I/O in Intel Arria 10 Devices*. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Arria 10 Devices*. See Notes 2, 3, 4, 8, and 10.
VCCPGM	Power	Configuration pins power supply.	Connect these pins to a 1.2V, 1.5V, or 1.8V power supply. When dual-purpose configuration pins are used for configuration, tie VCCIO of the bank to the same regulator as VCCPGM, ranging from 1.2V, 1.5V, or 1.8V. When you do not use dual-purpose configuration pins for configuration, connect VCCIO to 1.2V, 1.25V, 1.35V, 1.5V, or 1.8V.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			When these pins require the same voltage level as VCCIO, you have the option to tie them to the same regulator as VCCIO. Provide a minimum decoupling of 47nF for the VCCPGM power rail near the VCCPGM pin. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Arria 10 Devices*. See Notes 2, 3, 4, and 10.
VCCERAM	Power	Memory power pins.	Connect all VCCERAM pins to a 0.9V or 0.95V linear or low noise switching power supply. You have the option to share VCCL_HPS with VCCERAM plane if the VCCL_HPS voltage is at the same level for Intel Arria 10 SX devices. VCC, VCCP, and VCCERAM must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a dedicated regulator that is separate from the VCCERAM regulator. When you use the SmartVID feature, VCCERAM must be equal to 0.9V. See Notes 2, 3, 7, and 10.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	When using the design security volatile key, connect this pin to a non-volatile battery power source in the range of 1.2V - 1.8V. When not using the volatile key, tie this pin to a supply ranging from more than 1.5V to 1.8V. If 1.8V is selected when the design security key is unused, you have the option to source this pin from the same regulator as VCCPT. This pin must be properly powered as per the recommended voltage range as the POR circuitry of the Intel Arria 10 devices monitoring VCCBAT. Provide a minimum decoupling of 47nF for the VCCBAT power rail near the VCCBAT pin. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Arria 10 Devices*.
GND	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
VREFB[[2][A, F,G,H,I,J,K, L], [3][A, B,C,D,E,F,G, H]]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then use these pins as voltage-reference pins for the bank.	If VREF pins are not used, connect them to either the VCCIO in the bank in which the pin resides or GND. See Notes 2, 8, 10, and 11. The following lists the four pairs of VREF pins in the RF40 package of the Intel Arria 10 GX devices that must be connected to the same voltage source on the board: • VREFB2AN0 and VREFB2FN0 • VREFB2KN0 and VREFB2LN0 • VREFB3AN0 and VREFB3BN0 • VREFB3GN0 and VREFB3HN0
VCCLSENSE	Power	Differential sense line to external regulator.	VCCLSENSE and GNDSENSE are differential remote sense pins for the VCC power. Connect your regulators' differential remote sense lines to the respective VCCLSENSE and GNDSENSE pins. This compensates for the DC IR drop associated with the PCB and device package from the VCC power. Route these connections as differential pair traces and keep them isolated from any other noise source. Connect VCCLSENSE and GNDSENSE lines to the regulator's remote sense inputs when I_{CC} current >30A or when the SmartVID feature is used. VCCLSENSE and GNDSENSE line connections are optional if I_{CC} current <=30A and the SmartVID feature is not used. However, Intel recommends connecting the VCCLSENSE and GNDSENSE for regulators that support remote sense line feature. If you do not use the VCCLSENSE and GNDSENSE pins, leave the VCCLSENSE and GNDSENSE pins unconnected.
GNDSENSE	Ground		
ADCGND	Ground	Dedicated quiet ground.	If you are using voltage sensor, you must connect ADCGND plane to board GND through a proper isolation filter with ferrite bead. Select the ferrite bead according to the frequency of the noise profile when it shows the maximum noise level. Alternatively, you can choose the ferrite bead based on the ADCGND maximum current value as well, which is 10 mA. If you are not using voltage sensor, isolation filter with ferrite bead to board GND is optional.

Transceiver Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 10. Transceiver Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCR_GXB[L1,R4][C,D,E,F,G,H,I,J]	Power	Analog power, receiver, specific to each transceiver bank of the left (L) side or right (R) side of the device.	Connect VCCR_GXB pins to a 0.95V, 1.03V, or 1.12V low noise switching regulator. 1.12V is applicable only for Intel Arria 10 GT devices. For transceivers data rates in respect to each voltage level, refer to the *Notes to Power Supply Sharing Guidelines*. If all of the transceivers, fPLLs, and IOPLLs on a side are not used, then the VCCR_GXB power rails of those inner banks on that side can be tied to GND to save power. The two outer banks on either the left or right side must always be powered on for proper operation of the device. The outer banks are always the first bank (lowest alphabetical letter) and last bank (highest alphabetical letter) on a side. Example 1—Device with 8 transceiver banks on a side. • VCCR_GXB1J—left side top outer bank. Do not power down. • VCCR_GXB1I • VCCR_GXB1H • VCCR_GXB1G • VCCR_GXB1F • VCCR_GXB1E • VCCR_GXB1D • VCCR_GXB1C—left side bottom outer bank. Do not power down. • VCCR_GXB4J—right side top outer bank. Do not power down. • VCCR_GXB4I • VCCR_GXB4H • VCCR_GXB4G • VCCR_GXB4F

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			• VCCR_GXB4E • VCCR_GXB4D • VCCR_GXB4C—right side bottom outer bank. Do not power down. Example 2—Device with 4 transceiver banks on a side. • VCCR_GXB1F—left side top outer bank. Do not power down. • VCCR_GXB1E • VCCR_GXB1D • VCCR_GXB1C—left side bottom outer bank. Do not power down. • VCCR_GXB4F—right side top outer bank. Do not power down. • VCCR_GXB4E • VCCR_GXB4D • VCCR_GXB4C—right side bottom outer bank. Do not power down. VCCR_GXB pins on the same side of the device must have the same voltage. The VCCT_GXB and VCCR_GXB power supplies voltage level must be equivalent if both power supplies are powered on. See Notes 2, 3, 4, 7, and 10.
VCCT_GXB[L1,R4][C,D,E,F,G,H,I,J]	Power	Analog power, transmitter, specific to each transceiver bank of the left (L) side or right (R) side of the device.	Connect VCCT_GXB pins to a 0.95V, 1.03V, or 1.12V low noise switching regulator. 1.12V is applicable only for Intel Arria 10 GT devices. For transceivers data rates in respect to each voltage level, refer to the *Notes to Power Supply Sharing Guidelines*. If all of the transceivers, fPLLs, and IOPLLs on a side are not used, then the VCCT_GXB power rails on that side can be tied to GND to save power regardless of whether they are an inner or outer bank. VCCT_GXB pins on the same side of the device must have the same voltage. The VCCT_GXB and VCCR_GXB power supplies voltage level must be equivalent if both power supplies are powered on. See Notes 2, 3, 4, 7, and 10.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCH_GXB[L,R]	Power	Analog power, block level transmitter buffers, specific to the left (L) side or right (R) side of the device.	Connect VCCH_GXB to 1.8V low noise switching regulator. With a proper isolation filtering, you have the option to source VCCH_GXB from the same regulator as VCCPT. All VCCH_GXB of all transceiver banks must be powered on for proper device operation except for the HF34 and NF40 packages of the Intel Arria 10 GX and GT devices. For the HF34 and NF40 packages of the Intel Arria 10 GX and GT devices, the VCCH_GXBR power rails can be tied to GND to save power if all of the transceivers, fPLLs, and IOPLLs on that side are not used. VCCH_GXB pins on the same side of the device must have the same voltage. Provide a minimum decoupling of 2.2nF for the VCCH_GXB power rail near the VCCH_GXB pin. To reduce voltage regulator module (VRM) switching noise impact on channel jitter performance, the VRM switching frequency for the VCCH_GXB rail should be below 2 MHz. For OTN application, the VRM switching frequency for the VCCH_GXB rail should be below 500 KHz. See Notes 2, 3, 4, 7, and 10.
GXB[L1,R4][C,D,E,F,G,H,I,J]_RX_[0:5]p, GXB[L,R][1][C,D,E,F,G,H,I,J]_REFCLK_CH[0:5]p	Input	High speed positive differential receiver channels. Specific to each transceiver bank of the left (L) side or right (R) side of the device.	These pins can be AC-coupled or DC-coupled when used. Connect all unused GXB_RXp pins directly to GND, VCCR_GXB, or VCCT_GXB pins.
GXB[L1,R4][C,D,E,F,G,H,I,J]_RX_[0:5]n, GXB[L,R][1][C,D,E,F,G,H,I,J]_REFCLK_CH[0:5]n	Input	High speed negative differential receiver channels. Specific to each transceiver bank of the left (L) side or right (R) side of the device.	These pins can be AC-coupled or DC-coupled when used. Connect all unused GXB_RXn pins directly to GND.
GXB[L1,R4][C,D,E,F,G,H,I,J]_TX_CH[0:5]p	Output	High speed positive differential transmitter channels. Specific to each transceiver bank of the left (L) side or right (R) side of the device.	Leave all unused GXB_TXp pins floating.
GXB[L1,R4][C,D,E,F,G,H,I,J]_TX_CH[0:5]n	Output	High speed negative differential transmitter channels. Specific to each transceiver bank of the left (L) side or right (R) side of the device.	Leave all unused GXB_TXn pins floating.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J]_CH[B,T]p	Input	High speed differential reference clock positive receiver channels, specific to each transceiver bank of the left (L) side or right (R) side of the device. REFCLK_GXB can be used as dedicated clock input pins with fPLL for core clock generation even when the transceiver channel is not available.	These pins must be AC-coupled if the selected REFCLK I/O standard is not HCSL. In the PCI Express configuration, DC-coupling is allowed on the REFCLK if the selected REFCLK I/O standard is HCSL. Connect all unused pins either individually to GND or tie all unused pins together through a single 10-kΩ resistor to GND. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 9.
REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J]_CH[B,T]n	Input	High speed differential reference clock complement, complementary receiver channel, specific to each transceiver bank of the left (L) side or right (R) side of the device. REFCLK_GXB can be used as dedicated clock input pins with fPLL for core clock generation even when the transceiver channel is not available.	These pins must be AC-coupled if the selected REFCLK I/O standard is not HCSL. In the PCI Express configuration, DC-coupling is allowed on the REFCLK if the selected REFCLK I/O standard is HCSL. Connect all unused pins either individually to GND or tie all unused pins together through a single 10-kΩ resistor to GND. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 9.
CLKUSR	I/O	This pin is used as the clock for transceiver calibration, and is a mandatory requirement when using transceivers. This pin is optionally used for EMIF HMC calibration, as well as a configuration clock input for synchronizing the initialization of more than one device. This is a user-supplied clock and the input frequency range must be in the range from 100 MHz to 125 MHz. This pin can be used as a GPIO pin only if you are not using transceivers, not using EMIF HMC, and not using this pin as a user-supplied configuration clock.	If you are using the CLKUSR pin for configuration and transceiver calibration, you must supply an external free running and stable clock to the CLKUSR pin at start of device configuration and also when the device entered user mode. If the clock is not present at device power-up, transceiver calibration will be delayed until the clock is available. This may impact protocol compliance. You need to ensure supplying the CLKUSR pin with a common clock frequency that is applicable for both the configuration mode and transceiver calibration.
			If you are not using the CLKUSR pin for configuration but using the CLKUSR pin for transceiver calibration, you must supply an external free running and stable clock to the CLKUSR pin at start of device configuration and also when the device entered user mode. If the clock is not present at device power-up, transceiver calibration will be delayed until the clock is available. This may impact protocol compliance.
			If you are using the CLKUSR pin for configuration but not using the CLKUSR pin for transceiver calibration, you must use a user-supplied clock input.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			For more information, refer to the *Configuration, Design Security, and Remote System Upgrades for Intel Arria 10 Devices* chapter.
			Connect the CLKUSR pin to GND if you are not using the CLKUSR pin for any of the following: • Configuration clock input • Transceiver calibration clock • An I/O pin
RREF_[T,B][L,R]	Input	Reference resistor for fPLL, IOPLL, and transceiver, specific to the top (T) side or bottom (B) side and left (L) side or right (R) side of the device.	If any REFCLK pin or transceiver channel on one side (left or right) of the device or IOPLL is used, you must connect each RREF pin on that side of the device to its own individual 2kΩ resistor to GND. Otherwise, you can connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Notes to Intel Arria 10 GX and GT Pin Connection Guidelines

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Arria 10 GX and GT device variants.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage drop requirements of the device/supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Arria 10 Early Power Estimator (EPE) to determine the current requirements for VCC and other power supplies. Use the Intel Quartus Prime PowerPlay Power Analyzer for the most accurate current requirements for this and other power supplies.

4. These supplies may share power planes across multiple Intel Arria 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
6. Example 1 through Example 7 and Figure 1 through Figure 7 illustrate the power supply sharing guidelines for the Intel Arria 10 GX and Intel Arria 10 GT devices. Example 11 illustrates the power supply sharing guidelines for Intel Arria 10 GX device using the SmartVID feature.
7. Low Noise Switching Regulator—defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response. The switching frequency range is not an Intel requirement. However, Intel does require the Line Regulation and Load Regulation meet the following specifications:
   - Line Regulation < 0.4%
   - Load Regulation < 1.2%
8. The number of modular I/O banks on Intel Arria 10 devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the *Intel Arria 10 Device Handbook*.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. Decoupling for these pins depends on the design decoupling requirements of the specific board.
11. Do not connect voltage above 1.8V to the VREFB[[2][A, F,G,H,I,J,K, L], [3] [A, B,C,D,E,F,G, H]]N0 pins. For 3V I/O banks, tie unused VREF pins to GND.
12. Do not drive the I/O pins externally during the power-up and power-down time to avoid excess current on the I/O pins:
    - Excess I/O pin current affects the device's lifetime and reliability.
    - Excess current on the 3V I/O pins can damage the Intel Arria 10 device.

    For the acceptable limits on the input current, refer to the Absolute Maximum Ratings section in the *Intel Arria 10 Device Datasheet*.

Related Information

Absolute Maximum Ratings

Intel Arria 10 SX Pin Connection Guidelines

HPS Supply Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 11. HPS Supply Pins

HPS Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCL_HPS	Power	VCCL_HPS supplies power to the HPS core.	Connect all VCCL_HPS pins to a 0.9V or 0.95V low noise switching regulator. For more information about the voltage requirements for various operating temperatures and speed grades, refer to the Maximum HPS Clock Frequencies Across Device Speed Grade for Intel Arria 10 Devices table in the *Intel Arria 10 Device Datasheet*. Use the Intel Arria 10 Early Power Estimator (EPE) to determine the current requirements for VCCL_HPS and other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 6.
VCCIO_HPS	Power	HPS dedicated I/Os can support a different voltage level from 1.8V to 3.0V. The supported I/O standard is LVTTL/ LVCMOS (3.0, 2.5, 1.8).	Connect these pins to a 1.8V, 2.5V, or 3.0V power supply, depending on the I/O standard required by the specified bank. If these pins have the same voltage requirement as VCCIO and VCCPGM, you have the option to source VCCIO_HPS pins from the same regulator as VCCIO and VCCPGM. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8.
VCCPLL_HPS	Power	VCCPLL_HPS supplies analog power to the HPS core PLLs.	Connect these pins to a 1.8V low noise switching power supply through a proper isolation filter. Share VCCPLL_HPS with the same regulator as VCCPT when all power rails require 1.8V but only with a proper isolation filter.

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HPS Pin Name	Pin Functions	Pin Description	Connection Guidelines
			Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCIOREF_HPS	Power	HPS power supply for I/O pre-drivers.	The VCCIOREF_HPS pins require 1.8V. When these pins have the same voltage requirements as VCCIO_HPS, you have the option to tie them to the same regulator. If these pins have the same voltage requirement as VCCPT, you have the option to tie them to the same regulator. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8.

HPS Dedicated I/O Bank Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 12. HPS Dedicated I/O Bank Pins

HPS Pin Name	Pin Functions	Pin Description	Connection Guidelines
HPS_CLK1	Input, Clock	Dedicated clock input pin that drives the main PLL. This provides clocks to the MPU, L3/L4 sub-systems, debug sub-system and the Flash controllers. It can also be programmed to drive the peripherals.	Connect a single-ended clock source to this pin. The I/O standard of the clock source must be compatible with VCCIO_HPS. Refer to the valid frequency range of the clock source in the *Intel Arria 10 Device Datasheet*. Unless the hps_clk_f fuse is blown, an input clock must be present on this pin for the HPS to boot properly.
HPS_ nRST	Bidirectional	Warm reset to the HPS block. Active low bi-directional pin. When driven from the board, the system reset domains that allow debugging to operate are affected. Any cold HPS reset drives the HPS_nRST pin low. HPS_nRST may be driven low on a warm reset if enabled using the nrstwarmmask register in the Reset Manager.	Connect this pin through a 1-kΩ pull-up resistor to VCCIO_HPS.
HPS_ nPOR	Input	Cold reset to the HPS block. Active low input that resets all HPS logic that can be reset. Places the HPS in a default state sufficient for the software to boot. This pin has an internal 25-kΩ pull-up resistor that is always active.	Connect this pin through a 1–10-kΩ pull-up resistor to VCCIO_HPS.

HPS Peripheral Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 13. HPS Peripheral Pins

HPS Pin Name	Pin Type	Pin Functions See Notes 11, 12, and 13.	Pin Description	Connection Guidelines
HPS_DEDICATED_4	I/O	Pin Mux Select 4	QSPI CLK	When configured as the QSPI Clock and if a single memory topology is used, connect a 50-Ω series termination resistor near this Intel Arria 10 SoC FPGA device pin. For other topologies, use a 25-Ω series termination resistor. When you are booting the HPS from a SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	SDMMC Data Bit 0	
		Pin Mux Select 14	NAND Data Bit 0	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 0	
HPS_DEDICATED_5	I/O	Pin Mux Select 4	QSPI Data IO Bit 0	When you are booting the HPS from a SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	SDMMC Command Line	
		Pin Mux Select 14	NAND Data Bit 1	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 1	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 11, 12, and 13.	Pin Description	Connection Guidelines
BOOTSEL2 (BSEL2)/ HPS_DEDICATED_6	I/O	Pin Mux Select 4	QSPI Slave Select 0	Connect a 4.7-kΩ pull-up or pull-down resistor to the pin to select the desired boot select values. For more information about the boot select values, refer to the Booting and Configuration appendix in the *Intel Arria 10 Hard Processor System Technical Reference Manual*. This is a multi-function pin. The HPS Boot ROM samples the value of the BSEL from this pin upon power up. After boot up, the function of this pin will be according to the settings in the Platform Designer. This resistor will not interfere with the slow speed interface signals that could share this pin.
		Pin Mux Select 8	SDMMC Clock Out	
		Pin Mux Select 14	NAND Write Enable See Note 19.	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 2	
HPS_DEDICATED_7	I/O	Pin Mux Select 4	QSPI Data IO Bit 1	When you are booting the HPS from a SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	SDMMC Data Bit 1	
		Pin Mux Select 14	NAND Read Enable See Note 19.	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 3	
HPS_DEDICATED_8	I/O	Pin Mux Select 4	QSPI Data IO Bit 2/ Write Protect See Note 19.	When you are booting the HPS from a SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	SDMMC Data Bit 2	
		Pin Mux Select 14	NAND Data Bit 2	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 4	

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HPS Pin Name	Pin Type	Pin Functions See Notes 11, 12, and 13.	Pin Description	Connection Guidelines
HPS_DEDICATED_9	I/O	Pin Mux Select 4	QSPI Data IO Bit 3/ Hold	When you are booting the HPS from a SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. The SD card has an internal pull-up on the SDMMC Data Bit 3 which can be disabled in the software using the SET_CLR_CARD_DETECT (ACMD42) command. This is not applicable for the MMC/eMMC flash. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	SDMMC Data Bit 3	
		Pin Mux Select 14	NAND Data Bit 3	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 5	
BOOTSEL1 (BSEL1)/ HPS_DEDICATED_10	I/O	Pin Mux Select 2	SPIS0 Master In Slave Out	Connect a 4.7-kΩ pull-up or pull-down resistor to the pin to select the desired boot select values. For more information about the boot select values, refer to the Booting and Configuration appendix in the *Intel Arria 10 Hard Processor System Technical Reference Manual*. This is a multi-function pin. The HPS Boot ROM samples the value of the BSEL from this pin upon power up. After boot up, the function of this pin will be according to the settings in the Platform Designer. This resistor will not interfere with the slow speed interface signals that could share this pin.
		Pin Mux Select 3	SPIM0 Slave Select 1 See Note 19.	
		Pin Mux Select 8	SDMMC Power Enable See Note 15.	
		Pin Mux Select 14	NAND Command Latch Enable	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 6	
BOOTSEL0 (BSEL0)/ HPS_DEDICATED_11	I/O	Pin Mux Select 3	SPIM 0 Clock	Connect a 4.7-kΩ pull-up or pull-down resistor to the pin to select the desired boot select values. For more information about the boot select values, refer to the Booting and Configuration appendix in the *Intel Arria 10 Hard Processor System Technical Reference Manual*. This is a multi-function pin. The HPS Boot ROM samples the value of the BSEL from this pin upon power up. After boot up, the function of this pin will be according to the settings in the Platform Designer.
		Pin Mux Select 4	PLL Clock 0	
		Pin Mux Select 8	QSPI Slave Select 1	
		Pin Mux Select 14	NAND Address Latch Enable	

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HPS Pin Name	Pin Type	Pin Functions See Notes 11, 12, and 13.	Pin Description	Connection Guidelines
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 7	This resistor will not interfere with the slow speed interface signals that could share this pin.
HPS_DEDICATED_12	I/O	Pin Mux Select 0	I2C EMAC1 Serial Data	If used as the NAND Ready/Busy input, connect this pin through a 1–10-kΩ pull-up resistor to VCCIO_HPS in the dedicated I/O bank which the NAND_RB pin resides. When you are booting the HPS from a MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC1 MDIO	
		Pin Mux Select 3	SPIM0 Master Out Slave In	
		Pin Mux Select 4	PLL Clock 1	
		Pin Mux Select 8	SDMMC Data Bit 4	
		Pin Mux Select 13	UART1 Transmit	
		Pin Mux Select 14	NAND Ready/Busy	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 8	
HPS_DEDICATED_13	I/O	Pin Mux Select 0	I2C EMAC1 Serial Clock	When you are booting the HPS from a MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC1 MDC	
		Pin Mux Select 3	SPIM0 Master In Slave Out	
		Pin Mux Select 4	PLL Clock 2	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 11, 12, and 13.	Pin Description	Connection Guidelines
		Pin Mux Select 8	SDMMC Data Bit 5	
		Pin Mux Select 13	UART1 Request to Send See Note 19.	
		Pin Mux Select 14	NAND Chip Enable See Note 19.	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 9	
HPS_DEDICATED_14	I/O	Pin Mux Select 0	I2C EMAC2 Serial Data	When you are booting the HPS from a MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC2 MDIO	
		Pin Mux Select 3	SPIM0 Slave Select 0 See Note 19.	
		Pin Mux Select 4	PLL Clock 3	
		Pin Mux Select 8	SDMMC Data Bit 6	
		Pin Mux Select 13	UART1 Clear to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 4	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 10	

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HPS Pin Name	Pin Type	Pin Functions See Notes 11, 12, and 13.	Pin Description	Connection Guidelines
HPS_DEDICATED_15	I/O	Pin Mux Select 0	I2C EMAC2 Serial Clock	When you are booting the HPS from a MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC2 MDC	
		Pin Mux Select 2	SPIS0 Clock	
		Pin Mux Select 4	PLL Clock 4	
		Pin Mux Select 8	SDMMC Data Bit 7	
		Pin Mux Select 13	UART1 Receive	
		Pin Mux Select 14	NAND Data Bit 5	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 11	
HPS_DEDICATED_16	I/O	Pin Mux Select 0	I2C EMAC0 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC0 MDIO	
		Pin Mux Select 2	SPIS0 Master Out Slave In	
		Pin Mux Select 8	QSPI Slave Select 2	
		Pin Mux Select 13	UART1 Transmit	
		Pin Mux Select 14	NAND Data Bit 6	

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HPS Pin Name	Pin Type	Pin Functions See Notes 11, 12, and 13.	Pin Description	Connection Guidelines
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 12	
HPS_DEDICATED_17	I/O	Pin Mux Select 0	I2C EMAC0 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC0 MDC	
		Pin Mux Select 2	SPIS0 Slave Select 0 See Note 19.	
		Pin Mux Select 8	QSPI Slave Select 3	
		Pin Mux Select 13	UART1 Receive	
		Pin Mux Select 14	NAND Data Bit 7	
		Pin Mux Select 15 See Note 14.	GPIO 2 Bit 13	

Shared 3V I/O Bank Pins

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 14. Shared 3V I/O Bank Pins

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
HPS_Shared_Q1_1	I/O	Pin Mux Select 2	SPIS0 Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 3	SPIM0 Slave Select 1 See Note 19.	
		Pin Mux Select 4	SDMMC Data Bit 0	
		Pin Mux Select 8	USB0 Clock	
		Pin Mux Select 13	UART0 Clear to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 0	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 0	
HPS_Shared_Q1_2	I/O	Pin Mux Select 2	SPIS 0 Master Out Slave In	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 3	SPIM 1 Slave Select 1 See Note 19.	
		Pin Mux Select 4	SDMMC Command Line	
		Pin Mux Select 8	USB 0 Stop Data	
		Pin Mux Select 13	UART 0 Request to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 1	
		Pin Mux Select 15	GPIO 0 Bit 1	

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HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		See Note 18.		
HPS_Shared_Q1_3	I/O	Pin Mux Select 0	I2C 1 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS 0 Slave Select 0 See Note 19.	
		Pin Mux Select 4	SDMMC Clock Out	
		Pin Mux Select 8	USB 0 Direction	
		Pin Mux Select 13	UART 0 Transmit	
		Pin Mux Select 14	NAND Write Enable See Note 19.	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 2	
HPS_Shared_Q1_4	I/O	Pin Mux Select 0	I2C 1 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 2	SPIS 0 Master In Slave Out	
		Pin Mux Select 4	SDMMC Data Bit 1	
		Pin Mux Select 8	USB 0 Data Bit 0	
		Pin Mux Select 13	UART 0 Receive	
		Pin Mux Select 14	NAND Read Enable See Note 19.	
		Pin Mux Select 15	GPIO 0 Bit 3	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		See Note 18.		
HPS_Shared_Q1_5	I/O	Pin Mux Select 0	I2C 0 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 3	SPIM 0 Clock	
		Pin Mux Select 4	SDMMC Data Bit 2	
		Pin Mux Select 8	USB0 Data Bit 1	
		Pin Mux Select 12	QSPI Slave Select 2	
		Pin Mux Select 13	UART 1 Clear to Send See Note 19.	
		Pin Mux Select 14	NAND Write Protect See Note 19.	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 4	
HPS_Shared_Q1_6	I/O	Pin Mux Select 0	I2C 0 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the SD/MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ. The SD card has an internal pull-up on the SDMMC Data Bit 3 that can be disabled in the software using the SET_CLR_CARD_DETECT (ACMD42) command. This is not applicable for the MMC/eMMC flash.
		Pin Mux Select 3	SPIM 0 Master Out Slave In	
		Pin Mux Select 4	SDMMC Data Bit 3	
		Pin Mux Select 8	USB 0 Next Data	
		Pin Mux Select 12	QSPI Slave Select 3	
		Pin Mux Select 13	UART 1 Request to Send See Note 19.	

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HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 14	NAND Data Bit 2	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 5	
HPS_Shared_Q1_7	I/O	Pin Mux Select 0	I2C EMAC 2 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 1	EMAC 2 MDIO	
		Pin Mux Select 3	SPIM 0 Master In SlaveOut	
		Pin Mux Select 4	SDMMC Data Bit 4	
		Pin Mux Select 8	USB0 Data Bit 2	
		Pin Mux Select 13	UART 1 Transmit	
		Pin Mux Select 14	NAND Data Bit 3	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 6	
HPS_Shared_Q1_8	I/O	Pin Mux Select 0	I2C EMAC 2 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 1	EMAC 2 MDC	
		Pin Mux Select 3	SPIM 0 Slave Select 0 See Note 19.	
		Pin Mux Select 4	SDMMC Data Bit 5	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 8	USB 0 Data Bit 3	
		Pin Mux Select 13	UART 1 Receive	
		Pin Mux Select 14	NAND Command Latch Enable	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 7	
HPS_Shared_Q1_9	I/O	Pin Mux Select 0	I2C EMAC 1 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 1	EMAC 1 MDIO	
		Pin Mux Select 2	SPIS 1 Clock	
		Pin Mux Select 3	SPIM 1 Clock	
		Pin Mux Select 4	SDMMC Data Bit 6	
		Pin Mux Select 8	USB 0 Data Bit 4	
		Pin Mux Select 14	NAND Data Bit 4	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 8	
HPS_Shared_Q1_10	I/O	Pin Mux Select 0	I2C EMAC 1 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 1	EMAC 1 MDC	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 2	SPIS 1 Master Out Slave In	
		Pin Mux Select 3	SPIM 1 Master Out Slave In	
		Pin Mux Select 4	SDMMC Data Bit 7	
		Pin Mux Select 8	USB 0 Data Bit 5	
		Pin Mux Select 14	NAND Data Bit 5	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 9	
HPS_Shared_Q1_11	I/O	Pin Mux Select 0	I2C EMAC 0 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin for the MMC/eMMC device, pull this pin high on the board with a weak pull-up resistor such as 10-kΩ.
		Pin Mux Select 1	EMAC 0 MDIO	
		Pin Mux Select 2	SPIS 1 Slave Select 0 See Note 19.	
		Pin Mux Select 3	SPIM 1 Master In Slave Out	
		Pin Mux Select 8	USB 0 Data Bit 6	
		Pin Mux Select 14	NAND Data Bit 6	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 10	
HPS_Shared_Q1_12	I/O	Pin Mux Select 0	I2C EMAC 0 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.

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HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 1	EMAC 0 MDC	
		Pin Mux Select 2	SPIS 1 Master In Slave Out	
		Pin Mux Select 3	SPIM 1 Slave Select 0 See Note 19.	
		Pin Mux Select 8	USB 0 Data Bit 7	
		Pin Mux Select 14	NAND Data Bit 7	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 11	
HPS_Shared_Q2_1	I/O	Pin Mux Select 4	EMAC 0 Transmit Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	USB 1 Clock	
		Pin Mux Select 14	NAND Address Latch Enable	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 12	
HPS_Shared_Q2_2	I/O	Pin Mux Select 4	EMAC 0 Transmit Control	If used as the NAND Ready/Busy input, connect this pin through a 1–10-kΩ pull-up resistor to VCCIO_2L in the dedicated I/O bank which the NAND_RB pin resides. If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	USB 1 Stop Data	
		Pin Mux Select 14	NAND Ready/Busy	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 13	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
HPS_Shared_Q2_3	I/O	Pin Mux Select 4	EMAC 0 Receive Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	USB 1 Direction	
		Pin Mux Select 14	NAND Chip Enable See Note 19.	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 14	
HPS_Shared_Q2_4	I/O	Pin Mux Select 4	EMAC 0 Receive Control	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	USB 1 Data Bit 0	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 15	
HPS_Shared_Q2_5	I/O	Pin Mux Select 4	EMAC 0 Transmit Data Bit 0	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	USB 1 Data Bit 1	
		Pin Mux Select 14	NAND Data Bit 8	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 16	
HPS_Shared_Q2_6	I/O	Pin Mux Select 4	EMAC 0 Transmit Data Bit 1	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	USB 1 Next Data	
		Pin Mux Select 14	NAND Data Bit 9	

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HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 17	
HPS_Shared_Q2_7	I/O	Pin Mux Select 4	EMAC0 Receive Data Bit 0	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	USB1 Data Bit 2	
		Pin Mux Select 14	NAND Data Bit 10	
		Pin Mux Select 15 See Note 18.	GPIO0 Bit 18	
HPS_Shared_Q2_8	I/O	Pin Mux Select 3	SPIM 1 Slave Select 1 See Note 19.	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 4	EMAC 0 Receive Data Bit 1	
		Pin Mux Select 8	USB 1 Data Bit 3	
		Pin Mux Select 14	NAND Data Bit 11	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 19	
HPS_Shared_Q2_9	I/O	Pin Mux Select 0	I2C 1 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS 0 Clock	
		Pin Mux Select 3	SPIM 1 Clock	
		Pin Mux Select 4	EMAC 0 Transmit Data Bit 2	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 8	USB 1 Data Bit 4	
		Pin Mux Select 13	UART 0 Clear to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 12	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 20	
HPS_Shared_Q2_10	I/O	Pin Mux Select 0	I2C 1 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS 0 Master Out Slave In	
		Pin Mux Select 3	SPIM 1 Master Out Slave In	
		Pin Mux Select 4	EMAC 0 Transmit Data Bit 3	
		Pin Mux Select 8	USB 1 Data Bit 5	
		Pin Mux Select 13	UART 0 Request to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 13	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 21	
HPS_Shared_Q2_11	I/O	Pin Mux Select 0	I2C 0 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS 0 Slave Select 0 See Note 19.	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 3	SPIM 1 Master In Slave Out	
		Pin Mux Select 4	EMAC 0 Receive Data Bit 2	
		Pin Mux Select 8	USB 1 Data Bit 6	
		Pin Mux Select 13	UART 0 Transmit	
		Pin Mux Select 14	NAND Data Bit 14	
		Pin Mux Select 15 See Note 18.	GPIO 0 Bit 22	
HPS_Shared_Q2_12	I/O	Pin Mux Select 0	I2C0 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS0 Master In Slave Out	
		Pin Mux Select 3	SPIM1 Slave Select 0 See Note 19.	
		Pin Mux Select 4	EMAC0 Receive Data Bit 3	
		Pin Mux Select 8	USB1 Data Bit 7	
		Pin Mux Select 13	UART0 Receive	
		Pin Mux Select 14	NAND Data Bit 15	
		Pin Mux Select 15 See Note 18.	GPIO0 Bit 23	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
HPS_Shared_Q3_1	I/O	Pin Mux Select 3	SPIM 1 Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	EMAC 1 Transmit Clock	
		Pin Mux Select 13	UART 0 Clear to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 0	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 0	
HPS_Shared_Q3_2	I/O	Pin Mux Select 3	SPIM 1 Master Out Slave In	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	EMAC 1 Transmit Control	
		Pin Mux Select 13	UART 0 Request to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 1	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 1	
HPS_Shared_Q3_3	I/O	Pin Mux Select 0	I2C0 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 3	SPIM1 Master In Slave Out	
		Pin Mux Select 8	EMAC1 Receive Clock	
		Pin Mux Select 13	UART0 Transmit	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 14	NAND Write Enable See Note 19.	
		Pin Mux Select 15 See Note 18.	GPIO1 Bit 2	
HPS_Shared_Q3_4	I/O	Pin Mux Select 0	I2C 0 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 3	SPIM 1 Slave Select 0 See Note 19.	
		Pin Mux Select 8	EMAC 1 Receive Control	
		Pin Mux Select 13	UART 0 Receive	
		Pin Mux Select 14	NAND Read Enable See Note 19.	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 3	
HPS_Shared_Q3_5	I/O	Pin Mux Select 2	SPIS 1 Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 3	SPIM 1 Slave Select 1 See Note 19.	
		Pin Mux Select 8	EMAC 1 Transmit Data Bit 0	
		Pin Mux Select 13	UART 1 Clear to Send See Note 19.	
		Pin Mux Select 14	NAND Write Protect See Note 19.	
		Pin Mux Select 15	GPIO 1 Bit 4	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		See Note 18.		
HPS_Shared_Q3_6	I/O	Pin Mux Select 2	SPIS 1 Master Out Slave In	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	EMAC 1 Transmit Data Bit 1	
		Pin Mux Select 13	UART 1 Request to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 2	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 5	
HPS_Shared_Q3_7	I/O	Pin Mux Select 0	I2C 1 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS 1 Slave Select 0 See Note 19.	
		Pin Mux Select 8	EMAC 1 Receive Data Bit 0	
		Pin Mux Select 13	UART 1 Transmit	
		Pin Mux Select 14	NAND Data Bit 3	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 6	
HPS_Shared_Q3_8	I/O	Pin Mux Select 0	I2C 1 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS 1 Master In Slave Out	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 8	EMAC 1 Receive Data Bit 1	
		Pin Mux Select 13	UART 1 Receive	
		Pin Mux Select 14	NAND Command Latch Enable	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 7	
HPS_Shared_Q3_9	I/O	Pin Mux Select 0	I2C EMAC 2 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC 2 MDIO	
		Pin Mux Select 2	SPIS 0 Clock	
		Pin Mux Select 8	EMAC 1 Transmit Data Bit 2	
		Pin Mux Select 14	NAND Data Bit 4	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 8	
HPS_Shared_Q3_10	I/O	Pin Mux Select 0	I2C EMAC 2 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC 2 MDC	
		Pin Mux Select 2	SPIS 0 Master Out Slave In	
		Pin Mux Select 8	EMAC 1 Transmit Data Bit 3	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 14	NAND Data Bit 5	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 9	
HPS_Shared_Q3_11	I/O	Pin Mux Select 0	I2C EMAC 0 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC 0 MDIO	
		Pin Mux Select 2	SPIS 0 Slave Select 0 See Note 19.	
		Pin Mux Select 8	EMAC 1 Receive Data Bit 2	
		Pin Mux Select 14	NAND Data Bit 6	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 10	
HPS_Shared_Q3_12	I/O	Pin Mux Select 0	I2C EMAC 0 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC 0 MDC	
		Pin Mux Select 2	SPIS 0 Master In Slave Out	
		Pin Mux Select 8	EMAC 1 Receive Data Bit 3	
		Pin Mux Select 14	NAND Data Bit 7	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 11	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
HPS_Shared_Q4_1	I/O	Pin Mux Select 0	I2C 1 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 4	SDMMC Data Bit 0	
		Pin Mux Select 8	EMAC 2 Transmit Clock	
		Pin Mux Select 14	NAND Address Latch Enable	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 12	
HPS_Shared_Q4_2	I/O	Pin Mux Select 0	I2C 1 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up. When you are using this pin as the NAND Ready/ Busy input, connect this pin through a 1–10-kΩ pull-up resistor to the VCCIO_2L in the dedicated I/O bank which the NAND_RB pin resides.
		Pin Mux Select 4	SDMMC Command Line	
		Pin Mux Select 8	EMAC 2 Transmit Control	
		Pin Mux Select 14	NAND Ready/ Busy	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 13	
HPS_Shared_Q4_3	I/O	Pin Mux Select 4	SDMMC Clock Out	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	EMAC 2 Receive Clock	
		Pin Mux Select 13	UART 1 Transmit	
		Pin Mux Select 14	NAND Chip Enable See Note 19.	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 14	
HPS_Shared_Q4_4	I/O	Pin Mux Select 4	SDMMC Data Bit 1	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	EMAC 2 Receive Control	
		Pin Mux Select 12	Trace clock	
		Pin Mux Select 13	UART 1 Receive	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 15	
HPS_Shared_Q4_5	I/O	Pin Mux Select 4	SDMMC Data Bit 2	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 8	EMAC 2 Transmit Data Bit 0	
		Pin Mux Select 12	QSPI Slave Select 2	
		Pin Mux Select 13	UART 1 Clear to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 8	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 16	
HPS_Shared_Q4_6	I/O	Pin Mux Select 3	SPIM 0 Slave Select 1 See Note 19.	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 4	SDMMC Data Bit 3	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 8	EMAC 2 Transmit Data Bit 1	
		Pin Mux Select 12	QSPI Slave Select 3	
		Pin Mux Select 13	UART 1 Request to Send See Note 19.	
		Pin Mux Select 14	NAND Data Bit 9	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 17	
HPS_Shared_Q4_7	I/O	Pin Mux Select 0	I2C EMAC 1 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC 1 MDIO	
		Pin Mux Select 3	SPIM 0 Master In Slave Out	
		Pin Mux Select 4	SDMMC Data Bit 4	
		Pin Mux Select 8	EMAC 2 Receive Data Bit 0	
		Pin Mux Select 14	NAND Data Bit 10	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 18	
HPS_Shared_Q4_8	I/O	Pin Mux Select 0	I2C EMAC 1 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC 1 MDC	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 3	SPIM 0 Slave Select 0 See Note 19.	
		Pin Mux Select 4	SDMMC Data Bit 5	
		Pin Mux Select 8	EMAC 2 Receive Data Bit 1	
		Pin Mux Select 13	Trace Clock	
		Pin Mux Select 14	NAND Data Bit 11	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 19	
HPS_Shared_Q4_9	I/O	Pin Mux Select 0	I2C EMAC 2 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS 1 Clock	
		Pin Mux Select 3	SPIM 0 Clock	
		Pin Mux Select 4	SDMMC Data Bit 6	
		Pin Mux Select 8	EMAC 2 Transmit Data Bit 2	
		Pin Mux Select 12	Trace Data 0	
		Pin Mux Select 14	NAND Data Bit 12	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 20	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
HPS_Shared_Q4_10	I/O	Pin Mux Select 0	I2C EMAC 2 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 2	SPIS 1 Master Out Slave In	
		Pin Mux Select 3	SPIM 0 Master Out Slave In	
		Pin Mux Select 4	SDMMC Data Bit 7	
		Pin Mux Select 8	EMAC 2 Transmit Data Bit 3	
		Pin Mux Select 12	Trace Data 1	
		Pin Mux Select 14	NAND Data Bit 13	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 21	
HPS_Shared_Q4_11	I/O	Pin Mux Select 0	I2C EMAC 0 Serial Data	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC 0 MDIO	
		Pin Mux Select 2	SPIS 1 Slave Select 0 See Note 19.	
		Pin Mux Select 3	SPIM 0 Master In Slave Out	
		Pin Mux Select 8	EMAC 2 Receive Data Bit 2	
		Pin Mux Select 12	Trace Data 2	
		Pin Mux Select 14	NAND Data Bit 14	

continued...

HPS Pin Name	Pin Type	Pin Functions See Notes 16 and 17.	Pin Description	Connection Guidelines
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 22	
HPS_Shared_Q4_12	I/O	Pin Mux Select 0	I2C EMAC 0 Serial Clock	If unused, program it in the Intel Quartus Prime software as an input with a weak pull-up.
		Pin Mux Select 1	EMAC 0 MDC	
		Pin Mux Select 2	SPIS 1 Master In Slave Out	
		Pin Mux Select 3	SPIM 0 Slave Select 0 See Note 19.	
		Pin Mux Select 8	EMAC 2 Receive Data Bit 3	
		Pin Mux Select 12	Trace Data 3	
		Pin Mux Select 14	NAND Data Bit 15	
		Pin Mux Select 15 See Note 18.	GPIO 1 Bit 23	

Notes to Intel Arria 10 SX Pin Connection Guidelines

Note: Intel recommends that you create a Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are based on the Intel Arria 10 SX device variant.
2. Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage drop requirements of the device/supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Arria 10 Early Power Estimator (EPE) to determine the current requirements for VCC and other power supplies. Use the Intel Quartus Prime PowerPlay Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Arria 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA must have its own dedicated breakout via.
6. Example 8, Example 9, Example 10, Figure 8, Figure 9, and Figure 10 illustrate the power supply sharing guidelines for the Intel Arria 10 SX devices.
7. Low Noise Switching Regulator—a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response. The switching frequency range is not an Intel requirement. However, Intel does require the Line Regulation and Load Regulation meet the following specifications:
   - Line Regulation < 0.4%
   - Load Regulation < 1.2%
8. The number of modular I/O banks on Intel Arria 10 devices depends on the device density. For the indexes available for a specific device, refer to the I/O Bank section in the *Intel Arria 10 Device Handbook*.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires that the AC-coupling capacitor is placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. For item [#], refer to the device pin table for the pin-out mapping.
11. The peripheral pins are programmable through pin multiplexors. Each pin may have multiple functions. The HPS dedicated I/O pin multiplexing is programmable using the HPS software. The pin mux will determine how the pins are used.
12. Pin Mux Select 5, 6, 7, 9, 10, 11, and 12 will not assign any HPS dedicated pins to any specific function. Pin Mux Select 5, 6, 7, 9, 10, 11, and 12 are not listed in the HPS Peripheral Pins table.

13. A warm reset event will not change the configured value of the HPS dedicated I/O Pin Mux.
14. At cold reset, these pins will default to the GPIO and BSEL functions set.
15. SD/MMC Power Enable pins are inverted. For details, refer to the *Intel Arria 10 SoC Errata Sheet*.
16. Pin Mux Select 5, 6, 7, 9, 10, and 11 will not assign any HPS dedicated pins to any specific function. Pin Mux Select 5, 6, 7, 9, 10, and 11 are not listed in the Shared 3V I/O Bank Pins table.
17. A warm reset event will not change the configured value of the HPS shared I/O Pin Mux.
18. At cold reset, these pins will default to the GPIO function set.
19. These pins are inverted or active-low signals.
20. Do not drive the I/O pins externally during the power-up and power-down time to avoid excess current on the I/O pins:
    - Excess I/O pin current affects the device's lifetime and reliability.
    - Excess current on the 3V I/O pins can damage the Intel Arria 10 device.

    For the acceptable limits on the input current, refer to the Absolute Maximum Ratings section in the *Intel Arria 10 Device Datasheet*.

Related Information

Absolute Maximum Ratings

Power Supply Sharing Guidelines for Intel Arria 10 Devices

Example 1—Intel Arria 10 GX

Table 15. Power Supply Sharing Guidelines for Intel Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications

Example Requiring 3 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9	±30 mV	Switcher (*)	Share	You have the option to source VCC and VCCP from the same regulator as VCCERAM when all the power rails require the same voltage level. When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not
VCCP						
VCCERAM						

continued...

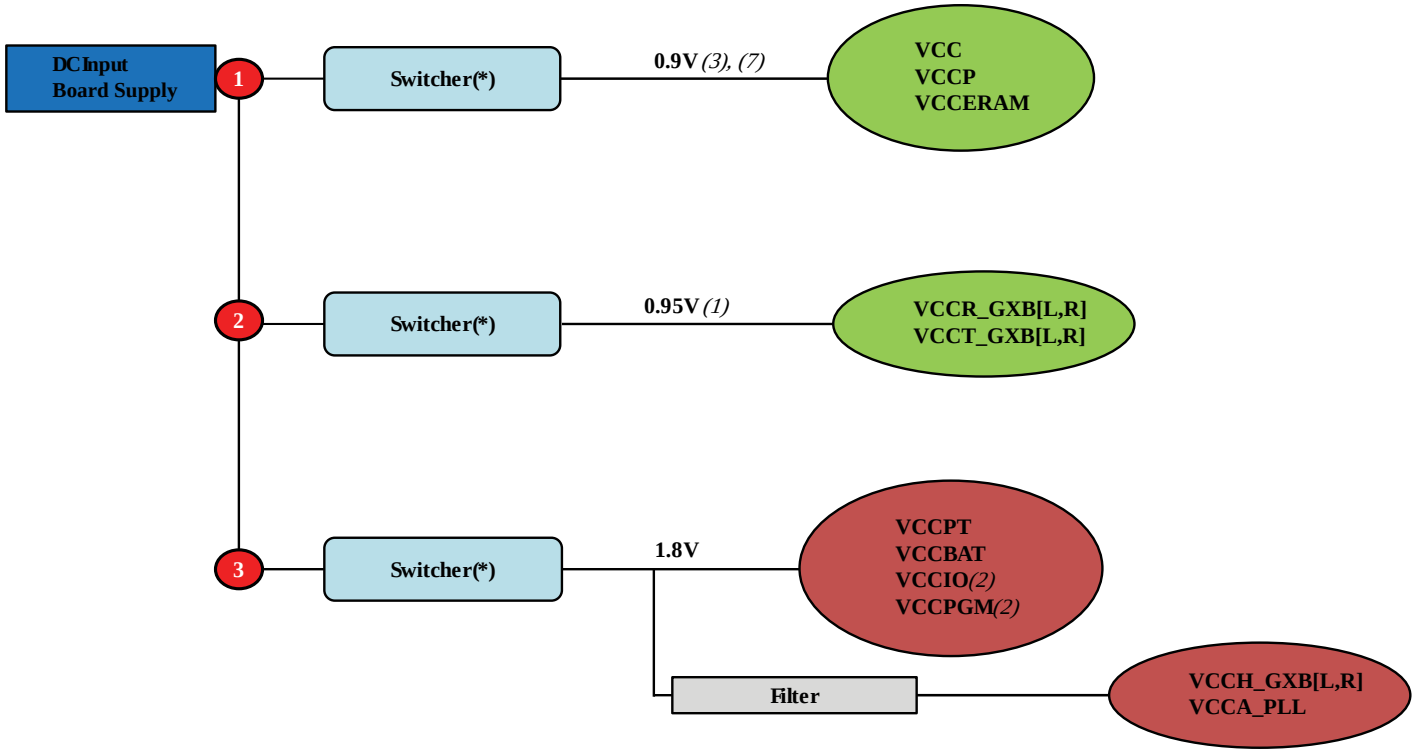
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCR_GXB[L,R] VCCT_GXB[L,R]	2	0.95	±30 mV	Switcher (*)	Share	For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. VCCR_GXB and VCCT_GXB must be 1.03V or higher in order to support PCIe Gen 3. To meet DisplayPort TX electrical full compliance, V_{CCT_GXB} must be 1.03V or higher. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCBAT	3	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, and VCCPGM to share the same regulator when all power rails required 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 GX device is provided in Figure 1.

Figure 1. Example Power Supply Sharing Guidelines for Intel Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications—



Example 2—Intel Arria 10 GX

Table 16. Power Supply Sharing Guidelines for Intel Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications

Example Requiring 2 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCP VCCERAM	1	0.95	±30 mV	Switcher(*)	Share	You have the option to source VCC and VCCP from the same regulator as VCCERAM when all the power rails require the same voltage level. When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCR_GXB[L,R] VCCT_GXB[L,R]					Isolate	Option provided to share VCCR_GXB and VCCT_GXB with the same regulator as VCC, VCCP, and VCCERAM when all power rails require 0.95V with proper isolation filter. For details, refer to note 1 of the *Notes to Power Supply Sharing Guidelines*. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. VCCR_GXB and VCCT_GXB must be 1.03V or higher in order to support PCIe Gen 3. To meet DisplayPort TX electrical full compliance, $_{VCCT\_GXB}$ must be 1.03V or higher. When implementing a filtered supply topology, you must consider the IR drop across the filter. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.

continued...

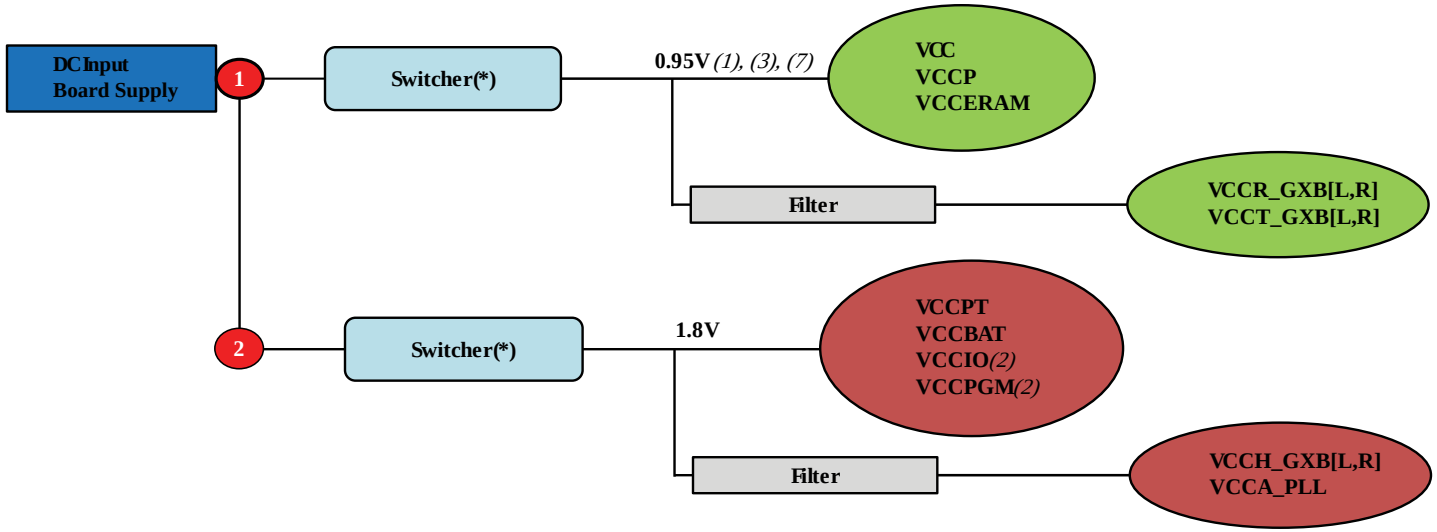
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCBAT	2	Varies	± 5% (**)	Switcher(*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, and VCCPGM to share the same regulator when all power rails required 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 GX device is provided in Figure 2.

Figure 2. Example Power Supply Sharing Guidelines for Intel Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications



Example 3—Intel Arria 10 GX

Table 17. Power Supply Sharing Guidelines for Intel Arria 10 GX with Transceiver Data Rate <= 17.4 Gbps(**) for Chip-to-Chip Applications (Transceiver Data Rate <= 12.5 Gbps (**) for Backplane Applications)

Example Requiring 3 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9/0.95	±30 mV	Switcher(*)	Share	VCC, VCCP, and VCCERAM support 0.9V and 0.95V. You have the option to source VCC and VCCP from the same regulator as VCCERAM when all the power rails require the same voltage level. For more details, refer to the Electrical Specifications in the *Intel Arria 10 Device Datasheet*.
VCCP						
VCCERAM						

continued...

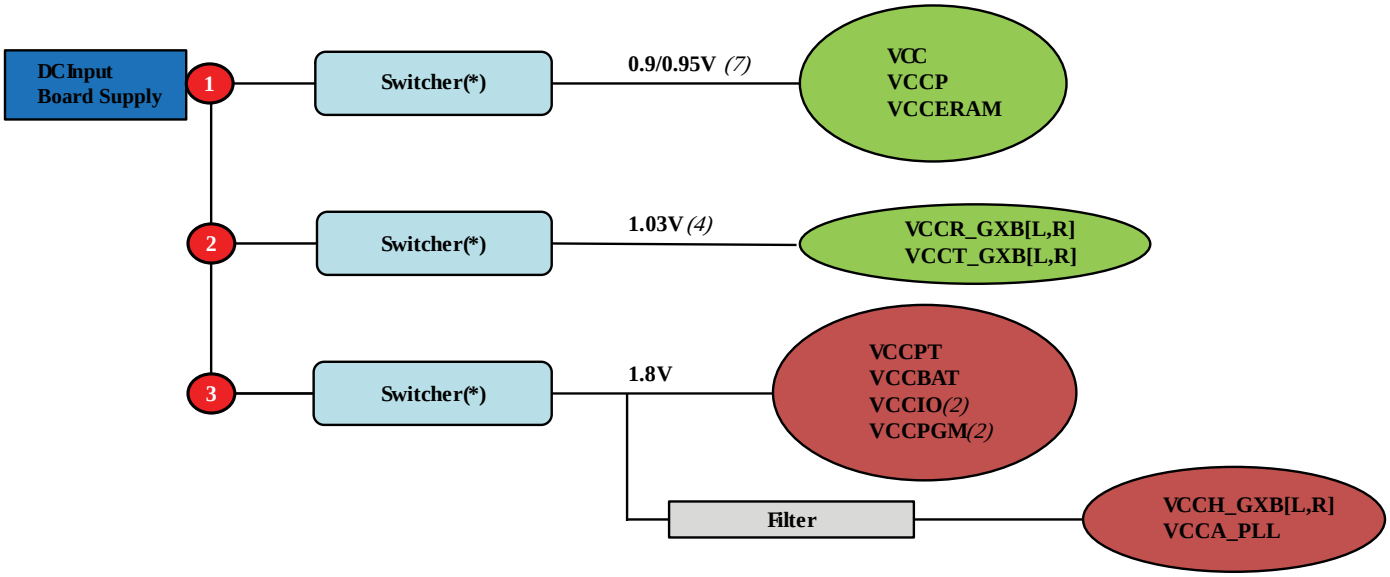
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCR_GXB[L,R] VCCT_GXB[L,R]	2	1.03	±30 mV	Switcher(*)	Share	Option provided for VCCR_GXB and VCCT_GXB to share the same regulator when all power rails required the same voltage level. For details, refer to note 4 of the *Notes to Power Supply Sharing Guidelines*. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCBAT	3	Varies	± 5% (**)	Switcher(*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO and VCCPGM to share the same regulator when all power rails require 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 GX device is provided in Figure 3.

Figure 3. Example Power Supply Sharing Guidelines for Intel Arria 10 GX with Transceiver Data Rate <= 17.4 Gbps(**) for Chip-to-Chip Applications (Transceiver Data Rate <= 12.5 Gbps (**) for Backplane Applications)



Example 4—Intel Arria 10 GT

Table 18. Power Supply Sharing Guidelines for Intel Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications

Example Requiring 3 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9	± 30mV	Switcher (*)	Share	You have the option to source VCC and VCCP from the same regulator as VCCERAM
VCCP						
VCCERAM						

continued...

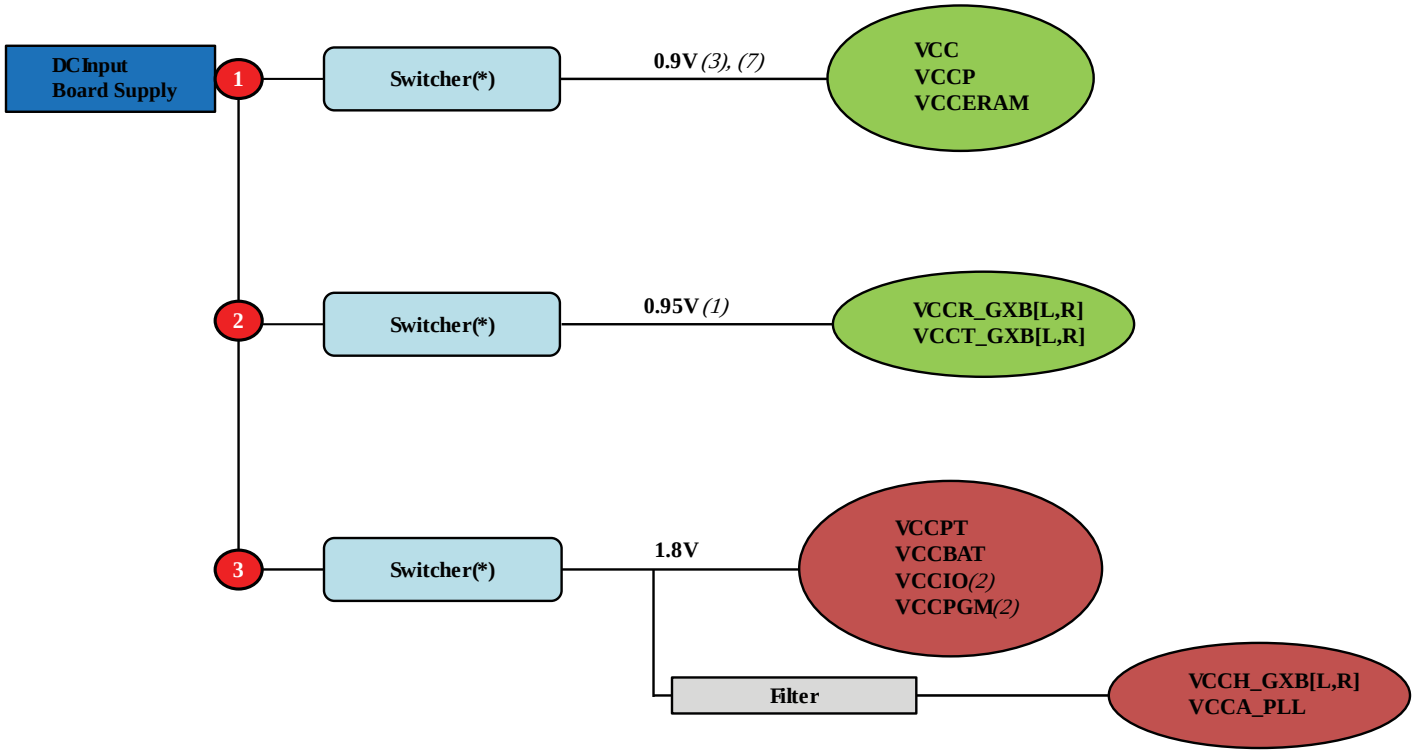
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						when all the power rails require the same voltage level. When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCR_GXB[L,R] VCCT_GXB[L,R]	2	0.95	± 30mV	Switcher (*)	Share	For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. VCCR_GXB and VCCT_GXB must be 1.03V or higher in order to support PCIe Gen 3. To meet DisplayPort TX electrical full compliance, $_{VCCT\_GXB}$ must be 1.03V or higher. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCBAT	3	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, and VCCPGM to share the same regulator when all power rails require 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 GT device is provided in Figure 4.

Figure 4. Example Power Supply Sharing Guidelines for Intel Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications



Example 5—Intel Arria 10 GT

Table 19. Power Supply Sharing Guidelines for Intel Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications

Example Requiring 2 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCP VCCERAM	1	0.95	± 30mV	Switcher (*)	Share	You have the option to source VCC and VCCP from the same regulator as VCCERAM when all the power rails require the same voltage level. When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCR_GXB[L,R] VCCT_GXB[L,R]					Isolate	Option provided to share VCCR_GXB and VCCT_GXB with the same regulator as VCC, VCCP, and VCCERAM when all power rails require 0.95V with proper isolation filter. For details, refer to note 1 of the *Notes to Power Supply Sharing Guidelines*. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. VCCR_GXB and VCCT_GXB must be 1.03V or higher in order to support PCIe Gen 3. To meet DisplayPort TX electrical full compliance, VCCT_GXB must be 1.03V or higher. When implementing a filtered supply topology, you must consider the IR drop across the filter. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCBAT VCCPT	2	Varies 1.8	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, and VCCPGM to share the same regulator when all power rails require

continued...

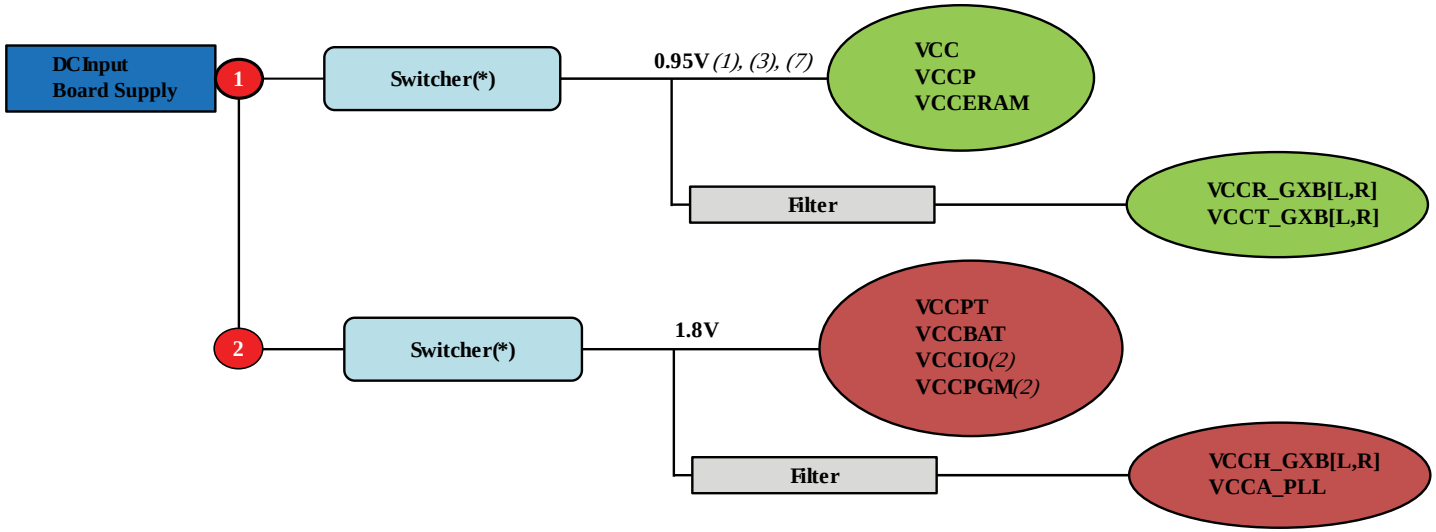
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCIO		Varies				1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPGM						
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 GT device is provided in Figure 5.

Figure 5. Example Power Supply Sharing Guidelines for Intel Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications



Example 6—Intel Arria 10 GT

Table 20. Power Supply Sharing Guidelines for Intel Arria 10 GT with Transceiver Data Rate <= 15.0 Gbps(**) for Chip-to-Chip Applications (Transceiver Data Rate <= 12.5 Gbps(**) for Backplane Applications)

Example Requiring 3 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9/0.95	± 30mV	Switcher (*)	Share	VCC, VCCP, and VCCERAM support 0.9V and 0.95V. You have the option to source VCC and VCCP from the same regulator as VCCERAM when all the power rails require the same voltage level. For more details, refer to the Electrical Specifications in the *Intel Arria 10 Device Datasheet*.
VCCP						
VCCERAM						

continued...

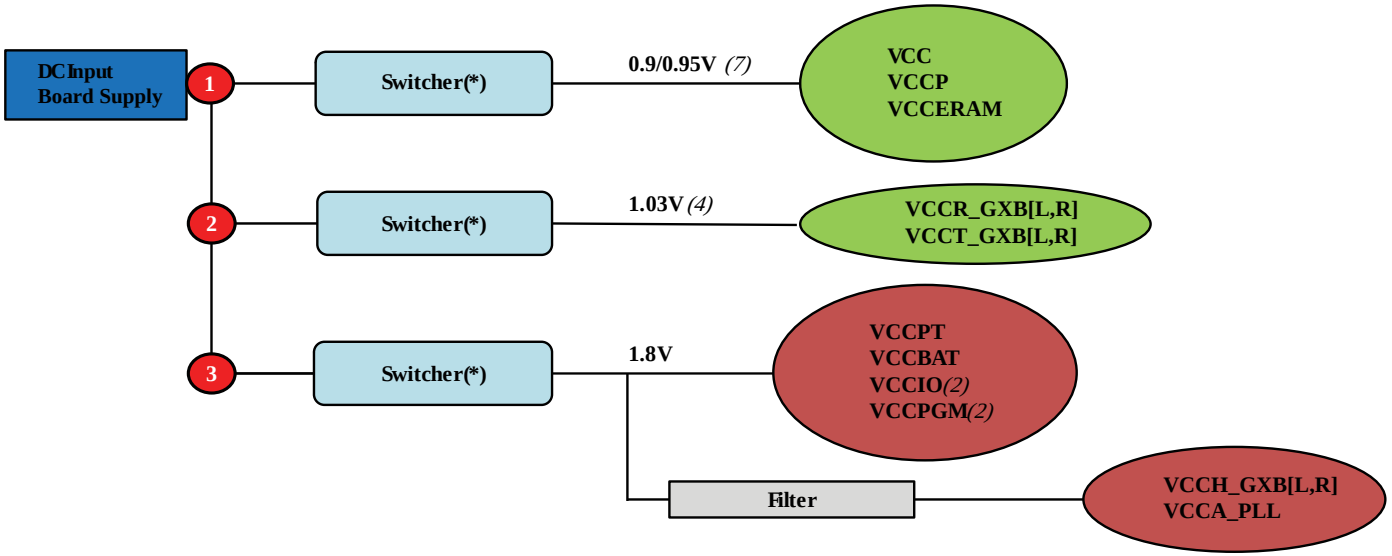
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCR_GXB[L,R] VCCT_GXB[L,R]	2	1.03	± 30mV	Switcher (*)	Share	Option provided for VCCR_GXB and VCCT_GXB to share the same regulator when all power rails require the same voltage level. For details, refer to note 4 of the *Notes to Power Supply Sharing Guidelines*. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCBAT	3	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, and VCCPGM to share the same regulator when all power rails require 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 GT device is provided in Figure 6.

Figure 6. Example Power Supply Sharing Guidelines for Intel Arria 10 GT with Transceiver Data Rate <= 15.0 Gbps(**) for Chip-to-Chip Applications (Transceiver Data Rate <= 12.5 Gbps(**) for Backplane Applications)



Example 7—Intel Arria 10 GT

Table 21. Power Supply Sharing Guidelines for Intel Arria 10 GT with Transceiver Data Rate <= 17.4 Gbps(**)/25.8 Gbps for Chip-to-Chip Applications (Transceiver Data Rate <= 12.5 Gbps(**) for Backplane Applications)

Example Requiring 4 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9/0.95	± 30mV	Switcher (*)	Share	VCC, VCCP, and VCCERAM support 0.9V and 0.95V. You have the option to source VCC and VCCP from the same regulator as VCCERAM when all the power rails require the same voltage level. For more
VCCP						
VCCERAM						

continued...

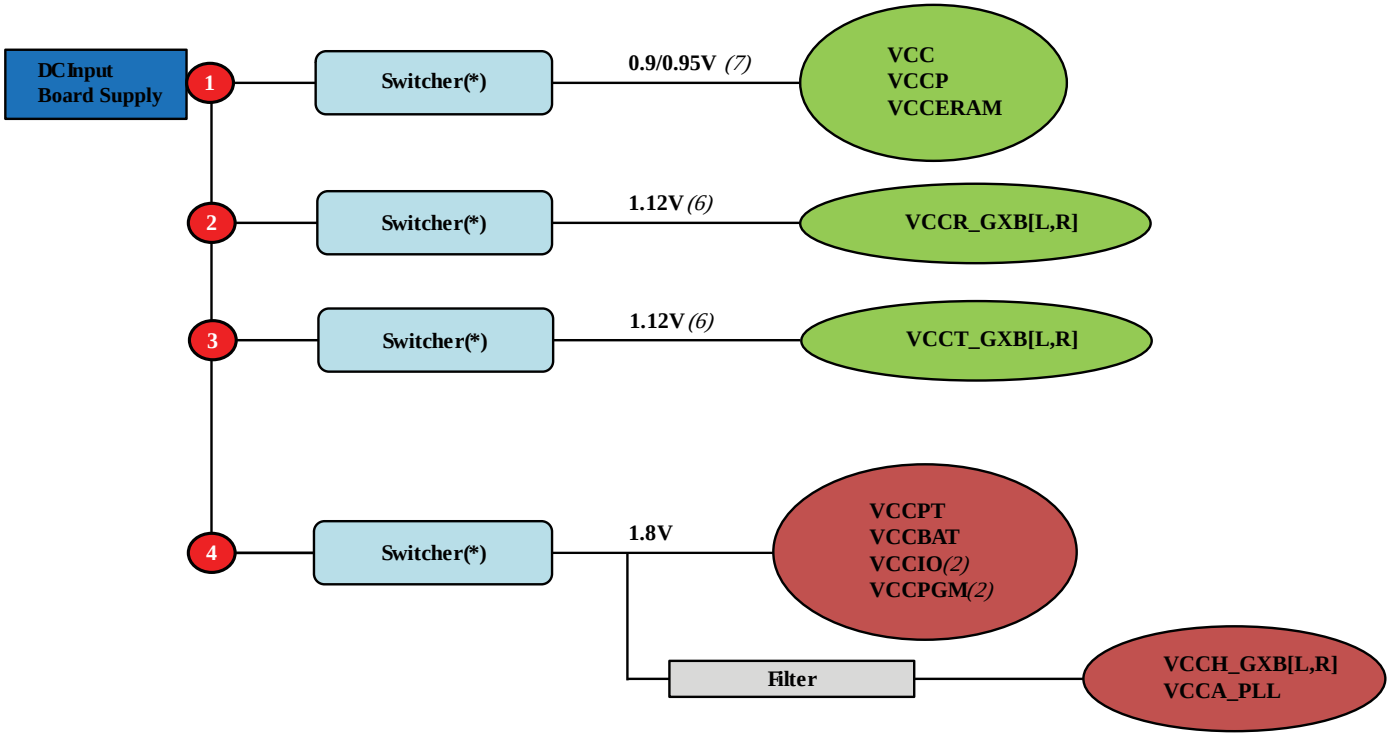
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						details, refer to the Electrical Specifications in the *Intel Arria 10 Device Datasheet*. When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCR_GXB[L,R]	2	1.12	± 20mV	Switcher (*)	Isolate	You have the option to source VCCR_GXB from a switcher. For details, refer to note 6 of the *Notes to Power Supply Sharing Guidelines*. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCT_GXB[L,R]	3	1.12	± 20mV	Switcher (*)	Isolate	You have the option to source VCCT_GXB from a switcher. For details, refer to note 6 of the *Notes to Power Supply Sharing Guidelines*. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCBAT	4	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, and VCCPGM to share the same regulator when all power rails require 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 GT device is provided in Figure 7.

Figure 7. Example Supply Sharing Guidelines for Intel Arria 10 GT with Transceiver Data Rate <= 17.4 Gbps(**)/25.8 Gbps for Chip-to-Chip Applications (Transceiver Data Rate <= 12.5 Gbps(**) for Backplane Applications)



Example 8—Intel Arria 10 SX

Table 22. Power Supply Sharing Guidelines for Intel Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications

Example Requiring 3 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9	± 30mV	Switcher (*)	Share	You have the option to source VCC, VCCP, and VCCERAM from the same regulator as VCCL_HPS when all the power rails require the same voltage level. When sharing the same regulator for VCCERAM, VCCL_HPS, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCP						
VCCERAM						
VCCL_HPS						
VCCR_GXB[L,R]	2	0.95	± 30mV	Switcher (*)	Share	For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. VCCR_GXB and VCCT_GXB must be 1.03V or higher in order to support PCIe Gen 3. To meet DisplayPort TX electrical full compliance, $_{VCCT\_GXB}$ must be 1.03V or higher. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCT_GXB[L,R]						
VCCBAT	3	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, VCCPGM, VCCIO_HPS, and VCCIOREF_HPS to share the same regulator when all power rails require 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCIO_HPS						
VCCIOREF_HPS		1.8				

continued...

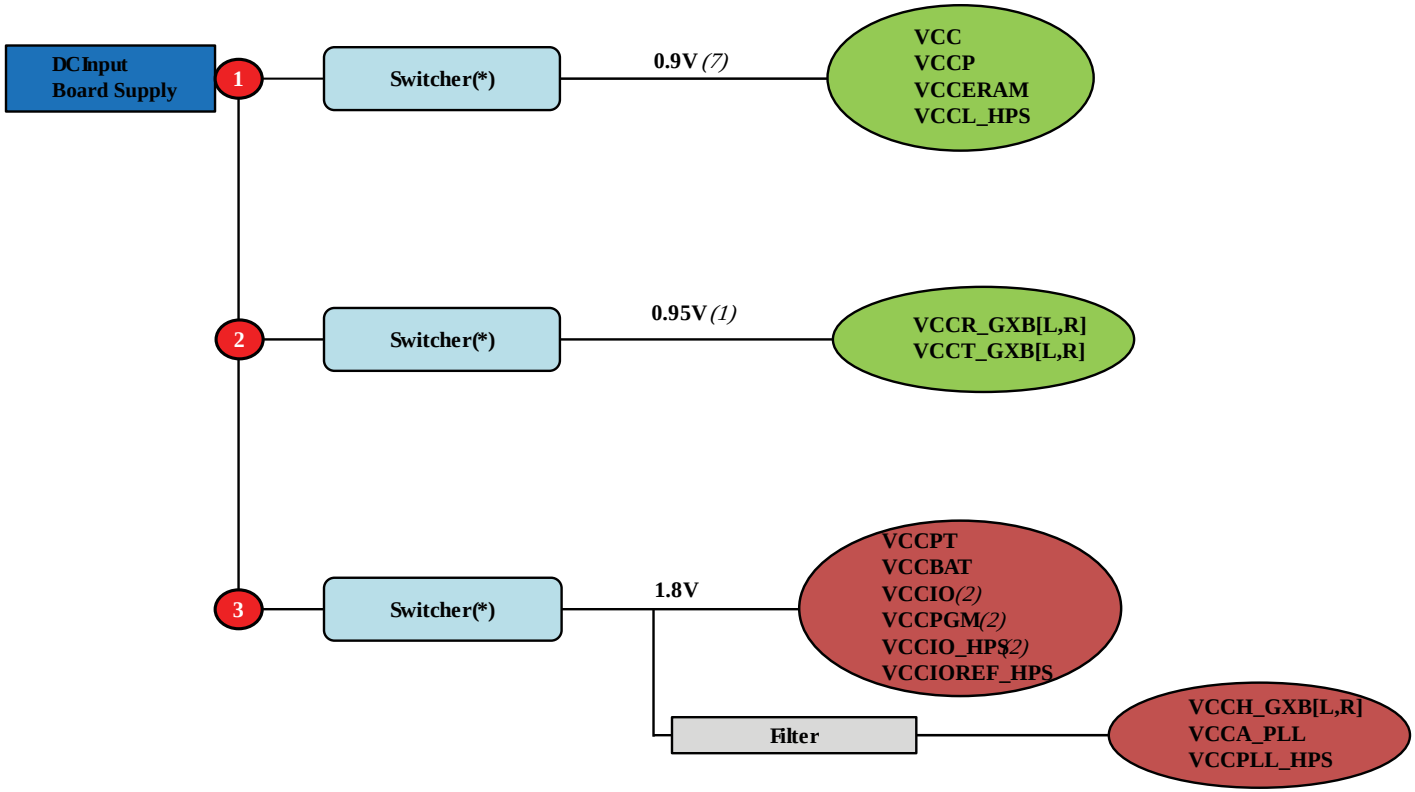
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB, VCCA_PLL, and VCCPLL_HPS with the same regulator as VCCBAT, VCCPT, VCCIO, VCCPGM, VCCIO_HPS, and VCCIOREF_HPS when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						
VCCPLL_HPS						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 SX Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 SX device is provided in Figure 8.

Figure 8. Example Power Supply Sharing Guidelines for Intel Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications



Example 9—Intel Arria 10 SX

Table 23. Power Supply Sharing Guidelines for Intel Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications

Example Requiring 2 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.95	± 30mV	Switcher (*)	Share	You have the option to source VCC, VCCP, and VCCERAM from the same regulator as VCCL_HPS when all the power rails require the same voltage level. When sharing the same regulator for VCCERAM, VCCL_HPS, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCP						
VCCERAM						
VCCL_HPS						
VCCR_GXB[L,R]					Isolate	Option provided to share VCCR_GXB and VCCT_GXB with the same regulator as VCC, VCCP, and VCCERAM when all power rails require 0.95V with proper isolation filter. For details, refer to note 1 of the *Notes to Power Supply Sharing Guidelines*. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. VCCR_GXB and VCCT_GXB must be 1.03V or higher in order to support PCIe Gen 3. To meet DisplayPort TX electrical full compliance, $_{VCCT\_GXB}$ must be 1.03V or higher. When implementing a filtered supply topology, you must consider the IR drop across the filter. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCT_GXB[L,R]						

continued...

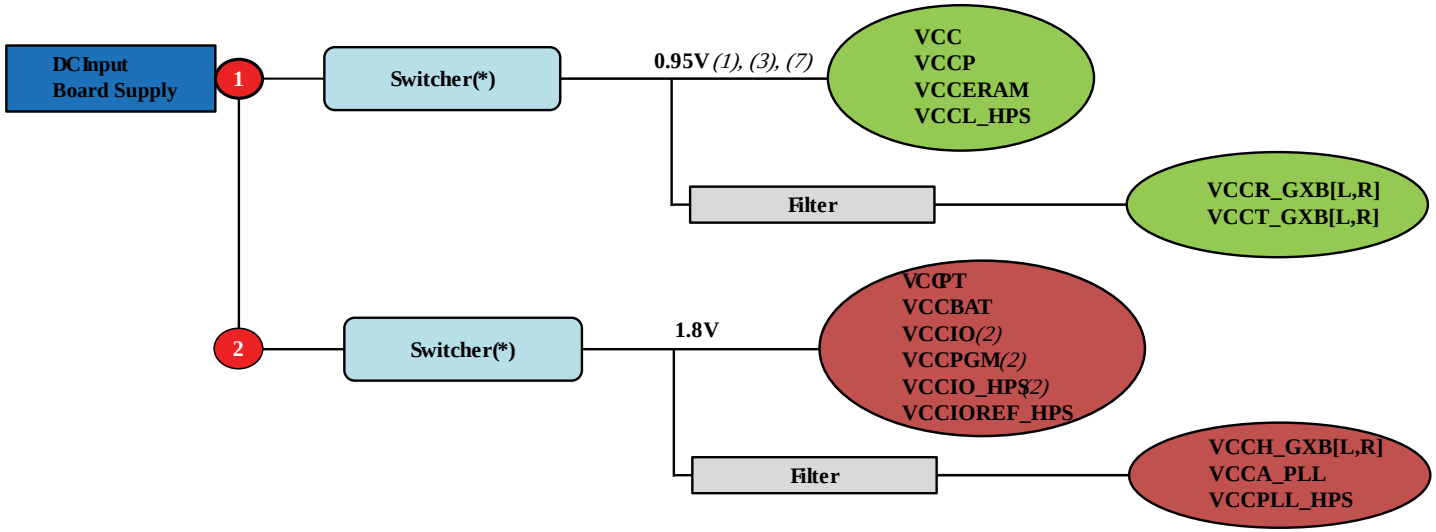
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCBAT	2	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, VCCPGM, VCCIO_HPS, and VCCIOREF_HPS to share the same regulator when all power rails require 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCIO_HPS						
VCCIOREF_HPS		1.8				
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB, VCCA_PLL, and VCCPLL_HPS with the same regulator as VCCBAT, VCCPT, VCCIO, VCCPGM, VCCIO_HPS, and VCCIOREF_HPS when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						
VCCPLL_HPS						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 SX Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 SX device is provided in Figure 9.

Figure 9. Example Power Supply Sharing Guidelines for Intel Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications



Example 10—Intel Arria 10 SX

Table 24. Power Supply Sharing Guidelines for Intel Arria 10 SX with Transceiver Data Rate <= 17.4 Gbps(**) for Chip-to-Chip Applications (Transceiver Data Rate <= 12.5 Gbps (**) for Backplane Applications)

Example Requiring 3 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9/0.95	± 30mV	Switcher (*)	Share	VCC, VCCP, VCCERAM, and VCCL_HPS support 0.9V and 0.95V. You have the option to source VCC, VCCP, and VCCERAM from the same regulator as VCCL_HPS when all the power rails require the same voltage level. For more details, refer to the Electrical Specifications in the *Intel Arria 10 Device Datasheet*.
VCCP						
VCCERAM						
VCCL_HPS						

continued...

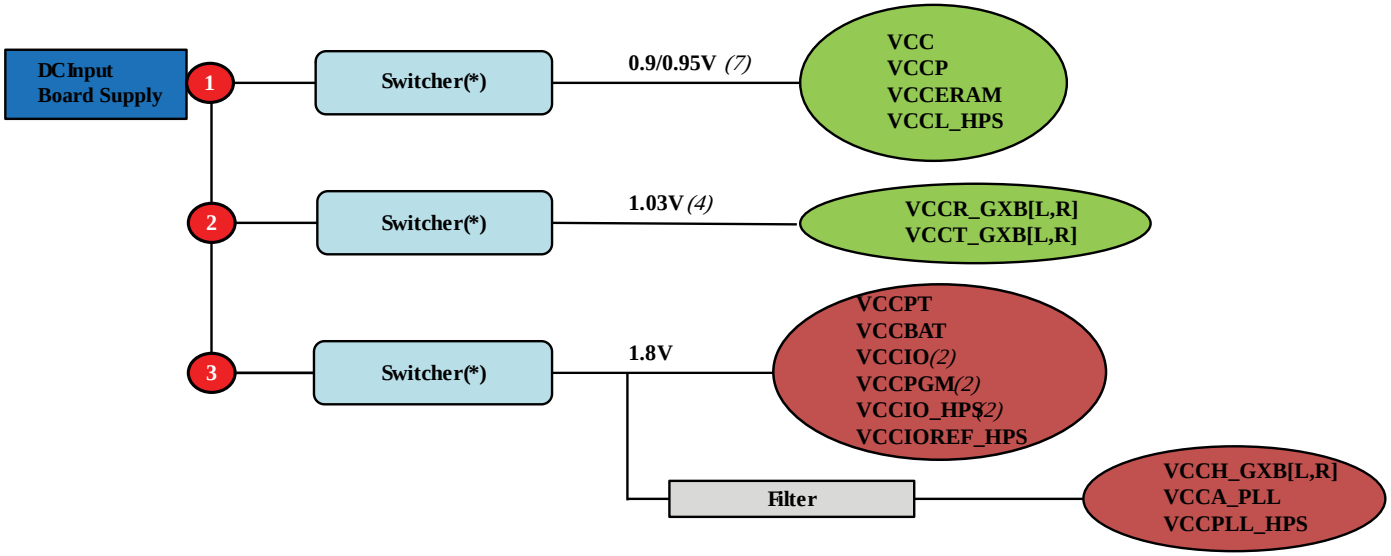
Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						When sharing the same regulator for VCCERAM, VCCL_HPS, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.
VCCR_GXB[L,R] VCCT_GXB[L,R]	2	1.03	± 30mV	Switcher (*)	Share	Option provided for VCCR_GXB and VCCT_GXB to share the same regulator when all power rails require the same voltage level. For details, refer to note 4 of the *Notes to Power Supply Sharing Guidelines*. For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCBAT	3	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, VCCPGM, VCCIO_HPS, and VCCIOREF_HPS to share the same regulator when all power rails require 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCIO_HPS						
VCCIOREF_HPS		1.8				
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB, VCCA_PLL, and VCCPLL_HPS with the same regulator as VCCBAT, VCCPT, VCCIO, VCCPGM, VCCIO_HPS, and VCCIOREF_HPS when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						
VCCPLL_HPS						

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 SX Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 SX device is provided in Figure 10.

Figure 10. Example Power Supply Sharing Guidelines for Intel Arria 10 SX with Transceiver Data Rate <= 17.4 Gbps(**) for Chip-to-Chip Applications (Transceiver Data Rate <= 12.5 Gbps (**) for Backplane Applications)



Example 11—Intel Arria 10 GX (Using the SmartVID Feature)

Table 25. Power Supply Sharing Guidelines for Intel Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications Using the SmartVID Feature (***)

Example Requiring 4 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	0.9	± 30mV	Switcher (*)	Share	For more details about the VCC and VCCP voltage range when the SmartVID feature is enabled, refer to the *Intel Arria 10 Device Datasheet*.
VCCP						
VCCERAM	2	0.9	± 30mV	Switcher (*)	Isolate	To use the SmartVID feature, VCCERAM has to be on a separate regulator.
VCCR_GXB[L,R]	3	0.95	± 30mV	Switcher (*)	Share	For better performance and in order to meet PCIe Gen 3 jitter specifications, isolate VCCR_GXB and VCCT_GXB from each other with at least 30dB of isolation for a 1MHz to 100MHz bandwidth. VCCR_GXB and VCCT_GXB must be 1.03V or higher in order to support PCIe Gen 3. To meet DisplayPort TX electrical full compliance, $_{VCCT\_GXB}$ must be 1.03V or higher. For designs that have high-current for VCCR_GXB or VCCT_GXB, you should consider the IR drop through the supply planes and compensate for it.
VCCT_GXB[L,R]						
VCCBAT	4	Varies	± 5% (**)	Switcher (*)	Share if 1.8V	Option provided for VCCBAT, VCCPT, VCCIO, and VCCPGM to share the same regulator when all power rails required 1.8V. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Arria 10 devices.
VCCPT		1.8				
VCCIO		Varies				
VCCPGM						
VCCH_GXB[L,R]		1.8			Isolate	Option provided to share VCCH_GXB and VCCA_PLL with the same regulator as VCCBAT, VCCPT, VCCIO, and VCCPGM when all power rails require 1.8V with a proper isolation filter.
VCCA_PLL						

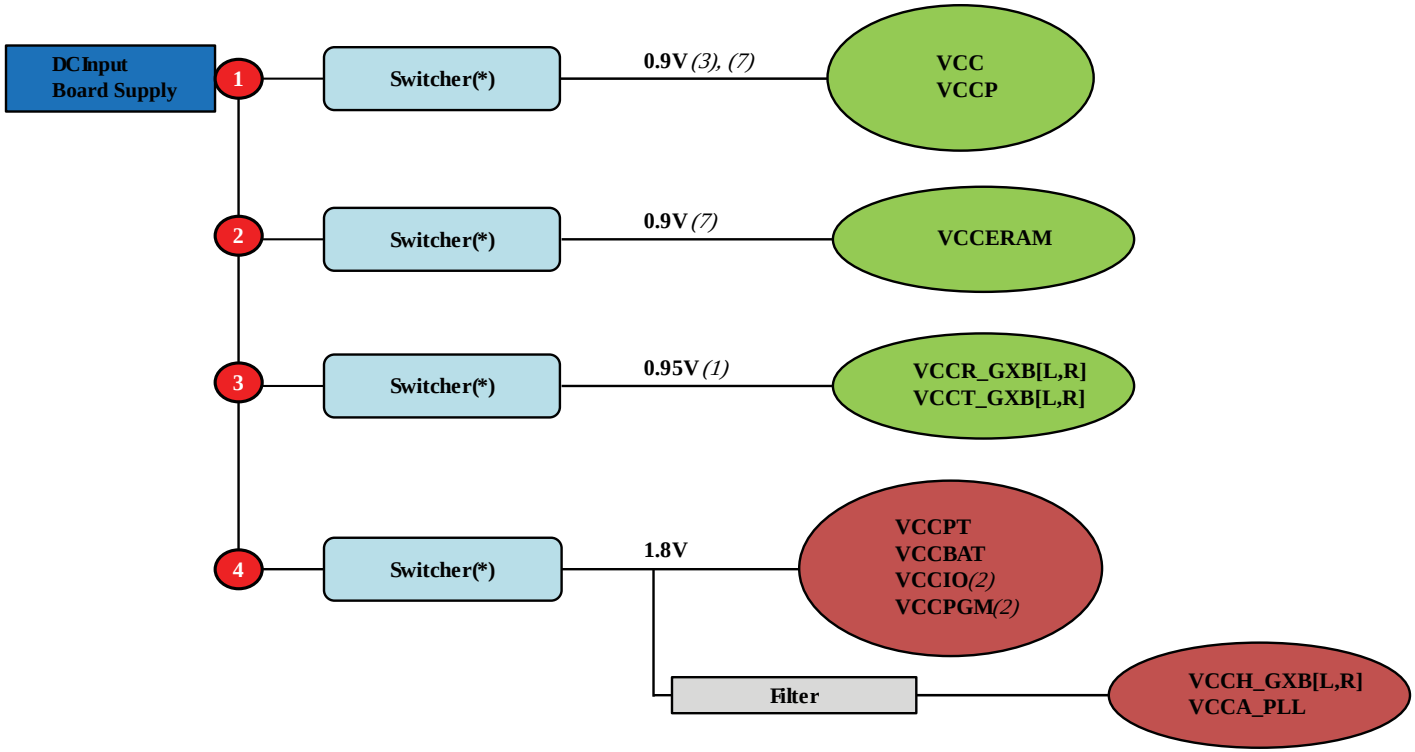
(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines*.

(**)The supported tolerance for the V_{CCIO} power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Arria 10 Device Datasheet*. Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

(***) This is an example using the Intel Arria 10 GX device when you are using the SmartVID feature. If you are using the SmartVID feature for other Intel Arria 10 devices, do take note that you need to source VCC and VCCP from a separate dedicated regulator.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Arria 10 GX device is provided in Figure 11.

Figure 11. Example Power Supply Sharing Guidelines for Intel Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications Using the SmartVID Feature



Notes to Power Supply Sharing Guidelines

1. For more information about the supported transceiver speed grades for Intel Arria 10 GX and SX devices, refer to the Transmitter and Receiver Data Rate Performance for Intel Arria 10 GX/SX Devices table in the *Intel Arria 10 Device Datasheet*.
2. Assumes VCCIO, VCCPGM, and VCCIO_HPS are 1.8V. Only if these power rails share the same regulator as VCCPT can their power sequence ramp with VCCPT in Group 2. If any of these rails are other than 1.8V, then these rails must be separately regulated and must follow the power sequence requirement in Group 3. For more information about the power sequence requirements, refer to the *Power Management for Intel Arria 10 Devices*.
3. The SmartVID feature is supported for VCC and VCCP. In these cases, VCC and VCCP can be 0.85V-0.9V depending on the device requirements. The SmartVID feature is not supported when VCCR_GXB and VCCT_GXB are shared with VCC and VCCP.
4. For more information about the supported transceiver speed grades for Intel Arria 10 GT devices, refer to the Transmitter and Receiver Data Rate Performance for Intel Arria 10 GT Devices table in the *Intel Arria 10 Device Datasheet*.
5. For more information about the maximum transceiver channel supported for Intel Arria 10 GT devices, refer to the *Intel Arria 10 Transceiver PHY User Guide*.
6. For more information about the transceiver data rate and maximum transceiver channel supported for Intel Arria 10 GT devices, refer to the *Intel Arria 10 Transceiver PHY User Guide*.
7. You have the option to source VCC and VCCP from the same regulator as VCCERAM when all the power rails require the same voltage level. When sharing the same regulator for VCCERAM, VCC, and VCCP, the SmartVID feature is not available. If you use the SmartVID feature, then VCC and VCCP need to be sourced by a separate dedicated regulator.

(*)When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 7 of the *Notes to Pin Connection Guidelines*.

(**)Actual transceiver data rate for the Intel Arria 10 GX and SX devices is dependent on the device's transceiver speed grade and core speed grade. For more information about the valid combinations of transceiver and core speed grades, refer to the Transmitter and Receiver Data Rate Performance for Intel Arria 10 GX/SX Devices table in the *Intel Arria 10 Device Datasheet*.

(***)Actual transceiver data rate for the Intel Arria 10 GT device is dependent on the device's transceiver speed grade and core speed grade. For more information about the valid combinations of transceiver and core speed grades, refer to the Transmitter and Receiver Data Rate Performance for Intel Arria 10 GT Devices table in the *Intel Arria 10 Device Datasheet*.

Document Revision History for Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines

Document Version	Changes
2018.12.12	• Updated the connection guidelines for the HPS_Shared_Q2_2 and HPS_Shared_Q4_2 pins.
2018.03.30	• Added guidelines to avoid excess current on the I/O pins in the *Notes to Intel Arria 10 GX and GT Pin Connection Guidelines* and *Notes to Intel Arria 10 SX Pin Connection Guidelines* sections. • Updated the connection guidelines for the nPERST[L,R][0:1] pins to include on the compatible I/O standards. • Updated the supported protocols in the pin description for the following pins: — CQ[#] — CQn[#] — CQ[#]_[#]/CQn[#]_[#] — QK[#]_[#] — QKn[#]_[#] — A_[#] — BA_[#] — REF# — WE_N_0 — CAS_N_0 — RAS_N_0 — RPS_N_0 — WPS_N_0 — REF_N_0 • Updated the connection guidelines for the VCCP and VCC pins. • Updated the connection guidelines for VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J] and VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J] pins. • Updated the connection guidelines for VCCH_GXB[L,R] pins to add the VRM switching frequency guidelines. • Updated the connection guidelines for the HPS_CLK1 pin to include the hps_clk_f fuse information. • Updated the connection guidelines of the HPS_DEDICATED_[4,5,7,8,9,12,13,14,15] pins to include information on the pull-up resistor. • Updated the connection guidelines of the HPS_Shared_Q1_[1,2,4,5,6,7,8,9,10,11] and HPS_Shared_Q4_2 pins to include information on the pull-up resistor. • Updated the connection guidelines of the BOOTSEL[0..2] pins. • Removed the CA_[#]_[#] pins.

Date	Version	Description of Changes
June 2017	2017.06.16	• Added note 11 to the Notes to Arria 10 GX and GT Pin Connection Guidelines. • Updated the pin functions and connection guidelines for the RZQ_[#] pin. • Updated the pin functions for the CLKUSR pin. • Added a note for the DisplayPort TX electrical full compliance in the following power sharing guidelines: — Example 1. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications — Example 2. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications — Example 4. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications — Example 5. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications — Example 8. Power Supply Sharing Guidelines for Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications — Example 9. Power Supply Sharing Guidelines for Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications — Example 11. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications Using the SmartVID Feature (***)
March 2017	2017.03.13	Rebranded as Intel.
December 2016	2016.12.09	• Updated the connection guidelines for VCCH_GXB[L,R] pins. • Updated the connection guidelines for CLK_[2,3] [A,B,C,D,E,F,G,H,I, J,K,L]_[0,1]p and CLK_[2,3] [A,B,C,D,E,F,G,H,I, J,K,L]_[0,1]n pins. • Updated the connection guidelines for the RZQ_[#] pin. • Updated the connection guidelines for the ALERT_N_0 pin.
June 2016	2016.06.10	• The document is no longer preliminary. • Updated the HPS Peripheral Pins and Shared 3V I/O Bank Pins. • Updated the connection guidelines for VCCR_GXB and VCCT_GXB pins. • Removed support for the VCC PowerManager feature. • Updated note (3) in the Notes to Power Supply Sharing Guidelines. • Updated the maximum backplane applications support to 12.5 Gbps. • Removed backplane applications support when VCCR_GXB amd VCCT_GXB is at 0.95V.
March 2016	2016.03.17	Updated the supported transceiver data rates in the Notes to Power Supply Sharing Guidelines section.
November 2015	2015.11.02	• Changed instances of Quartus II to Quartus Prime. • Updated the connection guidelines of the REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J]_CH[B,T]p and REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J]_CH[B,T]n pins. • Updated the connection guidelines of the VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J] pins.

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Date	Version	Description of Changes
		• Updated the connection guidelines of the VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J] pins. • Updated the connection guidelines of the VCCH_GXB[L,R] pins. • Updated the connection guidelines of the CLKUSR pin. • Updated the pin type and pin description for the ALERT_N_0, PAR_0, ACT_N_0, and BG_[#0 pins. • Updated the connection guidelines of the ADCGND pin. • Updated the pin description of the HPS_nRST pin. • Updated the pin description of the VCC pin. • Updated the connection guidelines of the nIO_PULLUP pin. • Updated the connection guidelines of the VCCLSENSE and GNDSENSE pins. • Updated the minimum voltage to 0.95V in the connection guidelines of the VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J] and VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J] pins. • Updated the following power sharing guidelines to include 0.95V and 1.12V support for VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J] and VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J]: — Example 1. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 2. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 4. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 5. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 7. Power Supply Sharing Guidelines for Arria 10 GT with 15.0 Gbps < Transceiver Data Rate <= 17.4 Gbps(**)/28.3 Gbps for Chip-to-Chip Applications (14.2 Gbps < Transceiver Data Rate <= 17.4 Gbps(**) for Backplane Applications) — Example 8. Power Supply Sharing Guidelines for Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 9. Power Supply Sharing Guidelines for Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 11. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) Using the SmartVID Feature (***)
April 2015	2015.04.05	• Updated the connection guidelines of VCCP and VCC pins. • Updated the connection guidelines of RREF [T,B][L,R] pins. • Updated the connection guidelines of nPERST[L,R][0:1] pins. • Updated the connection guidelines of the VREFP_ADC pins. • Updated the connection guidelines of the VCCERAM pin. • Updated the connection guidelines of VREFB[[2][A,F,G,H,I,J,K,L],[3][A,B,C,D,E,F,G,H]]N0 pins.

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Date	Version	Description of Changes
		• Updated the on-chip reference source to ±10% in the connection guidelines of the VREFP_ADC pin. • Updated the supported nominal voltage of VCCR_GXB[L1,R4][C,D,E,F,G,H,I,J] and VCCT_GXB[L1,R4][C,D,E,F,G,H,I,J] from 1.0V and 1.1V to 1.03V and 1.11V, respectively. — Updated the connection guidelines for VCCR_GXB[L1,R4][C,D,E,F,G,H,I,J] and VCCT_GXB[L1,R4][C,D,E,F,G,H,I,J]. — Updated the following power sharing guidelines for the supported nominal voltage of 1.03V and 1.11V for VCCR_GXB[L1,R4][C,D,E,F,G,H,I,J] and VCCT_GXB[L1,R4][C,D,E,F,G,H,I,J]: • Example 3. Power Supply Sharing Guidelines for Arria 10 GX with 11.3 Gbps < Transceiver Data Rate <= 17.4 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps <Transceiver Data Rate <= 17.4 Gbps (**) for Backplane Applications) • Example 6. Power Supply Sharing Guidelines for Arria 10 GT with 11.3 Gbps < Transceiver DataRate <= 15.0 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps < Transceiver Data Rate <= 14.2 Gbps(**) for Backplane Applications) • Example 7. Power Supply Sharing Guidelines for Arria 10 GT with 15.0 Gbps < Transceiver Data Rate <= 17.4 Gbps(**)/28.3 Gbps for Chip-to-Chip Applications (14.2 Gbps < Transceiver Data Rate <= 17.4 Gbps(**) for Backplane Applications) • Example 10. Power Supply Sharing Guidelines for Arria 10 SX with 11.3 Gbps < Transceiver Data Rate <= 17.4 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps <Transceiver Data Rate <= 17.4 Gbps (**) for Backplane Applications) — Updated the supported nominal voltage of 1.03V and 1.11V for VCCR_GXB[L1,R4][C,D,E,F,G,H,I,J] and VCCT_GXB[L1,R4][C,D,E,F,G,H,I,J] in the Notes to Power Supply Sharing Guidelines. • Added Shared 3V I/O Bank pins for Arria 10 HPS.
January 2015	2015.01.23	• Updated the connection guidelines for VCCIO([2][A, F,G,H,I,J,K, L, AF, KL], [3][A, B,C,D,E,F,G, H, AB, GH]) pins. • Updated the connection guidelines for the CONF_DONE pin. • Updated the connection guidelines for the nSTATUS pin. • Updated the connection guidelines for VREFP_ADC and VREFN_ADC pins. • Updated the pin type for VSIGP and VSIGN pins. • Updated the pin type for the HPS_nRST pin. • Updated the pin type for the HPS_nPOR pin. • Updated the pin description of the CRC_ERROR pin. • Updated the pin description of the HPS_nRST pin. • Updated the connection guidelines for VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J] and VCCR_GXB[L1,R4][C,D,E,F,G,H,I,J] pins. • Updated the pin description for VCCIOREF_HPS pin.

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Date	Version	Description of Changes
		• Updated note (11) in the Notes to Arria 10 SX Pin Connection Guidelines. • Updated the following power sharing guidelines to include 0.95V support for VCC and VCCP: — Example 1. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 3. Power Supply Sharing Guidelines for Arria 10 GX with 11.3 Gbps < Transceiver Data Rate <= 17.4 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps <Transceiver Data Rate <= 17.4 Gbps (**) for Backplane Applications) — Example 4. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 6. Power Supply Sharing Guidelines for Arria 10 GT with 11.3 Gbps < Transceiver Data Rate <= 15.0 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps < Transceiver Data Rate <= 14.2 Gbps(**) for Backplane Applications) — Example 7. Power Supply Sharing Guidelines for Arria 10 GT with 15.0 Gbps < Transceiver Data Rate <= 17.4 Gbps(**)/28.3 Gbps for Chip-to-Chip Applications (14.2 Gbps < Transceiver Data Rate <= 17.4 Gbps(**) for Backplane Applications) — Example 8. Power Supply Sharing Guidelines for Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 10. Power Supply Sharing Guidelines for Arria 10 SX with 11.3 Gbps < Transceiver Data Rate <= 17.4 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps <Transceiver Data Rate <= 17.4 Gbps (**) for Backplane Applications) • Added the following power sharing guidelines: — Example 2. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 5. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 9. Power Supply Sharing Guidelines for Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications)
August 2014	2014.08.18	• Added Example 8. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) Using the SmartVID Feature. • Updated the transceiver data rate to 28.3 Gbps. • Updated the pin name and pin description of the PLL_[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_FB[0,1] pins. • Updated the connection guidelines for the TCK, TMS, TDI, TDO, and TRST pins. • Updated the pin name and connection guidelines of the CRC_ERROR pin. • Updated the connection guidelines of the nPERST[L,R][0:1] pins. • Updated the connection guidelines of the VREFP_ADC pin. • Updated the connection guidelines of the VSIGP_[0,1] and VSIGN_[0,1] pins. • Updated the connection guidelines of the VCCP and VCC pins. • Updated the pin name of the VCCIO([2][A,F,G,H,I,J,K,L,AF,KL],[3][A,B,C,D,E,F,G,H,AB,GH]) pins. • Updated the connection guidelines of the VCCERAM pins.

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Date	Version	Description of Changes
		• Updated the connection guidelines of the VREFB([2][A,F,G,H,I,J,K,L],[3][A,B,C,D,E,F,G,H])N0 pins. • Updated the connection guidelines of the VCCLSENSE and GNDSENSE pins. • Updated the connection guidelines for the ADCGND pin. • Updated the pin name, pin description, and connection guidelines of the VCCR_GXB[L1,R4] [C,D,E,F,G,H,I,J] pins. • Updated the pin name, pin description, and connection guidelines of the VCCT_GXB[L1,R4] [C,D,E,F,G,H,I,J] pins. • Updated the pin description and connection guidelines of the VCCH_GXB[L,R] pins. • Updated the pin name and pin description of the GXB[L1,R4][C,D,E,F,G,H,I,J]_RX_[0:5]p, GXB[L1,R4] [C,D,E,F,G,H,I,J]_RX_[0:5]n, GXB[L1,R4][C,D,E,F,G,H,I,J]_TX_CH[0:5]p, GXB[L1,R4] [C,D,E,F,G,H,I,J]_TX_CH[0:5]n pins. • Updated the pin name, pin description, and connection guidelines for the REFCLK_GXB[L1,R4] [C,D,E,F,G,H,I,J]_CH[B,T]p and REFCLK_GXB[L1,R4][C,D,E,F,G,H,I,J]_CH[B,T]n pins. • Updated the connection guidelines of the CLKUSR pins. • Updated the pin description and connection guidelines for the RREF_[T,B][L,R] pins. • Updated the Function 2 pin description of the HPS_DEDICATED_16 pin.
June 2014	2014.06.24	• Added note (7) to the Notes to Power Supply Sharing Guidelines section. • Updated the pin description for the PLL_[2,3][A,B,C,D,E,F,G,H,I,J,K,L]_FB0 pins. • Updated the connection guidelines for the TCK, TMS, TDI, TDO, and TRST pins. • Updated the connection guidelines for the VCCR_GXB[L,R][1:4][C,D,E,F,G,H,I,J] and VCCT_GXB[L,R][1:4] [C,D,E,F,G,H,I,J] pins. • Updated the connection guidelines for the VCCLSENSE and GNDSENSE pins.

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Date	Version	Description of Changes
		• Updated the connection guidelines for the VCCBAT, VCCPGM, VCCPT, and VCCH_GXB[L,R] pins. • Updated the CRCERROR pin name. • Updated the following power sharing guidelines: — Example 1. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 2. Power Supply Sharing Guidelines for Arria 10 GX with Transceiver Data Rate 11.3 Gbps < Data Rates <= 17.4 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps <Data Rates <= 17.4 Gbps (**) for Backplane Applications) — Example 3. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 4. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate 11.3 Gbps < Data Rates <= 15.0 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps < Data Rates <= 14.2 Gbps(**) for Backplane Applications) — Example 5. Power Supply Sharing Guidelines for Arria 10 GT with Transceiver Data Rate 15.0 Gbps < Data Rates <= 17.4 Gbps(**)/28 Gbps for Chip-to-Chip Applications (14.2 Gbps < Data Rates <= 17.4 Gbps(**) for Backplane Applications) — Example 6. Power Supply Sharing Guidelines for Arria 10 SX with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications (10.3125 Gbps for Backplane Applications) — Example 7. Power Supply Sharing Guidelines for Arria 10 SX with Transceiver Data Rate 11.3 Gbps < Data Rates <= 17.4 Gbps(**) for Chip-to-Chip Applications (10.3125 Gbps <Data Rates <= 17.4 Gbps (**) for Backplane Applications)
May 2014	2014.05.23	Updated the pin description and connection guidelines for the CLKUSR pin.
December 2013	2013.12.18	Updated the connection guidelines for VCC and VCCP pins.
December 2013	2013.12.02	Initial release.