Table 1 shows all pins for the EP2A15 672-pin FineLine BGA and the 724-pin ball-grid array (BGA) Packages.

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
8	IO	TrueDiff_TX01p	A23	C25	no
8	IO	TrueDiff_TX01n (2)	B23	C24	no
8	IO	TrueDiff_TX02n (2)	A24	C27	no
8	IO	TrueDiff_TX02p	B24	C26	no
-	VCCIO		VCCIO8	VCCIO8	
8	IO	TrueDiff_TX03p	C24	D25	no
8	IO	TrueDiff_TX03n (2)	C23	D24	no
8	IO	nWS (3)	F22	J20	
8	IO	TrueDiff_TX04n (2)	C26	D27	no
8	IO	TrueDiff_TX04p	C25	D26	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO	TrueDiff_TX05p	D24	E25	no
8	IO	TrueDiff_TX05n (2)	D23	E24	no
8	IO	nRS (3)	G22	J21	
8	IO	TrueDiff_TX06n	D26	E27	no
8	IO	TrueDiff_TX06p	D25	E26	no
-	GNDIO		GND	GND	
8	IO	TrueDiff_TX07p	E24	F25	no
8	IO	TrueDiff_TX07n (2)	E23	F24	no
8	IO	nCS (3)	G21	K20	
8	IO	TrueDiff_TX08n (2)	E26	F27	no
8	IO	TrueDiff_TX08p	E25	F26	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO	TrueDiff_TX09p	F24	G25	no
8	IO	TrueDiff_TX09n (2)	F23	G24	no
8	IO	CS (3)	H22	K21	
8	IO	TrueDiff_TX10n (2)	F26	G27	no
8	IO	TrueDiff_TX10p	F25	G26	no
-	VCCIO		VCCIO8	VCCIO8	
8	IO	TrueDiff_TX11p	G24	H25	no
8	IO	TrueDiff_TX11n (2)	G23	H24	no
8	IO	DEV_CLRn (4)	H21	K19	
8	IO	TrueDiff_TX12n (2)	G26	H27	no
8	IO	TrueDiff_TX12p	G25	H26	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO	TrueDiff_TX13p	H24	J25	no
8	IO	TrueDiff_TX13n (2)	H23	J24	no
8	IO		J20	L20	
8	IO	TrueDiff_TX14n (2)	H26	J27	no
8	IO	TrueDiff_TX14p	H25	J26	no
-	GNDIO		GND	GND	
8	IO	TrueDiff_TX15p	J23	K25	no
8	IO	TrueDiff_TX15n (2)	J24	K24	no
8	IO	TXLOCK1 (5)	J21	L18	
8	IO	TrueDiff_TX16n (2)	J26	L25	no
8	IO	TrueDiff_TX16p	J25	L24	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
8	IO	TrueDiff_TX17p	K24	L27	no
8	IO	TrueDiff_TX17n (2)	K23	L26	no
8	IO	LOCK4 (5)	K20	L21	
8	IO	TrueDiff_TX18n (2)	K26	M27	no
8	IO	TrueDiff_TX18p	K25	M26	no
-	VCCIO		VCCIO8	VCCIO8	
8	IO	TXCLK_OUT01p (6)	L24	M25	no
8	IO	TXCLK_OUT01n (2)	L23	M24	no
8	IO	DATA6 (3)	L20	K22	
8	IO		M26	N27	no
8	IO		M25	N26	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO	DATA7 (3)	M20	L23	
8	IO		J19	M21	
8	IO		K19	M20	
8	IO		L19	L22	
8	IO		L18	M22	
8	VREFC8 (7)		J22	L19	
-	GND_CKLK6 (8)		K22	N21	
-	VCC_CKLK6 (8)		K21	M19	
-	VCC_CKLK4 (8)		L21	M18	
-	GND_CKLK4 (8)		L22	N20	
8	IO		M19	M23	
8	IO		M18	N19	
8	IO		N19	P23	
8	IO		N18	N18	
-	GNDIO		GND	GND	
8	IO	CLKLK_FB2n (2)	N26	N25	
9	CLKLK_FB2p, (9), (10)		N25	N24	
8	IO	CLK4n (2)	M23	N22	
8	CLK4p		M24	N23	
8	IO	CLK2n (2)	N24	P25	
-	VCCIO		VCCIO8	VCCIO8	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
-	nIO_PULLUP (9), (11)		N20	P22	
8	DATA0 (9), (12)		P20	P18	
8	DCLK (9)		R20	P21	
8	CLK2p		N23	P24	
8	nCE (9)		U20	T23	
8	TDI (9)		T20	T22	
-	GNDIO		GND	GND	
-	GND_CKLK2 (8)		T22	P20	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	VCC_CKLK2 (8)		T21	P19	
-	VCCIO		VCCIO7	VCCIO7	
7	IO	DEV_OE (4)	V21	R21	
-	VCC_CKOUT2 (13)		P21	U23	
-	GND_CKOUT2 (13)		R21	R18	
9	CLKLK_OUT2p (9), (14)		P25	P27	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
7	IO	CLKLK_OUT2n (2)	P26	P26	
-	GNDIO		GND	GND	
7	IO	CLK6n (2)	P23	R22	
7	CLK6p		P24	R23	
7	IO	LOCK2 (5)	W22	R19	
7	IO	CLK8n (2)	R25	R24	
7	CLK8p		R26	R25	
-	VCC_CKLKA (15)		U22	U22	
-	VCC_CKLK8 (8)		U21	T18	
-	VCCIO		VCCIO7	VCCIO7	
-	GND_CKLK8 (8)		V22	R20	
7	VREFC7 (7)		Y22	T19	
7	IO		P18	U19	
7	IO		P19	V22	
7	IO		T18	U18	
7	IO		R18	T21	
7	IO		R19	W23	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		R23	R26	no
7	IO		R24	R27	no
7	IO		T19	T20	
7	IO	TXCLK_OUT2n (2)	T23	T24	no
7	IO	TXCLK_OUT2p (6)	T24	T25	no
-	GNDIO		GND	GND	
7	IO	TrueDiff_TX36p	U25	T26	no
7	IO	TrueDiff_TX36n (2)	U26	T27	no
7	IO		U18	V19	
7	IO	TrueDiff_TX35n (2)	U23	U26	no
7	IO	TrueDiff_TX35p	U24	U27	no
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO	TrueDiff_TX34p	V25	U24	no
7	IO	TrueDiff_TX34n (2)	V26	U25	no
7	IO		U19	U20	
7	IO	TrueDiff_TX33n (2)	V23	V24	no
7	IO	TrueDiff_TX33p	V24	V25	no
-	VCCIO		VCCIO7	VCCIO7	
7	IO	TrueDiff_TX32p	W25	W26	no
7	IO	TrueDiff_TX32n (2)	W26	W27	no
7	IO		V19	U21	
7	IO	TrueDiff_TX31n (2)	W23	W24	no
7	IO	TrueDiff_TX31p	W24	W25	no
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO	TrueDiff_TX30p	Y25	Y26	no
7	IO	TrueDiff_TX30n (2)	Y26	Y27	no
7	IO	TXLOCK2 (5)	AA22	W22	
7	IO	TrueDiff_TX29n (2)	Y23	Y24	no
7	IO	TrueDiff_TX29p	Y24	Y25	no
-	GNDIO		GND	GND	
7	IO	TrueDiff_TX28p	AA25	AA26	no
7	IO	TrueDiff_TX28n (2)	AA26	AA27	no

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
7	IO		V20	V21	
7	IO	TrueDiff_TX27n (2)	AA23	AA24	no
7	IO	TrueDiff_TX27p	AA24	AA25	no
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO	TrueDiff_TX26p	AB25	AB26	no
7	IO	TrueDiff_TX26n (2)	AB26	AB27	no
7	IO		W21	V20	
7	IO	TrueDiff_TX25n (2)	AB23	AB24	no
7	IO	TrueDiff_TX25p	AB24	AB25	no
-	VCCIO		VCCIO7	VCCIO7	
7	IO	TrueDiff_TX24p	AC25	AC26	no
7	IO	TrueDiff_TX24n (2)	AC26	AC27	no
7	IO		Y21	W21	
7	IO	TrueDiff_TX23n (2)	AC23	AC24	no
7	IO	TrueDiff_TX23p	AC24	AC25	no
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO	TrueDiff_TX22p	AD25	AD26	no
7	IO	TrueDiff_TX22n (2)	AD26	AD27	no
7	IO		AB22	W20	
7	IO	TrueDiff_TX21n (2)	AD23	AD24	no
7	IO	TrueDiff_TX21p	AD24	AD25	no
-	GNDIO		GND	GND	
7	IO	TrueDiff_TX20p	AF24	AE26	no
7	IO	TrueDiff_TX20n (2)	AE24	AE27	no
7	IO	TrueDiff_TX19n (2)	AF23	AE24	no
7	IO	TrueDiff_TX19p	AE23	AE25	no
-	VCCIO		VCCIO7	VCCIO7	
6	IO	FlexDiff_TX01n (2)	AF22	AF25	
6	IO	FlexDiff_TX01p	AE22	AG25	
6	IO	FlexDiff_TX02n (2)	AD22	AG24	
6	IO	FlexDiff_TX02p	AC22	AF24	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX03n (2)	AF21	AD23	
6	IO	FlexDiff_TX03p	AE21	AE23	
6	IO	FlexDiff_TX04n (2)	AD21	AG23	
6	IO	FlexDiff_TX04p	AC21	AF23	
6	IO	FlexDiff_TX05n (2)	AF20	AB22	
-	VCCIO		VCCIO6	VCCIO6	
6	IO	FlexDiff_TX05p	AE20	AC22	
6	IO	FlexDiff_TX06n (2)	AD20	AE22	
6	IO	FlexDiff_TX06p	AC20	AD22	
6	IO	FlexDiff_TX07n (2)	AB20	AF22	
6	IO	FlexDiff_TX07p	AA20	AG22	
6	IO	FlexDiff_TX08n (2)	AF19	AC21	
6	IO	FlexDiff_TX08p	AE19	AB21	
6	IO	FlexDiff_TX09n (2)	AD19	AD21	
6	IO	FlexDiff_TX09p	AC19	AE21	
6	IO	FlexDiff_TX10n (2)	AB19	AG21	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX10p	AA19	AF21	
6	IO	FlexDiff_TX11n (2)	Y19	AB20	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
6	IO	FlexDiff_TX11p	W19	AC20	
6	IO	FlexDiff_TX12n (2)	AF18	AE20	
6	IO	FlexDiff_TX12p	AE18	AD20	
6	IO	FlexDiff_TX13n (2)	AD18	AF20	
6	IO	FlexDiff_TX13p	AC18	AG20	
6	IO	FlexDiff_TX14n (2)	AB18	AC19	
6	IO	FlexDiff_TX14p	AA18	AB19	
6	IO		AA21	Y18	
6	IO		AB21	AA18	
6	VREFC6 (7)		W20	Y17	
-	VCCIO		VCCIO6	VCCIO6	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
6	IO	CDS_ENA (16)	V18	Y16	
6	IO		Y20	AA17	
6	IO	FlexDiff_TX15p	Y18	AD19	
6	IO	FlexDiff_TX15n (2)	W18	AE19	
6	IO	FlexDiff_TX16p	AF17	AG19	
-	VCCIO		VCCIO6	VCCIO6	
6	IO	FlexDiff_TX16n (2)	AE17	AF19	
6	IO	FlexDiff_TX17p	AD17	AC18	
6	IO	FlexDiff_TX17n (2)	AC17	AB18	
6	IO	FlexDiff_TX18p	AB17	AE18	
6	IO	FlexDiff_TX18n (2)	AA17	AD18	
6	IO	FlexDiff_TX19p	Y17	AB17	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX19n (2)	W17	AC17	
6	IO	FlexDiff_TX20p	AF16	AE17	
6	IO	FlexDiff_TX20n (2)	AE16	AD17	
6	IO	FlexDiff_TX21p	AD16	AF17	
6	IO	FlexDiff_TX21n (2)	AC16	AG17	
6	IO	FlexDiff_TX22p	AB16	AB16	
6	IO	FlexDiff_TX22n (2)	AA16	AC16	
6	IO	FlexDiff_TX23p	Y16	AD16	
6	IO	FlexDiff_TX23n (2)	W16	AE16	
6	IO	FlexDiff_TX24p	AF15	AG16	
-	VCCIO		VCCIO6	VCCIO6	
6	IO	FlexDiff_TX24n (2)	AE15	AF16	
6	IO	FlexDiff_TX25p	AD15	AB15	
6	IO	FlexDiff_TX25n (2)	AC15	AC15	
6	IO	FlexDiff_TX26p	AB15	AE15	
6	IO	FlexDiff_TX26n (2)	AA15	AD15	
6	IO	FlexDiff_TX27p	Y15	AF15	
6	IO	FlexDiff_TX27n (2)	W15	AG15	
6	IO	FlexDiff_TX28p	AD14	AG14	
6	IO	FlexDiff_TX28n (2)	AC14	AF14	
-	VCCIO		VCCIO6	VCCIO6	
5	CONF_DONE (9)		AB14	AA15	
5	nSTATUS (9)		AA14	Y15	
5	FAST4 (17)		Y14	AA16	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
-	GNDIO		GND	GND	
5	FAST3 (17)		Y13	AC14	
5	TCK (9)		AA13	Y14	
5	TMS (9)		AB13	AB14	
-	VCCIO		VCCIO5	VCCIO5	
5	IO	FlexDiff_TX56n (2)	AC13	AD14	
5	IO	FlexDiff_TX56p	AD13	AE14	
5	IO	FlexDiff_TX55n (2)	AE12	AF13	
5	IO	FlexDiff_TX55p	AF12	AG13	
5	IO	FlexDiff_TX54n (2)	AC12	AD13	
5	IO	FlexDiff_TX54p	AD12	AE13	
5	IO	FlexDiff_TX53n (2)	AA12	AB13	
5	IO	FlexDiff_TX53p	AB12	AC13	
5	IO	FlexDiff_TX52n (2)	W12	AF12	
-	VCCIO		VCCIO5	VCCIO5	
5	IO	FlexDiff_TX52p	Y12	AG12	
5	IO	FlexDiff_TX51n (2)	AE11	AD12	
5	IO	FlexDiff_TX51p	AF11	AE12	
5	IO	FlexDiff_TX50n (2)	AC11	AB12	
5	IO	FlexDiff_TX50p	AD11	AC12	
5	IO	FlexDiff_TX49n (2)	AA11	AF11	
5	IO	FlexDiff_TX49p	AB11	AG11	
5	IO	FlexDiff_TX48n (2)	W11	AD11	
5	IO	FlexDiff_TX48p	Y11	AE11	
5	IO	FlexDiff_TX47n (2)	AE10	AB11	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX47p	AF10	AC11	
5	IO	FlexDiff_TX46n (2)	AC10	AD10	
5	IO	FlexDiff_TX46p	AD10	AE10	
5	IO	FlexDiff_TX45n (2)	AA10	AB10	
5	IO	FlexDiff_TX45p	AB10	AC10	
5	IO	FlexDiff_TX44n (2)	W10	AF9	
5	IO	FlexDiff_TX44p	Y10	AG9	
5	IO	FlexDiff_TX43n (2)	AE9	AD9	
5	IO	FlexDiff_TX43p	AF9	AE9	
5	IO		Y7	Y13	
5	IO		AA6	AA13	
-	VCCIO		VCCIO5	VCCIO5	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
5	VREFC5 (7)		V10	AA12	
-	VCCIO		VCCIO5	VCCIO5	
5	IO		AB6	AA11	
5	IO		AB5	Y12	
5	IO	FlexDiff_TX42p	AC9	AB9	
5	IO	FlexDiff_TX42n (2)	AD9	AC9	
5	IO	FlexDiff_TX41p	AA9	AG8	
5	IO	FlexDiff_TX41n (2)	AB9	AF8	
5	IO	FlexDiff_TX40p	W9	AD8	
5	IO	FlexDiff_TX40n (2)	Y9	AE8	
5	IO	FlexDiff_TX39p	AE8	AC8	
5	IO	FlexDiff_TX39n (2)	AF8	AB8	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
5	IO	FlexDiff_TX38p	AC8	AF7	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX38n (2)	AD8	AG7	
5	IO	FlexDiff_TX37p	AA8	AE7	
5	IO	FlexDiff_TX37n (2)	AB8	AD7	
5	IO	FlexDiff_TX36p	W8	AB7	
5	IO	FlexDiff_TX36n (2)	Y8	AC7	
5	IO	FlexDiff_TX35p	AE7	AG6	
5	IO	FlexDiff_TX35n (2)	AF7	AF6	
5	IO	FlexDiff_TX34p	AC7	AD6	
5	IO	FlexDiff_TX34n (2)	AD7	AE6	
5	IO	FlexDiff_TX33p	AA7	AC6	
-	VCCIO		VCCIO5	VCCIO5	
5	IO	FlexDiff_TX33n (2)	AB7	AB6	
5	IO	FlexDiff_TX32p	AE6	AF5	
5	IO	FlexDiff_TX32n (2)	AF6	AG5	
5	IO	FlexDiff_TX31p	AC6	AE5	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX31n (2)	AD6	AD5	
5	IO	FlexDiff_TX30p	AE5	AF4	
5	IO	FlexDiff_TX30n (2)	AF5	AG4	
5	IO	FlexDiff_TX29p	AC5	AG3	
5	IO	FlexDiff_TX29n (2)	AD5	AF3	
-	VCCIO		VCCIO4	VCCIO4	
4	IO	TrueDiff_RX19p	AF4	AE3	no
4	IO	TrueDiff_RX19n (2)	AE4	AE4	no
4	IO	TrueDiff_RX20n (2)	AF3	AE1	no
4	IO	TrueDiff_RX20p	AE3	AE2	no
-	GNDIO		GND	GND	
4	IO	TrueDiff_RX21p	AD3	AD3	no
4	IO	TrueDiff_RX21n (2)	AD4	AD4	no
4	IO		AA5	W8	
4	IO	TrueDiff_RX22n (2)	AD1	AD1	no
4	IO	TrueDiff_RX22p	AD2	AD2	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO	TrueDiff_RX23p	AC3	AC3	no
4	IO	TrueDiff_RX23n (2)	AC4	AC4	no
4	IO		Y5	W7	
4	IO	TrueDiff_RX24n (2)	AC1	AC1	no
4	IO	TrueDiff_RX24p	AC2	AC2	no
-	VCCIO		VCCIO4	VCCIO4	
4	IO	TrueDiff_RX25p	AB3	AB3	no
4	IO	TrueDiff_RX25n	AB4	AB4	no
4	IO		Y6	V8	
4	IO	TrueDiff_RX26n (2)	AB1	AB1	no
4	IO	TrueDiff_RX26p	AB2	AB2	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO	TrueDiff_RX27p	AA3	AA3	no
4	IO	TrueDiff_RX27n (2)	AA4	AA4	no
4	IO		W5	V7	
4	IO	TrueDiff_RX28n (2)	AA1	AA1	no

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
4	IO	TrueDiff_RX28p	AA2	AA2	no
-	GNDIO		GND	GND	
4	IO	TrueDiff_RX29p	Y3	Y3	no
4	IO	TrueDiff_RX29n (2)	Y4	Y4	no
4	IO		W6	W6	
4	IO	TrueDiff_RX30n (2)	Y1	Y1	no
4	IO	TrueDiff_RX30p	Y2	Y2	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO	TrueDiff_RX31p	W3	W3	no
4	IO	TrueDiff_RX31n (2)	W4	W4	no
4	IO		W7	U8	
4	IO	TrueDiff_RX32n (2)	W1	W1	no
4	IO	TrueDiff_RX32p	W2	W2	no
-	VCCIO		VCCIO4	VCCIO4	
4	IO	TrueDiff_RX33p	V3	V3	no
4	IO	TrueDiff_RX33n (2)	V4	V4	no
4	IO		V8	U7	
4	IO	TrueDiff_RX34n (2)	V1	U3	no
4	IO	TrueDiff_RX34p	V2	U4	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO	TrueDiff_RX35p	U3	U1	no
4	IO	TrueDiff_RX35n	U4	U2	no
4	IO		V9	V9	
4	IO	TrueDiff_RX36n	U1	T1	no
4	IO	TrueDiff_RX36p	U2	T2	no
-	GNDIO		GND	GND	
4	IO		U9	W5	
4	IO		U8	T7	
4	IO		U10	T8	
4	IO	RXCLK_IN2n (2)	R3	R1	no
4	IO	RXCLK_IN2p	R4	R2	no
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		T8	U5	
4	IO	RXLOCK2 (5)	U7	V6	
4	IO		T9	U10	
4	IO		R8	U6	
4	IO		T10	U9	
4	VREFC4 (7)		V7	T9	
-	GND_CKLK7 (8)		U6	R8	
-	GND_CKLK7 (8)		V5	T10	
-	VCCIO		VCCIO4	VCCIO4	
-	VCC_CKLK7 (8)		V6	R9	
-	VCC_CKLKA (15)		U5	T6	
4	IO		R9	R7	
4	IO		R10	Y5	
4	IO	LOCK1 (5)	T7	T5	
4	IO		P8	R6	
4	IO		P9	R5	
-	VCC_CKLK1 (8)		T6	R10	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
-	GND_CKLK1 (8)		R6	P8	
-	GNDIO		GND	GND	
4	IO	CLKLK_FB1n (2)	R1	T3	
10	CLKLK_FB1p (9), (10)		R2	T4	
4	IO	CLK3n (2)	P4	R4	
4	CLK3p		P3	R3	
4	IO	CLK1n (2)	P2	P4	
-	VCCIO		VCCIO4	VCCIO4	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
4	nCONFIG (9)		P7	P6	
4	PLL_ENA (9), (18)		R7	P7	
-	VCCSEL (9), (19)		P6	P5	
4	CLK1p		P1	P3	
4	MSEL1 (9)		M7	N5	
4	MSEL0 (9)		N7	P9	
-	GNDIO		GND	GND	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	VCC_CKOUT1 (13)		M6	P10	
-	GND_CKOUT1 (13)		N6	N6	
10	CLKLK_OUT1p (9), (14)		N4	P2	
3	IO	CLKLK_OUT1n (2)	N3	P1	
-	VCC_CKLK3 (8)		K5	N7	
-	VCCIO		VCCIO3	VCCIO3	
-	GND_CKLK3 (8)		L6	N8	
3	IO		N8	M5	
3	IO	CLK5n (2)	N1	N3	
3	CLK5p		N2	N4	
3	IO	LOCK3 (5)	L7	L6	
3	IO		N9	M6	
-	GNDIO		GND	GND	
-	GND_CKLK5 (8)		J6	M7	
-	GND_CKLK5 (8)		J5	N9	
-	VCC_CKLK5 (8)		K6	N10	
3	VREFC3 (7)		J7	M10	
3	IO	CLK7n (2)	M4	M4	
3	CLK7p		M3	M3	
3	IO		L9	M9	
3	IO		M9	K6	
3	IO		M8	L5	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	RXCLK_IN1p	M2	N2	no
3	IO	RXCLK_IN1n (2)	M1	N1	no
3	IO		L8	M8	
3	IO	RXLOCK1 (5)	K7	L7	
3	IO		K8	J5	
-	VCCIO		VCCIO3	VCCIO3	
3	IO	TrueDiff_RX18p	K2	M2	no
3	IO	TrueDiff_RX18n (2)	K1	M1	no
3	IO		K9	L9	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
3	IO	TrueDiff_RX17n (2)	K4	L2	no
3	IO	TrueDiff_RX17p	K3	L1	no
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	TrueDiff_RX16p	J2	L4	no
3	IO	TrueDiff_RX16n (2)	J1	L3	no
3	IO		J8	K9	
3	IO	TrueDiff_RX15n (2)	J4	K4	no
3	IO	TrueDiff_RX15p	J3	K3	no
-	GNDIO		GND	GND	
3	IO	TrueDiff_RX14p	H2	J2	no
3	IO	TrueDiff_RX14n (2)	H1	J1	no
3	IO		H7	L8	
3	IO	TrueDiff_RX13n (2)	H4	J4	no
3	IO	TrueDiff_RX13p	H3	J3	no
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	TrueDiff_RX12p	G2	H2	no
3	IO	TrueDiff_RX12n (2)	G1	H1	no
3	IO		H6	J6	
3	IO	TrueDiff_RX11n (2)	G4	H4	no
3	IO	TrueDiff_RX11p	G3	H3	no
-	VCCIO		VCCIO3	VCCIO3	
3	IO	TrueDiff_RX10p	F2	G2	no
3	IO	TrueDiff_RX10n (2)	F1	G1	no
3	IO		G6	K7	
3	IO	TrueDiff_RX09n (2)	F4	G4	no
3	IO	TrueDiff_RX09p	F3	G3	no
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	TrueDiff_RX08p	E2	F2	no
3	IO	TrueDiff_RX08n (2)	E1	F1	no
3	IO		G5	K8	
3	IO	TrueDiff_RX07n (2)	E4	F4	no
3	IO	TrueDiff_RX07p	E3	F3	no
-	GNDIO		GND	GND	
3	IO	TrueDiff_RX06p	D2	E2	no
3	IO	TrueDiff_RX06n (2)	D1	E1	no
3	IO		H5	J7	
3	IO	TrueDiff_RX05n (2)	D4	E4	no
3	IO	TrueDiff_RX05p	D3	E3	no
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	TrueDiff_RX04p	C2	D2	no
3	IO	TrueDiff_RX04n (2)	C1	D1	no
3	IO		F5	J8	
3	IO	TrueDiff_RX03n (2)	C4	D4	no
3	IO	TrueDiff_RX03p	C3	D3	no
-	VCCIO		VCCIO3	VCCIO3	
3	IO	TrueDiff_RX02p	A3	C2	no
3	IO	TrueDiff_RX02n (2)	B3	C1	no
3	IO	TrueDiff_RX01n (2)	A4	C4	no
3	IO	TrueDiff_RX01p	B4	C3	no

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
-	VCCIO		VCCIO2	VCCIO2	
2	IO	FlexDiff_RX29n (2)	C5	A3	
2	IO	FlexDiff_RX29p	D5	B3	
2	IO	FlexDiff_RX30n (2)	A5	A4	
2	IO	FlexDiff_RX30p	B5	B4	
2	IO	FlexDiff_RX31n (2)	C6	C5	
2	IO	FlexDiff_RX31p	D6	D5	
2	IO	FlexDiff_RX32n (2)	A6	A5	
2	IO	FlexDiff_RX32p	B6	B5	
2	IO	FlexDiff_RX33n (2)	E7	E6	
-	GNDIO		GND	GND	
2	IO	FlexDiff_RX33p	F7	F6	
2	IO	FlexDiff_RX34n (2)	C7	C6	
2	IO	FlexDiff_RX34p	D7	D6	
2	IO	FlexDiff_RX35n (2)	A7	A6	
2	IO	FlexDiff_RX35p	B7	B6	
2	IO	FlexDiff_RX36n (2)	G8	E7	
2	IO	FlexDiff_RX36p	H8	F7	
2	IO	FlexDiff_RX37n (2)	E8	C7	
2	IO	FlexDiff_RX37p	F8	D7	
2	IO	FlexDiff_RX38n (2)	C8	A7	
-	VCCIO		VCCIO2	VCCIO2	
2	IO	FlexDiff_RX38p	D8	B7	
2	IO	FlexDiff_RX39n (2)	A8	E8	
2	IO	FlexDiff_RX39p	B8	F8	
2	IO	FlexDiff_RX40n (2)	G9	C8	
2	IO	FlexDiff_RX40p	H9	D8	
2	IO	FlexDiff_RX41n (2)	E9	A8	
2	IO	FlexDiff_RX41p	F9	B8	
2	IO	FlexDiff_RX42n (2)	C9	E9	
2	IO	FlexDiff_RX42p	D9	F9	
2	IO		E6	G11	
2	IO		E5	L10	
2	VREFC2 (7)		J9	H11	
-	GNDIO		GND	GND	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	VCCIO		VCCIO2	VCCIO2	
2	IO		G7	G12	
2	IO		F6	H12	
2	IO	FlexDiff_RX43p	A9	C9	
2	IO	FlexDiff_RX43n (2)	B9	D9	
2	IO	FlexDiff_RX44p	G10	A9	
-	GNDIO		GND	GND	
2	IO	FlexDiff_RX44n (2)	H10	B9	
2	IO	FlexDiff_RX45p	E10	E10	
2	IO	FlexDiff_RX45n (2)	F10	F10	
2	IO	FlexDiff_RX46p	C10	C10	
2	IO	FlexDiff_RX46n (2)	D10	D10	
2	IO	FlexDiff_RX47p	A10	E11	
-	VCCIO		VCCIO2	VCCIO2	
2	IO	FlexDiff_RX47n (2)	B10	F11	
2	IO	FlexDiff_RX48p	G11	C11	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
2	IO	FlexDiff_RX48n (2)	H11	D11	
2	IO	FlexDiff_RX49p	E11	A11	
2	IO	FlexDiff_RX49n (2)	F11	B11	
2	IO	FlexDiff_RX50p	C11	E12	
2	IO	FlexDiff_RX50n (2)	D11	F12	
2	IO	FlexDiff_RX51p	A11	C12	
2	IO	FlexDiff_RX51n (2)	B11	D12	
2	IO	FlexDiff_RX52p	G12	A12	
-	GNDIO		GND	GND	
2	IO	FlexDiff_RX52n (2)	H12	B12	
2	IO	FlexDiff_RX53p	E12	E13	
2	IO	FlexDiff_RX53n (2)	F12	F13	
2	IO	FlexDiff_RX54p	C12	C13	
2	IO	FlexDiff_RX54n (2)	D12	D13	
2	IO	FlexDiff_RX55p	A12	A13	
2	IO	FlexDiff_RX55n (2)	B12	B13	
2	IO	FlexDiff_RX56p	C13	C14	
2	IO	FlexDiff_RX56n (2)	D13	D14	
-	VCCIO		VCCIO2	VCCIO2	
1	TRST (9)		E13	H13	
1	nCEO (9)		F13	G13	
1	FAST1 (17)		G13	E14	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	VCCIO		VCCIO1	VCCIO1	
1	FAST2 (17)		G14	H14	
1	TDO (9)		F14	F14	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
1	IO	FlexDiff_RX28n (2)	D14	B14	
1	IO	FlexDiff_RX28p	C14	A14	
1	IO	INIT_DONE/FlexDiff_RX27n (2), (4)	H15	B15	
1	IO	FlexDiff_RX27p	G15	A15	
1	IO	FlexDiff_RX26n (2)	F15	D15	
1	IO	RDYnBSY/FlexDiff_RX26p (3)	E15	C15	
1	IO	FlexDiff_RX25n (2)	D15	F15	
1	IO	FlexDiff_RX25p	C15	E15	
1	IO	CLKUSR/FlexDiff_RX24n (2), (3)	B15	B16	
-	GNDIO		GND	GND	
1	IO	FlexDiff_RX24p	A15	A16	
1	IO	FlexDiff_RX23n (2)	H16	D16	
1	IO	FlexDiff_RX23p	G16	C16	
1	IO	FlexDiff_RX22n (2)	F16	F16	
1	IO	DATA1/FlexDiff_RX22p	E16	E16	
1	IO	FlexDiff_RX21n (2)	D16	B17	
1	IO	FlexDiff_RX21p	C16	A17	
1	IO	FlexDiff_RX20n (2)	B16	D17	
1	IO	FlexDiff_RX20p	A16	C17	
1	IO	FlexDiff_RX19n (2)	H17	F17	
-	VCCIO		VCCIO1	VCCIO1	
1	IO	FlexDiff_RX19p	G17	E17	
1	IO	FlexDiff_RX18n (2)	F17	D18	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
1	IO	FlexDiff_RX18p	E17	C18	
1	IO	FlexDiff_RX17n (2)	D17	F18	
1	IO	FlexDiff_RX17p	C17	E18	
1	IO	FlexDiff_RX16n (2)	B17	B19	
1	IO	FlexDiff_RX16p	A17	A19	
1	IO	FlexDiff_RX15n (2)	H18	D19	
1	IO	FlexDiff_RX15p	G18	C19	
1	IO		G20	G16	
1	IO	DATA2 (3)	H20	H15	
-	GNDIO		GND	GND	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
1	VREFC1 (7)		E22	H17	
-	VCCIO		VCCIO1	VCCIO1	
1	IO		F21	H16	
1	IO		E21	G17	
1	IO	DATA3/FlexDiff_RX14p (3)	F18	F19	
1	IO	FlexDiff_RX14n (2)	E18	E19	
1	IO	FlexDiff_RX13p	D18	B20	
1	IO	FlexDiff_RX13n (2)	C18	A20	
1	IO	FlexDiff_RX12p	B18	D20	
1	IO	FlexDiff_RX12n (2)	A18	C20	
1	IO	FlexDiff_RX11p	H19	F20	
1	IO	FlexDiff_RX11n (2)	G19	E20	
1	IO	FlexDiff_RX10p	F19	B21	
-	VCCIO		VCCIO1	VCCIO1	
1	IO	FlexDiff_RX10n (2)	E19	A21	
1	IO	FlexDiff_RX09p	D19	D21	
1	IO	FlexDiff_RX09n (2)	C19	C21	
1	IO	FlexDiff_RX08p	B19	F21	
1	IO	FlexDiff_RX08n (2)	A19	E21	
1	IO	FlexDiff_RX07p	F20	B22	
1	IO	FlexDiff_RX07n (2)	E20	A22	
1	IO	FlexDiff_RX06p	D20	D22	
1	IO	FlexDiff_RX06n (2)	C20	C22	
1	IO	FlexDiff_RX05p	B20	F22	
-	GNDIO		GND	GND	
1	IO	FlexDiff_RX05n (2)	A20	E22	
1	IO	FlexDiff_RX04p	D21	B23	
1	IO	FlexDiff_RX04n (2)	C21	A23	
1	IO	FlexDiff_RX03p	B21	D23	
1	IO	DATA5/FlexDiff_RX03n (1), (2)	A21	C23	
1	IO	FlexDiff_RX02p	D22	B24	
1	IO	FlexDiff_RX02n (2)	C22	A24	
1	IO	FlexDiff_RX01p	B22	B25	
1	IO	DATA4/FlexDiff_RX01n (1), (2)	A22	A25	
-	VCCIO		VCCIO1	VCCIO1	
	VCCINT		J10	L11	
	VCCINT		J11	L13	
	VCCINT		J12	L15	
	VCCINT		J13	L17	
	VCCINT		J14	V18	
	VCCINT		J15	J18	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
	VCCINT		J16	J12	
	VCCINT		J17	W16	
	VCCINT		J18	K11	
	VCCINT		K10	M12	
	VCCINT		K17	M14	
	VCCINT		K18	M16	
	VCCINT		L5	K17	
	VCCINT		L10	K13	
	VCCINT		L17	N13	
	VCCINT		M5	N15	
	VCCINT		M10	V13	
	VCCINT		M17	W10	
	VCCINT		M22	J10	
	VCCINT		N10	P12	
	VCCINT		N17	P16	
	VCCINT		P10	W18	
	VCCINT		P17	K15	
	VCCINT		R5	R13	
	VCCINT		R11	R15	
	VCCINT		R17	V15	
	VCCINT		R22	V11	
	VCCINT		T5	T12	
	VCCINT		T11	T14	
	VCCINT		T17	T16	
	VCCINT		U11	V17	
	VCCINT		U17	U17	
	VCCINT		V11	U11	
	VCCINT		V12	U13	
	VCCINT		V13	U15	
	VCCINT		V14		
	VCCINT		V15		
	VCCINT		V16		
	VCCINT		V17		
	VCCIO8		B26	B27	
	VCCIO8		L26	K26	
	VCCIO8		M21	N17	
	VCCIO8			K18	
	VCCIO7		N21	AF27	
	VCCIO7		T26	R17	
	VCCIO7		AE26	V26	
	VCCIO7			W19	
	VCCIO6		W14	AF18	
	VCCIO6		AF14	AG26	
	VCCIO6		AF25	W15	
	VCCIO6			Y20	
	VCCIO5		W13	AF10	
	VCCIO5		AF2	AG2	
	VCCIO5		AF13	W13	
	VCCIO5			Y8	
	VCCIO4		T1	AF1	
	VCCIO4		T2	R11	
	VCCIO4		AE1	V2	
	VCCIO4			V10	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
	VCCIO3		B1	B1	
	VCCIO3		L1	K2	
	VCCIO3		L2	N11	
	VCCIO3			K10	
	VCCIO2		A2	A2	
	VCCIO2		A13	B10	
	VCCIO2		H13	J13	
	VCCIO2			H8	
	VCCIO1		A14	A26	
	VCCIO1		A25	B18	
	VCCIO1		H14	J15	
	VCCIO1			H20	
	GND		B2	J14	
	GND		B13	J16	
	GND		B14	K12	
	GND		B25	L12	
	GND		E14	G15	
	GND		K11	L14	
	GND		K12	L16	
	GND		K13	K16	
	GND		K14	W12	
	GND		K15	M11	
	GND		K16	M13	
	GND		L3	M15	
	GND		L4	M17	
	GND		L11	W14	
	GND		L12	J11	
	GND		L13	N12	
	GND		L14	N16	
	GND		L15	J17	
	GND		L16	K14	
	GND		L25	P11	
	GND		M11	P17	
	GND		M12	V14	
	GND		M13	W11	
	GND		M14	R12	
	GND		M15	R16	
	GND		M16	W17	
	GND		N5	J9	
	GND		N11	T11	
	GND		N12	T13	
	GND		N13	T15	
	GND		N14	T17	
	GND		N15	V16	
	GND		N16	V12	
	GND		N22	U12	
	GND		P5	U14	
	GND		P11	U16	
	GND		P12	A1	
	GND		P13	A10	
	GND		P14	A18	
	GND		P15	A27	
	GND		P16	B2	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
	GND		P22	B26	
	GND		R12	E5	
	GND		R13	E23	
	GND		R14	G14	
	GND		R15	K1	
	GND		R16	K5	
	GND		T3	K23	
	GND		T4	K27	
	GND		T12	V1	
	GND		T13	V5	
	GND		T14	V23	
	GND		T15	V27	
	GND		T16	AA14	
	GND		T25	AC5	
	GND		U12	AC23	
	GND		U13	AF2	
	GND		U14	AF26	
	GND		U15	AG1	
	GND		U16	AG10	
	GND		AE2	AG18	
	GND		AE13	AG27	
	GND		AE14	AA7	
	GND		AE25	AA21	
	GND			G7	
	GND			G21	
	GND			W9	
	GND			J19	
	NC			G8	
	NC			G9	
	NC			G10	
	NC			H9	
	NC			H10	
	NC			G18	
	NC			G19	
	NC			G20	
	NC			H18	
	NC			H19	
	NC			Y9	
	NC			Y10	
	NC			AA8	
	NC			AA9	
	NC			Y11	
	NC			Y19	
	NC			AA10	
	NC			AA19	
	NC			AA20	
	NC			F5	
	NC			G5	
	NC			G6	
	NC			H5	
	NC			H6	
	NC			H7	
	NC			F23	
	NC			G22	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support
	NC			G23	
	NC			H21	
	NC			H22	
	NC			H23	
	NC			J23	
	NC			Y23	
	NC			Y6	
	NC			Y7	
	NC			AA5	
	NC			AA6	
	NC			AB5	
	NC			Y21	
	NC			Y22	
	NC			J22	
	NC			AA22	
	NC			AA23	
	NC			AB23	
Total User I/O Pins (20)			492	492	

Table 1. EP2A15 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	HSTL Class II Output Support

Notes:

(1) The pins marked "no" in this column do not support the HSTL Class II output standard. All the unmarked pins support HSTL class II output in addition to other I/O standards.
(2) This pin is the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the differential channel. Pins with "pins" suffix carry the positive signal for the differential channel.
(3) This pin can be used as a user I/O pin after configuration.
(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(5) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock remains clocking. The LOCK function is optional, if the LOCK output is not used, this pin is a user I/O pin.
(6) Dedicated external clock output from one of the two LVDS TX PLLs. TXCLK_OUT1p is from TXPLL1, TXCLK_OUT2p is from TXPLL2.
(7) This pin is the dedicated power pin of VREF Control circuits (In addition to the program able VREF pins) for each of the I/O banks. This pin can be connected to 2.5 V or 3.3 V if a voltage referenced I/O standard is used. Otherwise, it can be connected to 1.8 V, 2.5 V, or 3.3 V.
(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To insure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuity should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as VCCINT and should be connected to a 1.5-V power supply. If the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as VCCINT and should be connected to a 1.5 V power supply. If the ClockLock and ClockBoost circuitry is not used, this power or ground pin should be connected to the VCCINT or GND, respectively.
(9) This pin is a dedicated pin; it is not available as a user I/O pin.
(10) Dedicated external clock feedback from the general-purpose PLLs. CLK_FB1p feeds PLL2. The external clock feedback must use the same I/O standard as the external clock output and the global clock input to the general.-purpose PLL. If this pin feature is not used, it should be connected to GND on the board.
(11) Dedicated input that is used to control whether weak active pull-up resistors are on for all I/O pins during power-up and configuration. A "0" means active pull-up resistors are enabled, a "1" (1.5 V, 1.8 V, 2.5 V, 3.3 V) means they are disabled.
(12) This pin is tri-stated in user mode.
(13) This pin is power or ground (Bank #9 and #10 in the Quartus II software) for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock output. To insure noise resistance, the power and ground supply to the Pll external output should be isolated from power and ground to the rest of the device. If the PLL or external output is not used, this power and ground pin should be connected to VCCIO or GND respectively.
(14) Dedicated external clock output from the general-purpose PLLs. CLKLK_OUT1p is from PLL1, CLKLD_OUT2p is from PLL2. Each dedicated clock output has its own VVVIO power for output standard selection. If this pin feature is not used, it should be connected to GND on the board.
(15) This pin is a dedicated power pin for the ClockLock and ClockBoost circuitry. It should be connected to the highest voltage level on the device. If possible, do not connect this pin to a noisy VCCIO pin.
(16) This is a dual-purpose pin for enabling the clock data synchronization (CDS) circuitry.
(17) This pin is a dedicated pin for driving the global fast lines within the entire device.
(18) This pin is a dedicated input pin that is the active high enable pin for all of the PLL circuits in the device. When de-asserted (low), all PLLs are reset to their default unlocked state and will stop clocking. Once re-asserted (can be 1.5 V, 1.8 V, 2.5 V, 3.3 V but should be the same as the VCCIO for that bank), the PLLs will lock again and start clocking. This PLL enable control can be selected on a per PLL basis. If this pin feature is not used, it should be connected to GND on the board.
(19) Dedicated input that is used to choose whether programming input pins can accept 3.3 V, 2.5 V, or 1.8 V during configuration. A high (1.5 V, 1.8 V, 2.5 V, 3.3 V) means 1.8 V, and a "0" means 2.5 V/3.3 V. VCCSEL can select the input buffer type for the programming and configuration input pins, including PLL_ENA, before and during configuration and also in user mode.
(20) The user I/O pin count includes 4 dedicated inputs and 8 dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Table 2 provides descriptions for all power, HSDI, and general-purpose PLL related pins.

Table 2. Power, HSDI & General-Purpose PLL Pins

Pin Name	Pin Description
TrueDiff_RX[1..36]	Dual-purpose HSDI receiver channels 1 through 36. If not used, these pins are regular I/O pins.
TrueDiff_TX[1..36]	Dual-purpose HSDI transmitter channels 1 through 36. If not used, these pins are regular I/O pins.
FlexDiff_RX[1..56]	Dual-purpose Flexible-LVDS receiver channels 1 through 56. If not used, these pins are regular I/O pins.
FlexDiff_TX[1..56]	Dual-purpose Flexible-LVDS transmitter channels 1 through 56. If not used, these pins are regular I/O pins.
RXLOCK1	Dual-purpose pin for lock output of RX PLL1. If the PLL is not used, then this is a regular I/O pin.
RXLOCK2	Dual-purpose pin for lock output of RX PLL2. If the PLL is not used, then this is a regular I/O pin.
TXLOCK1	Dual-purpose pin for lock output of TX PLL1. If the PLL is not used, then this is a regular I/O pin.
TXLOCK2	Dual-purpose pin for lock output of TX PLL2. If the PLL is not used, then this is a regular I/O pin.
RXCLK_IN1	Dual-purpose clock input pin for RX PLL1.
RXCLK_IN2	Dual-purpose clock input pin for RX PLL2.
TXCLK_OUT1	Dual-purpose clock output pin for TXPLL1.
TXCLK_OUT2	Dual-purpose clock output pin for TXPLL2.
FAST [1..4]	Dedicated pins for driving the global fast lines within the entire device.
CLK1p	Dedicated global clock input.
CLK1n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK1p input.
CLK2p	Dedicated global clock input.
CLK2n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK2p input.
CLK3p	Dedicated global clock input.
CLK3n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK3p input.
CLK4p	Dedicated global clock input.
CLK4n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK4p input.
CLK5p	Dedicated global clock input.
CLK5n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK5p input.
CLK6p	Dedicated global clock input.
CLK6n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK6p input.
CLK7p	Dedicated global clock input.
CLK7n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK7p input.
CLK8p	Dedicated global clock input.
CLK8n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK8p input.
Lock1	Dual-purpose pin for Lock output of general-purpose PLL1. If the PLL is not used, then this is a regular I/O pin.
Lock2	Dual-purpose pin for Lock output of general-purpose PLL2. If the PLL is not used, then this is a regular I/O pin.
Lock3	Dual-purpose pin for Lock output of general-purpose PLL3. If the PLL is not used, then this is a regular I/O pin.
Lock4	Dual-purpose pin for Lock output of general-purpose PLL4. If the PLL is not used, then this is a regular I/O pin.
CLKLK_FB1	Dual-purpose external feedback pin for general-purpose PLL1.
CLKLK_FB2	Dual-purpose external feedback pin for general-purpose PLL2.
CLKLK_OUT1	Dual-purpose external clock output pin for general-purpose PLL1.
CLKLK_OUT2	Dual-purpose external clock output pin for general-purpose PLL2.
VCCSEL	Dedicated input that is used to choose whether programming input pins can accept 3.3 V, 2.5 V, or 1.8 V during configuration. A high (1.5 V, 1.8 V, 2.5 V, 3.3 V) means 1.8 V, and a “0” means 2.5 V/3.3 V. VCCSEL can select the input buffer type for the programming and configuration input pins, including PLL_ENA, before and during configuration and also in user mode.

Table 2. Power, HSDI & General-Purpose PLL Pins

Pin Name	Pin Description
VCCINT	Internal core voltage.
VCCIO [1...8]	I/O and configuration pin voltage for I/O banks, these can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
VCC_CKLK [1...4]	Digital power for the four general-purpose PLLs.
VCC_CKLK [5, 7]	Digital power for the high-speed receiver PLLs 1 and 2, respectively.
VCC_CKLK [6, 8]	Digital power for the high-speed transmitter PLLs 1 and 2, respectively.
VCC_CKOUT [1, 2]	External clock output buffer power for CLKLK_OUT1 and CLKCL_OUT2 of PLL1 and PLL2.
VREFC [1...8]	VREF control the circuit's dedicated power pin for each of the I/O banks. This pin can be connected to 2.5 V, or 3.3 V if a voltage referenced I/O standard is used. Otherwise, it can be connected to 1.8 V, 2.5 V, or 3.3 V.