| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | VCCD_PLL7 | | | K25 | | | | | | | |
| | | VCCA_PLL7 | | | J26 | | | | | | | |
| | | GNDA_PLL7 | | | K26 | | | | | | | |
| | | GNDA_PLL7 | | | J25 | | | | | | | |
| B2 | VREFB2N0 | FPLL7CLKp | INPUT | | C34 | | | | | | | |
| B2 | VREFB2N0 | FPLL7CLKn | INPUT | | C33 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX41p | | J28 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX41n | | K27 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX40p | | E34 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX40n | | D34 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX40p | | J30 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX40n | | J29 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX39p | | F32 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX39n | | F31 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX39p | | K30 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX39n | | K29 | | | | | | | |
| B2 | VREFB2N0 | VREFB2N0 | VREFB2N0 | | R30 | T21 | J18 | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX38p | | F34 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX38n | | F33 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX38p | | L26 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX38n | | L25 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX37p | | G33 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX37n | | G32 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX37p | | M26 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX37n | | M25 | | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX36p | | H32 | C28 | B20 | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX36n | | H31 | C27 | B19 | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX36p | | K28 | H23 | D19 | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX36n | | L28 | H22 | D18 | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX35p | | G34 | D28 | A17 | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_RX35n | | H34 | D27 | B17 | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_TX35p | | L29 | F24 | C20 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B2 | VREFB2N0 | IO | DIFFIO_TX35n | | M29 | F23 | C19 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX34p | | J32 | F27 | A19 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX34n | | J31 | F26 | A18 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX34p | | M28 | G24 | D20 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX34n | | M27 | G23 | E20 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX33p | | J34 | E28 | A21 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX33n | | J33 | F28 | A20 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX33p | | N27 | E26 | F20 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX33n | | N26 | E25 | F19 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX32p | | K33 | G28 | B22 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX32n | | K32 | G27 | A22 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX32p | | N25 | K24 | G19 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX32n | | N24 | J23 | G18 | | | | | |
| B2 | VREFB2N1 | VREFB2N1 | VREFB2N1 | | M30 | M23 | H19 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX31p | | L32 | J27 | C22 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX31n | | L31 | J26 | C21 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX31p | | N23 | K22 | F18 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX31n | | P23 | K21 | F17 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX30p | | L34 | H28 | D22 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX30n | | K34 | J28 | D21 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX30p | | N29 | K23 | G17 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX30n | | N28 | L23 | G16 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX29p | | M32 | L26 | E22 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX29n | | M31 | L25 | F22 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX29p | | P29 | G26 | H16 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX29n | | P28 | G25 | J16 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX28p | | M34 | K28 | F21 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_RX28n | | M33 | K27 | G21 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX28p | | R29 | M22 | K15 | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_TX28n | | R28 | M21 | K14 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX27p | | N31 | M27 | G20 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX27n | | N30 | M26 | H20 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B2 | VREFB2N2 | IO | DIFFIO_TX27p | | R23 | J25 | J17 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX27n | | T23 | J24 | K16 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX26p | | N33 | L28 | G22 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX26n | | N32 | M28 | H22 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX26p | | T29 | H26 | L16 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX26n | | T28 | H25 | L15 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX25p | | P32 | N28 | J22 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX25n | | P31 | P28 | J21 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX25p | | U24 | K26 | M14 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX25n | | U23 | K25 | N14 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX24p | | N34 | N26 | J20 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX24n | | P34 | N25 | J19 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX24p | | U31 | M25 | M16 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX24n | | U30 | M24 | M15 | | | | | |
| B2 | VREFB2N2 | VREFB2N2 | VREFB2N2 | | K31 | F25 | E19 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX23p | | R32 | P27 | K22 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX23n | | R31 | P26 | K21 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX23p | | U29 | P25 | K20 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX23n | | U28 | P24 | K19 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX22p | | R34 | R28 | L22 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX22n | | R33 | T28 | L21 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX22p | | W29 | M20 | N16 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX22n | | V29 | N20 | N15 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX21p | | T32 | T27 | L20 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_RX21n | | T31 | T26 | L19 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX21p | | U27 | R21 | P16 | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_TX21n | | V28 | R20 | P15 | | | | | |
| B2 | VREFB2N2 | IO | CLK0n/DIFFIO_RX_C0n | | T34 | R25 | M21 | | | | | |
| B2 | VREFB2N2 | IO | CLK0p/DIFFIO_RX_C0p | | U34 | R26 | M22 | | | | | |
| B2 | VREFB2N2 | CLK1n | INPUT | | U32 | T24 | M19 | | | | | |
| B2 | VREFB2N2 | CLK1p | INPUT | | U33 | T25 | M20 | | | | | |
| | | VCCD_PLL1 | | | R27 | N22 | K17 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | VCCA_PLL1 | | | T25 | N23 | K18 | | | | | |
| | | GNDA_PLL1 | | | T26 | P23 | L17 | | | | | |
| | | GNDA_PLL1 | | | R26 | P22 | L18 | | | | | |
| | | GNDA_PLL2 | | | W26 | R23 | M17 | | | | | |
| | | GNDA_PLL2 | | | V26 | R22 | M18 | | | | | |
| | | VCCA_PLL2 | | | V25 | T23 | N18 | | | | | |
| | | VCCD_PLL2 | | | W27 | T22 | N17 | | | | | |
| B1 | VREFB1N0 | IO | CLK2p/DIFFIO_RX_C1p | | W34 | U28 | N22 | | | | | |
| B1 | VREFB1N0 | IO | CLK2n/DIFFIO_RX_C1n | | V34 | U27 | N21 | | | | | |
| B1 | VREFB1N0 | CLK3p | INPUT | | V32 | U26 | N20 | | | | | |
| B1 | VREFB1N0 | CLK3n | INPUT | | V31 | U25 | N19 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX20p | | W31 | V28 | P22 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX20n | | W30 | W28 | P21 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX20p | | V23 | T19 | T15 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX20n | | W23 | U19 | T14 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX19p | | W33 | Y28 | P20 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX19n | | W32 | AA28 | P19 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX19p | | Y24 | U20 | T16 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX19n | | Y23 | V20 | U16 | | | | | |
| B1 | VREFB1N0 | VREFB1N0 | VREFB1N0 | | AE31 | AD23 | U19 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX18p | | Y32 | W27 | R22 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX18n | | Y31 | W26 | T22 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX18p | | W28 | Y25 | P17 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX18n | | Y29 | Y24 | R16 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX17p | | Y34 | Y27 | T21 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX17n | | Y33 | Y26 | T20 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX17p | | Y28 | U24 | V17 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX17n | | Y27 | U23 | W17 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX16p | | AA32 | V26 | U21 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX16n | | AA31 | V25 | U20 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX16p | | AA29 | AA26 | U18 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX16n | | AA28 | AA25 | U17 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B1 | VREFB1N0 | IO | DIFFIO_RX15p | | AB31 | AB28 | U22 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_RX15n | | AB30 | AB27 | V22 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX15p | | AA23 | V23 | R17 | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_TX15n | | AB23 | V22 | T17 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX14p | | AB33 | AC28 | W22 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX14n | | AB32 | AD28 | W21 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX14p | | AA26 | W21 | W19 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX14n | | AA25 | Y21 | W18 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX13p | | AA34 | AD26 | Y22 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX13n | | AB34 | AD25 | Y21 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX13p | | AB29 | AC25 | Y19 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX13n | | AB28 | AC24 | Y18 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX12p | | AC32 | W25 | AA22 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX12n | | AC31 | W24 | AB22 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX12p | | AB24 | AB22 | V20 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX12n | | AC24 | AB21 | V19 | | | | | |
| B1 | VREFB1N1 | VREFB1N1 | VREFB1N1 | | AC30 | Y23 | R20 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX11p | | AC34 | AC27 | AB21 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX11n | | AC33 | AC26 | AB20 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX11p | | AB26 | AE26 | R19 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX11n | | AB25 | AE25 | T19 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX10p | | AD32 | AB26 | AB19 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX10n | | AD31 | AB25 | AB18 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX10p | | AC27 | AB24 | AB17 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX10n | | AB27 | AB23 | AA17 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX9p | | AE33 | AE28 | AA20 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX9n | | AE32 | AE27 | AA19 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX9p | | AD26 | AC23 | AA16 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX9n | | AD25 | AC22 | Y17 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX8p | | AD34 | AF28 | W20 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_RX8n | | AE34 | AF27 | Y20 | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_TX8p | | AC29 | AA23 | AB16 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B1 | VREFB1N1 | IO | DIFFIO_TX8n | | AC28 | AA22 | AB15 | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX7p | | AF32 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX7n | | AF31 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX7p | | AD29 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX7n | | AD28 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX6p | | AF34 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX6n | | AF33 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX6p | | AE30 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX6n | | AE29 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX5p | | AG32 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX5n | | AG31 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX5p | | AE28 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX5n | | AE27 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX4p | | AG34 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX4n | | AH34 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX4p | | AF30 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX4n | | AF29 | | | | | | | |
| B1 | VREFB1N2 | VREFB1N2 | VREFB1N2 | | Y30 | W23 | P18 | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX3p | | AH33 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX3n | | AH32 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX3p | | AF28 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX3n | | AF27 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX2p | | AJ34 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX2n | | AJ33 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX2p | | AG29 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX2n | | AG28 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX1p | | AJ32 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_RX1n | | AJ31 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX1p | | AH31 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX1n | | AH30 | | | | | | | |
| B1 | VREFB1N2 | FPLL8CLKn | INPUT | | AM33 | | | | | | | |
| B1 | VREFB1N2 | FPLL8CLKp | INPUT | | AM34 | | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B1 | VREFB1N2 | IO | DIFFIO_TX0p | | AH29 | | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_TX0n | | AH28 | | | | | | | |
| | | GNDA_PLL8 | | | AF25 | | | | | | | |
| | | GNDA_PLL8 | | | AE26 | | | | | | | |
| | | VCCA_PLL8 | | | AF26 | | | | | | | |
| | | VCCD_PLL8 | | | AE25 | | | | | | | |
| B8 | VREFB8N0 | TDI | | TDI | AL31 | V19 | AA14 | | | | | |
| B8 | VREFB8N0 | TMS | | TMS | AM32 | W19 | Y16 | | | | | |
| B8 | VREFB8N0 | TCK | | TCK | AE24 | V17 | AB13 | | | | | |
| B8 | VREFB8N0 | TRST | | TRST | AM31 | W17 | AB14 | | | | | |
| B8 | VREFB8N0 | nCONFIG | | nCONFIG | AL30 | V16 | Y15 | | | | | |
| B8 | VREFB8N0 | VCCSEL | | VCCSEL | AF24 | W18 | AB12 | | | | | |
| B8 | VREFB8N0 | IO | | | AL29 | | | | | | | |
| B8 | VREFB8N0 | IO | | CS | AH27 | AE24 | Y14 | | | | | |
| B8 | VREFB8N0 | IO | | CLKUSR | AH26 | AC21 | AA11 | | | | | |
| B8 | VREFB8N0 | IO | | nWS | AG26 | AE22 | AA13 | | | | | |
| B8 | VREFB8N0 | IO | | nRS | AG25 | AE21 | AB11 | | | | | |
| B8 | VREFB8N0 | IO | | | AH24 | | | | | | | |
| B8 | VREFB8N0 | IO | | | AH25 | | | | | | | |
| B8 | VREFB8N0 | IO | DQ17B | | AM30 | AF26 | | DQ8B | DQ3B | | | |
| B8 | VREFB8N0 | IO | | | AN31 | AF25 | | DQ8B | DQ3B | DQ3B | DQ1B | DQ1B |
| B8 | VREFB8N0 | VREFB8N0 | VREFB8N0 | | AK28 | AD22 | W16 | | | | | |
| B8 | VREFB8N0 | IO | DQ17B | | AN32 | AG26 | | DQ8B | DQ3B | DQ3B | DQ1B | |
| B8 | VREFB8N0 | IO | DQ17B | | AP32 | AH25 | | DQ8B | DQ3B | DQ3B | DQ1B | DQ1B |
| B8 | VREFB8N0 | IO | DQ17B | | AP30 | AH26 | | DQ8B | DQ3B | DQ3B | DQ1B | DQ1B |
| B8 | VREFB8N0 | IO | DQS17B | | AP31 | AG25 | | | | | | |
| B8 | VREFB8N0 | IO | | | AE23 | AD20 | W15 | | | | | |
| B8 | VREFB8N0 | IO | | | AF23 | | | | | | | |
| B8 | VREFB8N0 | IO | DQ16B | | AP29 | AE20 | | DQ8B | | DQ3B | | DQ1B |
| B8 | VREFB8N0 | IO | | | AN29 | | | | | DQ3B | | DQ1B |
| B8 | VREFB8N0 | IO | DQ16B | | AM29 | W16 | | DQ8B | | DQ3B | | DQ1B |
| B8 | VREFB8N0 | IO | DQ16B | | AP28 | | | DQ8B | | DQ3B | | DQ1B |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B8 | VREFB8N0 | IO | DQ16B | | AM28 | AC20 | | DQ8B | | DQ3B | | DQ1B |
| B8 | VREFB8N0 | IO | DQS16B | | AN28 | | | DQS8B | | | | |
| B8 | VREFB8N0 | IO | | | AC23 | | | | | | | |
| B8 | VREFB8N0 | IO | DQ15B | | AJ27 | AH24 | | DQ7B | DQ3B | DQ3B | DQ1B | DQ1B |
| B8 | VREFB8N0 | IO | | | AL28 | AF23 | | DQ7B | | | DQ1B | DQ1B |
| B8 | VREFB8N1 | IO | DQ15B | | AJ28 | AF24 | | DQ7B | DQ3B | DQ3B | DQ1B | DQ1B |
| B8 | VREFB8N1 | IO | DQ15B | | AM27 | AF22 | | DQ7B | DQ3B | DQ3B | DQ1B | DQ1B |
| B8 | VREFB8N1 | IO | DQ15B | | AP27 | AH23 | | DQ7B | DQ3B | DQ3B | DQ1B | DQ1B |
| B8 | VREFB8N1 | IO | DQS15B | | AL27 | AG23 | | | DQS3B | DQS3B | | |
| B8 | VREFB8N1 | IO | | | AF22 | | | | | | | |
| B8 | VREFB8N1 | IO | | | AG22 | | | | | | | |
| B8 | VREFB8N1 | IO | DQ14B | | AN26 | AE19 | | DQ7B | | DQ3B | | DQ1B |
| B8 | VREFB8N1 | IO | | | AL26 | | | | | DQ3B | | DQ1B |
| B8 | VREFB8N1 | IO | DQ14B | | AJ26 | AB19 | | DQ7B | | DQ3B | | DQ1B |
| B8 | VREFB8N1 | IO | DQ14B | | AK26 | | | DQ7B | | DQ3B | | DQ1B |
| B8 | VREFB8N1 | IO | DQ14B | | AP26 | AC19 | | DQ7B | | DQ3B | | DQ1B |
| B8 | VREFB8N1 | IO | DQS14B | | AM26 | | | DQS7B | | | | |
| B8 | VREFB8N1 | IO | | | AC22 | | | | | | | |
| B8 | VREFB8N1 | IO | DQ13B | | AJ24 | AG22 | W14 | DQ6B | DQ2B | | DQ1B | |
| B8 | VREFB8N1 | IO | | | AL25 | AF20 | | DQ6B | DQ2B | DQ2B | | |
| B8 | VREFB8N1 | VREFB8N1 | VREFB8N1 | | AK25 | AD19 | V16 | | | | | |
| B8 | VREFB8N1 | IO | DQ13B | | AJ25 | AH22 | | DQ6B | DQ2B | DQ2B | DQ1B | DQ1B |
| B8 | VREFB8N1 | IO | DQ13B | | AN25 | AH21 | | DQ6B | DQ2B | DQ2B | DQ1B | DQ1B |
| B8 | VREFB8N1 | IO | DQ13B | | AP25 | AF21 | | DQ6B | DQ2B | DQ2B | DQ1B | DQ1B |
| B8 | VREFB8N1 | IO | DQS13B | | AM25 | AG20 | | | | | DQS1B | DQS1B |
| B8 | VREFB8N1 | IO | | | AB21 | | | | | | | |
| B8 | VREFB8N1 | IO | DQ12B | | AM24 | AE18 | | DQ6B | | DQ2B | | DQ1B |
| B8 | VREFB8N1 | IO | | | AL24 | | | | | DQ2B | | DQ1B |
| B8 | VREFB8N1 | IO | DQ12B | | AJ23 | W15 | | DQ6B | | DQ2B | | DQ1B |
| B8 | VREFB8N1 | IO | DQ12B | | AK23 | | | DQ6B | | DQ2B | | DQ1B |
| B8 | VREFB8N1 | IO | DQ12B | | AP24 | AC18 | | DQ6B | | DQ2B | | DQ1B |
| B8 | VREFB8N1 | IO | DQS12B | | AL23 | | | DQS6B | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B8 | VREFB8N1 | IO | | | AC21 | | | | | | | |
| B8 | VREFB8N1 | IO | DQ11B | | AM23 | AH20 | Y13 | DQ5B | DQ2B | DQ2B | DQ1B | DQ1B |
| B8 | VREFB8N1 | IO | | | AN23 | AG19 | Y12 | DQ5B | | | DQ1B | DQ1B |
| B8 | VREFB8N2 | IO | DQ11B | | AP23 | AF19 | W12 | DQ5B | DQ2B | DQ2B | DQ1B | DQ1B |
| B8 | VREFB8N2 | IO | DQ11B | | AM22 | AF18 | Y11 | DQ5B | DQ2B | DQ2B | DQ1B | DQ1B |
| B8 | VREFB8N2 | IO | DQ11B | | AP22 | AH18 | | DQ5B | DQ2B | DQ2B | DQ1B | DQ1B |
| B8 | VREFB8N2 | IO | DQS11B | | AN22 | AH19 | W13 | | DQS2B | DQS2B | | |
| B8 | VREFB8N2 | IO | | | AB20 | | | | | | | |
| B8 | VREFB8N2 | IO | | | AC20 | | | | | | | |
| B8 | VREFB8N2 | IO | DQ10B | | AJ22 | AC17 | | DQ5B | | DQ2B | | DQ1B |
| B8 | VREFB8N2 | IO | | | AL22 | | | | | DQ2B | | DQ1B |
| B8 | VREFB8N2 | IO | DQ10B | | AM21 | Y17 | | DQ5B | | DQ2B | | DQ1B |
| B8 | VREFB8N2 | IO | DQ10B | | AP21 | | | DQ5B | | DQ2B | | DQ1B |
| B8 | VREFB8N2 | IO | DQ10B | | AJ21 | AB17 | | DQ5B | | DQ2B | | DQ1B |
| B8 | VREFB8N2 | IO | DQS10B | | AL21 | | | DQS5B | | | | |
| B8 | VREFB8N2 | VREFB8N2 | VREFB8N2 | | AK22 | AD17 | V14 | | | | | |
| B8 | VREFB8N2 | IO | | | AB18 | | | | | | | |
| B8 | VREFB8N2 | IO | | | AH21 | | | | | | | |
| B8 | VREFB8N2 | IO | | | AH23 | | | | | | | |
| B8 | VREFB8N2 | IO | | RUnLU | AH18 | AC16 | T13 | | | | | |
| B8 | VREFB8N2 | IO | | DEV_OE | AG20 | AD16 | U14 | | | | | |
| B8 | VREFB8N2 | IO | | DEV_CLRn | AH20 | AE17 | U13 | | | | | |
| B8 | VREFB8N2 | IO | | nCS | AJ18 | AF17 | AB10 | | | | | |
| B12 | VREFB8N2 | IO | PLL12_FBn/OUT2n | | AJ20 | AE16 | AB9 | | | | | |
| B12 | VREFB8N2 | IO | PLL12_FBp/OUT2p | | AK20 | | | | | | | |
| B8 | VREFB8N2 | IO | | | AC18 | | | | | | | |
| B12 | VREFB8N2 | IO | PLL12_OUT1n | | AL20 | | | | | | | |
| B12 | VREFB8N2 | IO | PLL12_OUT1p | | AM20 | | | | | | | |
| B12 | VREFB8N2 | IO | PLL12_OUT0n | | AN20 | | | | | | | |
| B12 | VREFB8N2 | IO | PLL12_OUT0p | | AP20 | AF16 | W11 | | | | | |
| B8 | VREFB8N2 | IO | CLK5n | | AH19 | AB15 | W10 | | | | | |
| B8 | VREFB8N2 | IO | CLK5p | | AJ19 | AC15 | Y9 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B8 | VREFB8N2 | IO | CLK4n | | AM19 | AG17 | Y10 | | | | | |
| B8 | VREFB8N2 | IO | CLK4p | | AN19 | AH17 | AA10 | | | | | |
| B12 | | VCC_PLL12_OUT | | | AE20 | | | | | | | |
| | | VCCD_PLL12 | | | AF20 | | | | | | | |
| | | VCCA_PLL12 | | | AE18 | | | | | | | |
| | | GNDA_PLL12 | | | AF19 | | | | | | | |
| | | GNDA_PLL12 | | | AF18 | | | | | | | |
| | | GNDA_PLL6 | | | AE17 | W13 | T12 | | | | | |
| | | GNDA_PLL6 | | | AF17 | W14 | U11 | | | | | |
| | | VCCA_PLL6 | | | AE16 | Y14 | U12 | | | | | |
| | | VCCD_PLL6 | | | AF16 | V14 | T11 | | | | | |
| B10 | | VCC_PLL6_OUT | | | AG16 | AA14 | V10 | | | | | |
| B7 | VREFB7N0 | IO | CLK7p | | AL19 | AF15 | AB8 | | | | | |
| B7 | VREFB7N0 | IO | CLK7n | | AK19 | AE15 | AA8 | | | | | |
| B7 | VREFB7N0 | IO | CLK6p | | AP18 | AH16 | Y8 | | | | | |
| B7 | VREFB7N0 | IO | CLK6n | | AP19 | AG16 | W9 | | | | | |
| B10 | VREFB7N0 | IO | PLL6_OUT1p | | AM18 | AG14 | AA7 | | | | | |
| B10 | VREFB7N0 | IO | PLL6_OUT1n | | AL18 | AF14 | Y7 | | | | | |
| B10 | VREFB7N0 | IO | PLL6_OUT0p | | AP17 | AH15 | AB7 | | | | | |
| B10 | VREFB7N0 | IO | PLL6_OUT0n | | AN17 | AH14 | AB6 | | | | | |
| B10 | VREFB7N0 | IO | PLL6_FBp/OUT2p | | AM17 | AE14 | W8 | | | | | |
| B10 | VREFB7N0 | IO | PLL6_FBn/OUT2n | | AL17 | AD14 | W7 | | | | | |
| B7 | VREFB7N0 | IO | | | AJ17 | | | | | | | |
| B7 | VREFB7N0 | IO | | | AH17 | | | | | | | |
| B7 | VREFB7N0 | IO | | | AC16 | | | | | | | |
| B7 | VREFB7N0 | IO | | | AH14 | | | | | | | |
| B7 | VREFB7N0 | IO | DQ9B | | AJ16 | AG13 | U10 | DQ4B | DQ1B | | | |
| B7 | VREFB7N0 | IO | | | AL16 | AE13 | | DQ4B | DQ1B | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N0 | VREFB7N0 | VREFB7N0 | | AK17 | AB14 | V11 | | | | | |
| B7 | VREFB7N0 | IO | DQ9B | | AK16 | AC14 | T8 | DQ4B | DQ1B | DQ1B | DQ0B | |
| B7 | VREFB7N0 | IO | DQ9B | | AN16 | AC13 | T9 | DQ4B | DQ1B | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N0 | IO | DQ9B | | AP16 | AD13 | T10 | DQ4B | DQ1B | DQ1B | DQ0B | DQ0B |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B7 | VREFB7N0 | IO | DQS9B | | AM16 | AF13 | | | | | | |
| B7 | VREFB7N0 | IO | | | AG14 | | | | | | | |
| B7 | VREFB7N0 | IO | | | AF14 | | | | | | | |
| B7 | VREFB7N0 | IO | DQ8B | | AH16 | Y13 | | DQ4B | | DQ1B | | DQ0B |
| B7 | VREFB7N0 | IO | | | AM15 | | | | | DQ1B | | DQ0B |
| B7 | VREFB7N0 | IO | DQ8B | | AH15 | W12 | U8 | DQ4B | | DQ1B | | DQ0B |
| B7 | VREFB7N0 | IO | DQ8B | | AJ15 | V13 | | DQ4B | | DQ1B | | DQ0B |
| B7 | VREFB7N0 | IO | DQ8B | | AP15 | | | DQ4B | | DQ1B | | DQ0B |
| B7 | VREFB7N0 | IO | DQS8B | | AL15 | AB13 | | DQS4B | | | | |
| B7 | VREFB7N0 | IO | | | AC15 | | | | | | | |
| B7 | VREFB7N0 | IO | DQ7B | | AP14 | AH13 | AB4 | DQ3B | DQ1B | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N0 | IO | | | AM14 | AF12 | AB5 | DQ3B | | | DQ0B | DQ0B |
| B7 | VREFB7N1 | IO | DQ7B | | AK14 | AH12 | | DQ3B | DQ1B | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N1 | IO | DQ7B | | AJ14 | AG11 | | DQ3B | DQ1B | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N1 | IO | DQ7B | | AN14 | AH11 | AA4 | DQ3B | DQ1B | DQ1B | DQ0B | DQ0B |
| B7 | VREFB7N1 | IO | DQS7B | | AL14 | AE12 | AA5 | | DQS1B | DQS1B | | |
| B7 | VREFB7N1 | IO | | | AE14 | | | | | | | |
| B7 | VREFB7N1 | IO | | | AC14 | | | | | | | |
| B7 | VREFB7N1 | IO | DQ6B | | AP13 | V11 | | DQ3B | | DQ1B | | DQ0B |
| B7 | VREFB7N1 | IO | | | AM13 | AB12 | | | | DQ1B | | DQ0B |
| B7 | VREFB7N1 | IO | DQ6B | | AH13 | | | DQ3B | | DQ1B | | DQ0B |
| B7 | VREFB7N1 | IO | DQ6B | | AJ13 | W11 | Y6 | DQ3B | | DQ1B | | DQ0B |
| B7 | VREFB7N1 | IO | DQ6B | | AN13 | | | DQ3B | | DQ1B | | DQ0B |
| B7 | VREFB7N1 | IO | DQS6B | | AL13 | AC12 | | DQS3B | | | | |
| B7 | VREFB7N1 | IO | | | AD14 | | | | | | | |
| B7 | VREFB7N1 | IO | | | AF13 | | | | | | | |
| B7 | VREFB7N1 | IO | DQ5B | | AP12 | AD11 | Y5 | DQ2B | DQ0B | | DQ0B | |
| B7 | VREFB7N1 | IO | | | AM12 | AF11 | | DQ2B | DQ0B | DQ0B | | |
| B7 | VREFB7N1 | VREFB7N1 | VREFB7N1 | | AK13 | AC10 | V8 | | | | | |
| B7 | VREFB7N1 | IO | DQ5B | | AH11 | AF10 | | DQ2B | DQ0B | DQ0B | DQ0B | DQ0B |
| B7 | VREFB7N1 | IO | DQ5B | | AH12 | AG10 | | DQ2B | DQ0B | DQ0B | DQ0B | DQ0B |
| B7 | VREFB7N1 | IO | DQ5B | | AJ12 | AH10 | | DQ2B | DQ0B | DQ0B | DQ0B | DQ0B |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B7 | VREFB7N1 | IO | DQS5B | | AL12 | AE11 | | | | | DQS0B | DQS0B |
| B7 | VREFB7N1 | IO | | | AG11 | | | | | | | |
| B7 | VREFB7N1 | IO | DQ4B | | AP11 | | | DQ2B | | DQ0B | | DQ0B |
| B7 | VREFB7N1 | IO | | | AM11 | AB11 | | | | DQ0B | | DQ0B |
| B7 | VREFB7N1 | IO | DQ4B | | AJ11 | | | DQ2B | | DQ0B | | DQ0B |
| B7 | VREFB7N1 | IO | DQ4B | | AK11 | Y11 | | DQ2B | | DQ0B | | DQ0B |
| B7 | VREFB7N1 | IO | DQ4B | | AN11 | AC11 | | DQ2B | | DQ0B | | DQ0B |
| B7 | VREFB7N1 | IO | DQS4B | | AL11 | | | DQS2B | | | | |
| B7 | VREFB7N1 | IO | | | AG10 | | | | | | | |
| B7 | VREFB7N1 | IO | | | AF11 | | | | | | | |
| B7 | VREFB7N1 | IO | DQ3B | | AP10 | AE10 | Y4 | DQ1B | DQ0B | DQ0B | DQ0B | DQ0B |
| B7 | VREFB7N1 | IO | | | AM10 | AF9 | | DQ1B | | | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQ3B | | AH10 | AH8 | | DQ1B | DQ0B | DQ0B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQ3B | | AJ10 | AH9 | | DQ1B | DQ0B | DQ0B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQ3B | | AN10 | AD10 | | DQ1B | DQ0B | DQ0B | DQ0B | DQ0B |
| B7 | VREFB7N2 | IO | DQS3B | | AL10 | AE9 | | | DQS0B | DQS0B | | |
| B7 | VREFB7N2 | IO | | | AC13 | | | | | | | |
| B7 | VREFB7N2 | IO | | | AD13 | | | | | | | |
| B7 | VREFB7N2 | IO | DQ2B | | AP9 | | | DQ1B | | DQ0B | | DQ0B |
| B7 | VREFB7N2 | IO | | | AM9 | | | | | DQ0B | | DQ0B |
| B7 | VREFB7N2 | IO | DQ2B | | AH9 | AB10 | | DQ1B | | DQ0B | | DQ0B |
| B7 | VREFB7N2 | IO | DQ2B | | AH8 | Y10 | | DQ1B | | DQ0B | | DQ0B |
| B7 | VREFB7N2 | IO | DQ2B | | AJ9 | | | DQ1B | | DQ0B | | DQ0B |
| B7 | VREFB7N2 | IO | DQS2B | | AL9 | | | DQS1B | | | | |
| B7 | VREFB7N2 | IO | | | AE11 | | | | | | | |
| B7 | VREFB7N2 | IO | DQ1B | | AP8 | AH7 | | DQ0B | | | | |
| B7 | VREFB7N2 | IO | | | AM8 | AG8 | | DQ0B | | | | |
| B7 | VREFB7N2 | VREFB7N2 | VREFB7N2 | | AK10 | AD8 | V7 | | | | | |
| B7 | VREFB7N2 | IO | DQ1B | | AJ8 | AE7 | | DQ0B | | | | |
| B7 | VREFB7N2 | IO | DQ1B | | AK8 | AF7 | | DQ0B | | | | |
| B7 | VREFB7N2 | IO | DQ1B | | AN8 | AE8 | | DQ0B | | | | |
| B7 | VREFB7N2 | IO | DQS1B | | AL8 | AF8 | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B7 | VREFB7N2 | IO | | | AE10 | AC8 | AB3 | | | | | |
| B7 | VREFB7N2 | IO | | | AE9 | AB8 | Y3 | | | | | |
| B7 | VREFB7N2 | IO | DQ0B | | AP7 | AB9 | | DQ0B | | | | |
| B7 | VREFB7N2 | IO | | | AM7 | AC9 | | | | | | |
| B7 | VREFB7N2 | IO | DQ0B | | AG8 | | | DQ0B | | | | |
| B7 | VREFB7N2 | IO | DQ0B | | AH7 | W10 | | DQ0B | | | | |
| B7 | VREFB7N2 | IO | DQ0B | | AJ7 | W9 | | DQ0B | | | | |
| B7 | VREFB7N2 | IO | DQS0B | | AL7 | | | DQS0B | | | | |
| B7 | VREFB7N2 | PORSEL | | PORSEL | AE8 | Y8 | AB2 | | | | | |
| B7 | VREFB7N2 | nIO_PULLUP | | nIO_PULLUP | AE7 | Y7 | AB1 | | | | | |
| B7 | VREFB7N2 | PLL_ENA | | PLL_ENA | AF8 | AA8 | AA2 | | | | | |
| | | GND | | | AF7 | AC7 | Y2 | | | | | |
| B7 | VREFB7N2 | nCEO | | nCEO | AF9 | AB7 | Y1 | | | | | |
| B15 | | GXB_RX11n | | | AM2 | | | | | | | |
| B15 | | GXB_RX11p | | | AM1 | | | | | | | |
| B15 | | GXB_TX11n | | | AP5 | | | | | | | |
| B15 | | GXB_TX11p | | | AP4 | | | | | | | |
| B15 | | GXB_RX10n | | | AK2 | | | | | | | |
| B15 | | GXB_RX10p | | | AK1 | | | | | | | |
| B15 | | GXB_TX10n | | | AM5 | | | | | | | |
| B15 | | GXB_TX10p | | | AM4 | | | | | | | |
| B15 | | RREFB15 | | | AH4 | | | | | | | |
| B15 | | REFCLK0_B15n | | | AK5 | | | | | | | |
| B15 | | REFCLK0_B15p | | | AK4 | | | | | | | |
| B15 | | REFCLK1_B15n | | | AH2 | | | | | | | |
| B15 | | REFCLK1_B15p | | | AH1 | | | | | | | |
| | | VCCA | | | AC11 | | | | | | | |
| | | VCCA | | | AA8 | | | | | | | |
| | | VCCA | | | AC9 | | | | | | | |
| B15 | | GXB_RX8n | | | AF2 | | | | | | | |
| B15 | | GXB_RX8p | | | AF1 | | | | | | | |
| B15 | | GXB_TX8n | | | AF5 | | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B15 | | GXB_TX8p | | | AF4 | | | | | | | |
| B15 | | GXB_RX9n | | | AD2 | | | | | | | |
| B15 | | GXB_RX9p | | | AD1 | | | | | | | |
| B15 | | GXB_TX9n | | | AD5 | | | | | | | |
| B15 | | GXB_TX9p | | | AD4 | | | | | | | |
| B14 | | GXB_RX7n | | | AB2 | AD2 | V2 | | | | | |
| B14 | | GXB_RX7p | | | AB1 | AD1 | V1 | | | | | |
| B14 | | GXB_TX7n | | | AB5 | AF5 | V5 | | | | | |
| B14 | | GXB_TX7p | | | AB4 | AF4 | V4 | | | | | |
| B14 | | GXB_RX6n | | | Y2 | AB2 | T2 | | | | | |
| B14 | | GXB_RX6p | | | Y1 | AB1 | T1 | | | | | |
| B14 | | GXB_TX6n | | | Y5 | AD5 | T5 | | | | | |
| B14 | | GXB_TX6p | | | Y4 | AD4 | T4 | | | | | |
| B14 | | RREFB14 | | | V4 | Y4 | J3 | | | | | |
| B14 | | REFCLK0_B14n | | | V2 | Y2 | N1 | | | | | |
| B14 | | REFCLK0_B14p | | | V1 | Y1 | P1 | | | | | |
| B14 | | REFCLK1_B14n | | | U7 | AB5 | J1 | | | | | |
| B14 | | REFCLK1_B14p | | | U6 | AB4 | K1 | | | | | |
| | | VCCA | | | W11 | V9 | P6 | | | | | |
| | | VCCA | | | U8 | T6 | M3 | | | | | |
| | | VCCA | | | W9 | V7 | P4 | | | | | |
| B14 | | GXB_RX4n | | | R2 | V2 | G2 | | | | | |
| B14 | | GXB_RX4p | | | R1 | V1 | G1 | | | | | |
| B14 | | GXB_TX4n | | | R5 | V5 | G5 | | | | | |
| B14 | | GXB_TX4p | | | R4 | V4 | G4 | | | | | |
| B14 | | GXB_RX5n | | | N2 | T2 | E2 | | | | | |
| B14 | | GXB_RX5p | | | N1 | T1 | E1 | | | | | |
| B14 | | GXB_TX5n | | | N5 | T5 | E5 | | | | | |
| B14 | | GXB_TX5p | | | N4 | T4 | E4 | | | | | |
| B13 | | GXB_RX3n | | | L2 | N2 | | | | | | |
| B13 | | GXB_RX3p | | | L1 | N1 | | | | | | |
| B13 | | GXB_TX3n | | | L5 | N5 | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B13 | | GXB_TX3p | | | L4 | N4 | | | | | | |
| B13 | | GXB_RX2n | | | J2 | L2 | | | | | | |
| B13 | | GXB_RX2p | | | J1 | L1 | | | | | | |
| B13 | | GXB_TX2n | | | J5 | L5 | | | | | | |
| B13 | | GXB_TX2p | | | J4 | L4 | | | | | | |
| B13 | | RREFB13 | | | G4 | J4 | | | | | | |
| B13 | | REFCLK0_B13n | | | G2 | J2 | | | | | | |
| B13 | | REFCLK0_B13p | | | G1 | J1 | | | | | | |
| B13 | | REFCLK1_B13n | | | E5 | G5 | | | | | | |
| B13 | | REFCLK1_B13p | | | E4 | G4 | | | | | | |
| | | VCCA | | | R11 | P9 | | | | | | |
| | | VCCA | | | N8 | M6 | | | | | | |
| | | VCCA | | | R9 | P7 | | | | | | |
| B13 | | GXB_RX0n | | | E2 | G2 | | | | | | |
| B13 | | GXB_RX0p | | | E1 | G1 | | | | | | |
| B13 | | GXB_TX0n | | | C5 | E5 | | | | | | |
| B13 | | GXB_TX0p | | | C4 | E4 | | | | | | |
| B13 | | GXB_RX1n | | | C2 | E2 | | | | | | |
| B13 | | GXB_RX1p | | | C1 | E1 | | | | | | |
| B13 | | GXB_TX1n | | | A5 | C5 | | | | | | |
| B13 | | GXB_TX1p | | | A4 | C4 | | | | | | |
| NC | | NC | | | L7 | K7 | J5 | | | | | |
| NC | | NC | | | L8 | K8 | J6 | | | | | |
| | | VCCA | | | L9 | K9 | | | | | | |
| | | GND | | | J8 | F7 | C3 | | | | | |
| | | GND | | | J7 | G7 | C2 | | | | | |
| B4 | VREFB4N0 | TDO | | TDO | H10 | F8 | C1 | | | | | |
| B4 | VREFB4N0 | MSEL3 | | MSEL3 | H11 | G8 | A1 | | | | | |
| B4 | VREFB4N0 | MSEL2 | | MSEL2 | J10 | H8 | A2 | | | | | |
| B4 | VREFB4N0 | MSEL1 | | MSEL1 | J9 | E8 | C4 | | | | | |
| B4 | VREFB4N0 | MSEL0 | | MSEL0 | K10 | J8 | C5 | | | | | |
| B4 | VREFB4N0 | IO | DQS0T | | D7 | | | DQS0T | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B4 | VREFB4N0 | IO | DQ0T | | F7 | | | DQ0T | | | | |
| B4 | VREFB4N0 | IO | DQ0T | | G7 | | | DQ0T | | | | |
| B4 | VREFB4N0 | IO | DQ0T | | H8 | K10 | | DQ0T | | | | |
| B4 | VREFB4N0 | IO | | | C7 | | | | | | | |
| B4 | VREFB4N0 | IO | DQ0T | | A7 | G9 | | DQ0T | | | | |
| B4 | VREFB4N0 | IO | | | J11 | C7 | H8 | | | | | |
| B4 | VREFB4N0 | IO | | | K11 | D7 | G8 | | | | | |
| B4 | VREFB4N0 | IO | DQS1T | | D8 | C8 | | | | | | |
| B4 | VREFB4N0 | IO | DQ1T | | B8 | D9 | | DQ0T | | | | |
| B4 | VREFB4N0 | IO | DQ1T | | E8 | A7 | | DQ0T | | | | |
| B4 | VREFB4N0 | IO | DQ1T | | F8 | D8 | | DQ0T | | | | |
| B4 | VREFB4N0 | VREFB4N0 | VREFB4N0 | | E10 | F9 | E7 | | | | | |
| B4 | VREFB4N0 | IO | | | C8 | B8 | B2 | DQ0T | | | | |
| B4 | VREFB4N0 | IO | DQ1T | | A8 | A8 | | DQ0T | | | | |
| B4 | VREFB4N0 | IO | | | J13 | | | | | | | |
| B4 | VREFB4N0 | IO | DQS2T | | D9 | E10 | | DQS1T | | | | |
| B4 | VREFB4N0 | IO | DQ2T | | F9 | | | DQ1T | | DQ0T | | DQ0T |
| B4 | VREFB4N0 | IO | DQ2T | | G8 | J10 | | DQ1T | | DQ0T | | DQ0T |
| B4 | VREFB4N0 | IO | DQ2T | | G9 | H10 | | DQ1T | | DQ0T | | DQ0T |
| B4 | VREFB4N0 | IO | | | C9 | | | | | DQ0T | | DQ0T |
| B4 | VREFB4N0 | IO | DQ2T | | A9 | G10 | F8 | DQ1T | | DQ0T | | DQ0T |
| B4 | VREFB4N0 | IO | | | K13 | | | | | | | |
| B4 | VREFB4N0 | IO | | | L13 | | | | | | | |
| B4 | VREFB4N0 | IO | DQS3T | | D10 | D10 | | | DQS0T | DQS0T | | |
| B4 | VREFB4N0 | IO | DQ3T | | B10 | B10 | | DQ1T | DQ0T | DQ0T | DQ0T | DQ0T |
| B4 | VREFB4N0 | IO | DQ3T | | F10 | A9 | | DQ1T | DQ0T | DQ0T | DQ0T | DQ0T |
| B4 | VREFB4N0 | IO | DQ3T | | G10 | C9 | F7 | DQ1T | DQ0T | DQ0T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | | | C10 | C10 | | DQ1T | | | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ3T | | A10 | E11 | | DQ1T | DQ0T | DQ0T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | | | H14 | K11 | | | | | | |
| B4 | VREFB4N1 | IO | DQS4T | | D11 | | | DQS2T | | | | |
| B4 | VREFB4N1 | IO | DQ4T | | B11 | G11 | | DQ2T | | DQ0T | | DQ0T |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B4 | VREFB4N1 | IO | DQ4T | | E11 | J11 | | DQ2T | | DQ0T | | DQ0T |
| B4 | VREFB4N1 | IO | DQ4T | | F11 | | | DQ2T | | DQ0T | | DQ0T |
| B4 | VREFB4N1 | IO | | | C11 | F11 | | | | DQ0T | | DQ0T |
| B4 | VREFB4N1 | IO | DQ4T | | A11 | H11 | | DQ2T | | DQ0T | | DQ0T |
| B4 | VREFB4N1 | IO | | | K14 | | | | | | | |
| B4 | VREFB4N1 | IO | | | L14 | | | | | | | |
| B4 | VREFB4N1 | IO | DQS5T | | D12 | C11 | | | | | DQS0T | DQS0T |
| B4 | VREFB4N1 | IO | DQ5T | | F12 | C12 | | DQ2T | DQ0T | DQ0T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ5T | | G12 | D11 | | DQ2T | DQ0T | DQ0T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ5T | | G11 | A10 | | DQ2T | DQ0T | DQ0T | DQ0T | DQ0T |
| B4 | VREFB4N1 | VREFB4N1 | VREFB4N1 | | E13 | F10 | E8 | | | | | |
| B4 | VREFB4N1 | IO | | | C12 | B11 | | DQ2T | DQ0T | DQ0T | | |
| B4 | VREFB4N1 | IO | DQ5T | | A12 | D12 | | DQ2T | DQ0T | | DQ0T | |
| B4 | VREFB4N1 | IO | | | M15 | | | | | | | |
| B4 | VREFB4N1 | IO | DQS6T | | D13 | | | DQS3T | | | | |
| B4 | VREFB4N1 | IO | DQ6T | | B13 | K12 | | DQ3T | | DQ1T | | DQ0T |
| B4 | VREFB4N1 | IO | DQ6T | | F13 | L12 | | DQ3T | | DQ1T | | DQ0T |
| B4 | VREFB4N1 | IO | DQ6T | | G13 | | | DQ3T | | DQ1T | | DQ0T |
| B4 | VREFB4N1 | IO | | | C13 | G12 | | | | DQ1T | | DQ0T |
| B4 | VREFB4N1 | IO | DQ6T | | A13 | L13 | G9 | DQ3T | | DQ1T | | DQ0T |
| B4 | VREFB4N1 | IO | | | N17 | | | | | | | |
| B4 | VREFB4N1 | IO | | | F18 | | | | | | | |
| B4 | VREFB4N1 | IO | DQS7T | | D14 | D13 | B4 | | DQS1T | DQS1T | | |
| B4 | VREFB4N1 | IO | DQ7T | | B14 | A11 | A3 | DQ3T | DQ1T | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ7T | | F14 | F13 | D7 | DQ3T | DQ1T | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N1 | IO | DQ7T | | E14 | A12 | C6 | DQ3T | DQ1T | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | | | C14 | C13 | B5 | DQ3T | | | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ7T | | A14 | E13 | A4 | DQ3T | DQ1T | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | | | M16 | | | | | | | |
| B4 | VREFB4N2 | IO | DQS8T | | D15 | L14 | | DQS4T | | | | |
| B4 | VREFB4N2 | IO | DQ8T | | A15 | H13 | | DQ4T | | DQ1T | | DQ0T |
| B4 | VREFB4N2 | IO | DQ8T | | F15 | | | DQ4T | | DQ1T | | DQ0T |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B4 | VREFB4N2 | IO | DQ8T | | G15 | K13 | | DQ4T | | DQ1T | | DQ0T |
| B4 | VREFB4N2 | IO | | | C15 | G13 | | | | DQ1T | | DQ0T |
| B4 | VREFB4N2 | IO | DQ8T | | G14 | | | DQ4T | | DQ1T | | DQ0T |
| B4 | VREFB4N2 | IO | | | N18 | | | | | | | |
| B4 | VREFB4N2 | IO | | | M17 | | | | | | | |
| B4 | VREFB4N2 | IO | DQS9T | | C16 | B14 | H9 | | | | | |
| B4 | VREFB4N2 | IO | DQ9T | | A16 | E14 | F11 | DQ4T | DQ1T | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ9T | | B16 | A13 | G10 | DQ4T | DQ1T | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ9T | | F16 | B13 | | DQ4T | DQ1T | DQ1T | DQ0T | |
| B4 | VREFB4N2 | VREFB4N2 | VREFB4N2 | | E16 | F12 | E11 | | | | | |
| B4 | VREFB4N2 | IO | | | D16 | C14 | H10 | DQ4T | DQ1T | DQ1T | DQ0T | DQ0T |
| B4 | VREFB4N2 | IO | DQ9T | | G16 | D14 | F10 | DQ4T | DQ1T | | | |
| B4 | VREFB4N2 | IO | | | F19 | | | | | | | |
| B4 | VREFB4N2 | IO | | | M18 | | | | | | | |
| B4 | VREFB4N2 | IO | | | M19 | | | | | | | |
| B9 | VREFB4N2 | IO | PLL5_FBn/OUT2n | | F17 | G14 | C7 | | | | | |
| B9 | VREFB4N2 | IO | PLL5_FBp/OUT2p | | E17 | F14 | B7 | | | | | |
| B9 | VREFB4N2 | IO | PLL5_OUT0n | | B17 | A14 | D9 | | | | | |
| B9 | VREFB4N2 | IO | PLL5_OUT0p | | A17 | A15 | C9 | | | | | |
| B9 | VREFB4N2 | IO | PLL5_OUT1n | | D17 | D15 | D8 | | | | | |
| B9 | VREFB4N2 | IO | PLL5_OUT1p | | C17 | C15 | C8 | | | | | |
| B4 | VREFB4N2 | IO | CLK12n | | A19 | B16 | B8 | | | | | |
| B4 | VREFB4N2 | IO | CLK12p | | A18 | A16 | A7 | | | | | |
| B4 | VREFB4N2 | IO | CLK13n | | D18 | G15 | A6 | | | | | |
| B4 | VREFB4N2 | IO | CLK13p | | C18 | F15 | A5 | | | | | |
| B9 | | VCC_PLL5_OUT | | | H16 | J14 | E10 | | | | | |
| | | VCCD_PLL5 | | | H17 | K16 | H11 | | | | | |
| | | VCCA_PLL5 | | | K16 | J15 | G12 | | | | | |
| | | GNDA_PLL5 | | | J16 | J16 | H12 | | | | | |
| | | GNDA_PLL5 | | | J17 | K15 | G11 | | | | | |
| | | GNDA_PLL11 | | | J18 | | | | | | | |
| | | GNDA_PLL11 | | | K18 | | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | VCCA_PLL11 | | | K17 | | | | | | | |
| | | VCCD_PLL11 | | | J19 | | | | | | | |
| B11 | | VCC_PLL11_OUT | | | K20 | | | | | | | |
| B3 | VREFB3N0 | IO | CLK14p | | B19 | A17 | A8 | | | | | |
| B3 | VREFB3N0 | IO | CLK14n | | C19 | B17 | A9 | | | | | |
| B3 | VREFB3N0 | IO | CLK15p | | D19 | C16 | C10 | | | | | |
| B3 | VREFB3N0 | IO | CLK15n | | E19 | D16 | D10 | | | | | |
| B11 | VREFB3N0 | IO | PLL11_OUT0p | | A20 | | | | | | | |
| B11 | VREFB3N0 | IO | PLL11_OUT0n | | B20 | C17 | | | | | | |
| B11 | VREFB3N0 | IO | PLL11_OUT1p | | C20 | | | | | | | |
| B11 | VREFB3N0 | IO | PLL11_OUT1n | | D20 | | | | | | | |
| B3 | VREFB3N0 | IO | | | G23 | | | | | | | |
| B11 | VREFB3N0 | IO | PLL11_FBp/OUT2p | | E20 | | | | | | | |
| B11 | VREFB3N0 | IO | PLL11_FBn/OUT2n | | F20 | | | | | | | |
| B3 | VREFB3N0 | IO | | PGM2 | G20 | E16 | C11 | | | | | |
| B3 | VREFB3N0 | IO | | PGM1 | H20 | F16 | D13 | | | | | |
| B3 | VREFB3N0 | IO | | PGM0 | H22 | G16 | D12 | | | | | |
| B3 | VREFB3N0 | IO | | ASDO | N21 | L16 | F12 | | | | | |
| B3 | VREFB3N0 | IO | | nCSO | G21 | D17 | B10 | | | | | |
| B3 | VREFB3N0 | IO | | CRC_ERROR | G22 | E17 | A10 | | | | | |
| B3 | VREFB3N0 | IO | | DATA0 | J20 | F17 | D11 | | | | | |
| B3 | VREFB3N0 | IO | | DATA1 | J22 | K17 | F13 | | | | | |
| B3 | VREFB3N0 | VREFB3N0 | VREFB3N0 | | E22 | E19 | E14 | | | | | |
| B3 | VREFB3N0 | IO | DQS10T | | D22 | D18 | | DQS5T | | | | |
| B3 | VREFB3N0 | IO | DQ10T | | C21 | | | DQ5T | | DQ2T | | DQ1T |
| B3 | VREFB3N0 | IO | DQ10T | | A21 | L17 | F14 | DQ5T | | DQ2T | | DQ1T |
| B3 | VREFB3N0 | IO | DQ10T | | F21 | | | DQ5T | | DQ2T | | DQ1T |
| B3 | VREFB3N0 | IO | | | D21 | F18 | | | | DQ2T | | DQ1T |
| B3 | VREFB3N0 | IO | DQ10T | | F22 | G18 | G13 | DQ5T | | DQ2T | | DQ1T |
| B3 | VREFB3N0 | IO | | | H23 | | | | | | | |
| B3 | VREFB3N0 | IO | | | M21 | | | | | | | |
| B3 | VREFB3N0 | IO | DQS11T | | C22 | A19 | D14 | | DQS2T | DQS2T | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B3 | VREFB3N0 | IO | DQ11T | | A22 | A18 | C12 | DQ5T | DQ2T | DQ2T | DQ1T | DQ1T |
| B3 | VREFB3N0 | IO | DQ11T | | B22 | C18 | C13 | DQ5T | DQ2T | DQ2T | DQ1T | DQ1T |
| B3 | VREFB3N0 | IO | DQ11T | | F23 | C19 | B13 | DQ5T | DQ2T | DQ2T | DQ1T | DQ1T |
| B3 | VREFB3N1 | IO | | | D23 | B19 | C14 | DQ5T | | | DQ1T | DQ1T |
| B3 | VREFB3N1 | IO | DQ11T | | E23 | A20 | B14 | DQ5T | DQ2T | DQ2T | DQ1T | DQ1T |
| B3 | VREFB3N1 | IO | | | G24 | | | | | | | |
| B3 | VREFB3N1 | IO | DQS12T | | C23 | | | DQS6T | | | | |
| B3 | VREFB3N1 | IO | DQ12T | | B23 | F19 | | DQ6T | | DQ2T | | DQ1T |
| B3 | VREFB3N1 | IO | DQ12T | | A23 | | | DQ6T | | DQ2T | | DQ1T |
| B3 | VREFB3N1 | IO | DQ12T | | D24 | K18 | | DQ6T | | DQ2T | | DQ1T |
| B3 | VREFB3N1 | IO | | | C24 | | | | | DQ2T | | DQ1T |
| B3 | VREFB3N1 | IO | DQ12T | | F24 | H19 | | DQ6T | | DQ2T | | DQ1T |
| B3 | VREFB3N1 | IO | | | J23 | | | | | | | |
| B3 | VREFB3N1 | IO | DQS13T | | B25 | B20 | H13 | | | | DQS1T | DQS1T |
| B3 | VREFB3N1 | IO | DQ13T | | A24 | A21 | H14 | DQ6T | DQ2T | DQ2T | DQ1T | DQ1T |
| B3 | VREFB3N1 | IO | DQ13T | | A25 | C21 | | DQ6T | DQ2T | DQ2T | DQ1T | DQ1T |
| B3 | VREFB3N1 | IO | DQ13T | | F25 | A22 | J14 | DQ6T | DQ2T | DQ2T | DQ1T | DQ1T |
| B3 | VREFB3N1 | VREFB3N1 | VREFB3N1 | | E25 | E20 | E16 | | | | | |
| B3 | VREFB3N1 | IO | | | C25 | C20 | G14 | DQ6T | DQ2T | DQ2T | | |
| B3 | VREFB3N1 | IO | DQ13T | | D25 | B22 | G15 | DQ6T | DQ2T | | DQ1T | |
| B3 | VREFB3N1 | IO | | | M23 | | | | | | | |
| B3 | VREFB3N1 | IO | | | K23 | | | | | | | |
| B3 | VREFB3N1 | IO | DQS14T | | C26 | D19 | | DQS7T | | | | |
| B3 | VREFB3N1 | IO | DQ14T | | B26 | | | DQ7T | | DQ3T | | DQ1T |
| B3 | VREFB3N1 | IO | DQ14T | | E26 | G19 | | DQ7T | | DQ3T | | DQ1T |
| B3 | VREFB3N1 | IO | DQ14T | | F26 | | | DQ7T | | DQ3T | | DQ1T |
| B3 | VREFB3N1 | IO | | | D26 | F20 | | | | DQ3T | | DQ1T |
| B3 | VREFB3N1 | IO | DQ14T | | A26 | | | DQ7T | | DQ3T | | DQ1T |
| B3 | VREFB3N1 | IO | | | J24 | | | | | | | |
| B3 | VREFB3N1 | IO | DQS15T | | B28 | B23 | | | DQS3T | DQS3T | | |
| B3 | VREFB3N1 | IO | DQ15T | | A27 | A23 | | DQ7T | DQ3T | DQ3T | DQ1T | DQ1T |
| B3 | VREFB3N1 | IO | DQ15T | | A28 | C22 | F16 | DQ7T | DQ3T | DQ3T | DQ1T | DQ1T |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B3 | VREFB3N1 | IO | DQ15T | | C27 | A24 | | DQ7T | DQ3T | DQ3T | DQ1T | DQ1T |
| B3 | VREFB3N2 | IO | | | C28 | C23 | | DQ7T | | | DQ1T | DQ1T |
| B3 | VREFB3N2 | IO | DQ15T | | D27 | C24 | | DQ7T | DQ3T | DQ3T | DQ1T | DQ1T |
| B3 | VREFB3N2 | IO | | | K24 | | | | | | | |
| B3 | VREFB3N2 | IO | DQS16T | | C29 | | | DQS8T | | | | |
| B3 | VREFB3N2 | IO | DQ16T | | A29 | G20 | | DQ8T | | DQ3T | | DQ1T |
| B3 | VREFB3N2 | IO | DQ16T | | D28 | | | DQ8T | | DQ3T | | DQ1T |
| B3 | VREFB3N2 | IO | DQ16T | | E29 | K20 | | DQ8T | | DQ3T | | DQ1T |
| B3 | VREFB3N2 | IO | | | D29 | | | | | DQ3T | | DQ1T |
| B3 | VREFB3N2 | IO | DQ16T | | B29 | D20 | | DQ8T | | DQ3T | | DQ1T |
| B3 | VREFB3N2 | IO | | | F29 | | | | | | | |
| B3 | VREFB3N2 | IO | | | G29 | | | | | | | |
| B3 | VREFB3N2 | IO | DQS17T | | A31 | B25 | | | | | | |
| B3 | VREFB3N2 | IO | DQ17T | | A30 | A26 | | DQ8T | DQ3T | DQ3T | DQ1T | DQ1T |
| B3 | VREFB3N2 | IO | DQ17T | | A32 | A25 | C15 | DQ8T | DQ3T | DQ3T | DQ1T | DQ1T |
| B3 | VREFB3N2 | IO | DQ17T | | B32 | C26 | | DQ8T | DQ3T | DQ3T | DQ1T | |
| B3 | VREFB3N2 | VREFB3N2 | VREFB3N2 | | E28 | E22 | E17 | | | | | |
| B3 | VREFB3N2 | IO | | | B31 | C25 | D16 | DQ8T | DQ3T | DQ3T | DQ1T | DQ1T |
| B3 | VREFB3N2 | IO | DQ17T | | C30 | B26 | | DQ8T | DQ3T | | | |
| B3 | VREFB3N2 | IO | | | H28 | | | | | | | |
| B3 | VREFB3N2 | IO | | | J27 | L20 | D15 | | | | | |
| B3 | VREFB3N2 | IO | | DATA2 | G25 | F21 | A12 | | | | | |
| B3 | VREFB3N2 | IO | | DATA3 | F27 | D21 | A13 | | | | | |
| B3 | VREFB3N2 | IO | | DATA4 | H25 | G21 | B11 | | | | | |
| B3 | VREFB3N2 | IO | | DATA5 | G27 | D23 | D17 | | | | | |
| B3 | VREFB3N2 | IO | | DATA6 | G26 | F22 | A14 | | | | | |
| B3 | VREFB3N2 | IO | | DATA7 | H26 | D22 | C16 | | | | | |
| B3 | VREFB3N2 | IO | | RDYnBSY | F28 | J21 | A11 | | | | | |
| B3 | VREFB3N2 | IO | | INIT_DONE | G28 | G22 | C17 | | | | | |
| B3 | VREFB3N2 | nSTATUS | | nSTATUS | D31 | D26 | A16 | | | | | |
| B3 | VREFB3N2 | nCE | | nCE | D30 | D24 | A15 | | | | | |
| B3 | VREFB3N2 | DCLK | | DCLK | C32 | D25 | B16 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| B3 | VREFB3N2 | CONF_DONE | | CONF_DONE | C31 | E23 | C18 | | | | | |
| | | VCCIO2 | | | P25 | J22 | J15 | | | | | |
| | | VCCIO2 | | | P26 | L22 | H17 | | | | | |
| | | VCCIO2 | | | U25 | N21 | | | | | | |
| | | VCCIO2 | | | U26 | | | | | | | |
| | | VCCIO1 | | | AC25 | U22 | R14 | | | | | |
| | | VCCIO1 | | | AC26 | V21 | T18 | | | | | |
| | | VCCIO1 | | | Y25 | Y22 | | | | | | |
| | | VCCIO1 | | | Y26 | | | | | | | |
| | | VCCIO8 | | | AE19 | AA16 | U15 | | | | | |
| | | VCCIO8 | | | AE21 | Y18 | V13 | | | | | |
| | | VCCIO8 | | | AF21 | Y19 | | | | | | |
| | | VCCIO8 | | | AG19 | | | | | | | |
| | | VCCIO7 | | | AE12 | AA10 | U7 | | | | | |
| | | VCCIO7 | | | AE15 | AA13 | U9 | | | | | |
| | | VCCIO7 | | | AF12 | Y9 | | | | | | |
| | | VCCIO7 | | | AF15 | | | | | | | |
| | | VCCT_B15 | | | AA10 | | | | | | | |
| | | VCCT_B15 | | | Y10 | | | | | | | |
| | | VCCH_B15 | | | AA11 | | | | | | | |
| | | VCCH_B15 | | | Y11 | | | | | | | |
| | | VCCR | | | AA9 | | | | | | | |
| | | VCCR | | | Y9 | | | | | | | |
| | | VCCA | | | Y8 | | | | | | | |
| | | VCCL_B15 | | | AB8 | | | | | | | |
| | | VCCT_B14 | | | T10 | R8 | L5 | | | | | |
| | | VCCT_B14 | | | U10 | T8 | M5 | | | | | |
| | | VCCH_B14 | | | T11 | R9 | L6 | | | | | |
| | | VCCH_B14 | | | U11 | T9 | M6 | | | | | |
| | | VCCR | | | T9 | R7 | L4 | | | | | |
| | | VCCR | | | U9 | T7 | M4 | | | | | |
| | | VCCA | | | T8 | R6 | L3 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | VCCL_B14 | | | V8 | U6 | N3 | | | | | |
| | | VCCT_B13 | | | M10 | L8 | | | | | | |
| | | VCCT_B13 | | | N10 | M8 | | | | | | |
| | | VCCH_B13 | | | M11 | L9 | | | | | | |
| | | VCCH_B13 | | | N11 | M9 | | | | | | |
| | | VCCR | | | M9 | L7 | | | | | | |
| | | VCCR | | | N9 | M7 | | | | | | |
| | | VCCA | | | M8 | L6 | | | | | | |
| | | VCCL_B13 | | | P8 | N6 | | | | | | |
| | | VCCP | | | AA12 | | | | | | | |
| | | VCCP | | | Y12 | | | | | | | |
| | | VCCP | | | T12 | R10 | L7 | | | | | |
| | | VCCP | | | U12 | T10 | M7 | | | | | |
| | | VCCP | | | M12 | L10 | | | | | | |
| | | VCCP | | | N12 | M10 | | | | | | |
| | | VCCIO4 | | | J12 | H14 | G7 | | | | | |
| | | VCCIO4 | | | J15 | J9 | F9 | | | | | |
| | | VCCIO4 | | | K12 | J12 | | | | | | |
| | | VCCIO4 | | | K15 | | | | | | | |
| | | VCCIO3 | | | H19 | H17 | F15 | | | | | |
| | | VCCIO3 | | | J21 | H20 | E13 | | | | | |
| | | VCCIO3 | | | K19 | J19 | | | | | | |
| | | VCCIO3 | | | K21 | | | | | | | |
| | | VCCA | | | | | J7 | | | | | |
| | | VCCINT | | | AA14 | M12 | K13 | | | | | |
| | | VCCINT | | | AA16 | M14 | K11 | | | | | |
| | | VCCINT | | | AA18 | M16 | J10 | | | | | |
| | | VCCINT | | | AA20 | M18 | K9 | | | | | |
| | | VCCINT | | | AA22 | N11 | L8 | | | | | |
| | | VCCINT | | | P15 | N13 | M9 | | | | | |
| | | VCCINT | | | P17 | N15 | N8 | | | | | |
| | | VCCINT | | | P19 | N17 | P9 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | VCCINT | | | P21 | P12 | R10 | | | | | |
| | | VCCINT | | | R14 | P14 | P11 | | | | | |
| | | VCCINT | | | R16 | P16 | N10 | | | | | |
| | | VCCINT | | | R18 | P18 | L10 | | | | | |
| | | VCCINT | | | R20 | R11 | M11 | | | | | |
| | | VCCINT | | | R22 | R13 | L12 | | | | | |
| | | VCCINT | | | T13 | R15 | M13 | | | | | |
| | | VCCINT | | | T15 | R17 | N12 | | | | | |
| | | VCCINT | | | T17 | T12 | P13 | | | | | |
| | | VCCINT | | | T19 | T14 | | | | | | |
| | | VCCINT | | | T21 | T16 | | | | | | |
| | | VCCINT | | | U14 | T18 | | | | | | |
| | | VCCINT | | | U16 | U11 | | | | | | |
| | | VCCINT | | | U18 | U13 | | | | | | |
| | | VCCINT | | | U20 | U15 | | | | | | |
| | | VCCINT | | | U22 | U17 | | | | | | |
| | | VCCINT | | | V13 | | | | | | | |
| | | VCCINT | | | V15 | | | | | | | |
| | | VCCINT | | | V17 | | | | | | | |
| | | VCCINT | | | V19 | | | | | | | |
| | | VCCINT | | | V21 | | | | | | | |
| | | VCCINT | | | W14 | | | | | | | |
| | | VCCINT | | | W16 | | | | | | | |
| | | VCCINT | | | W18 | | | | | | | |
| | | VCCINT | | | W20 | | | | | | | |
| | | VCCINT | | | W22 | | | | | | | |
| | | VCCINT | | | Y15 | | | | | | | |
| | | VCCINT | | | Y17 | | | | | | | |
| | | VCCINT | | | Y19 | | | | | | | |
| | | VCCINT | | | Y21 | | | | | | | |
| | | GND | | | A33 | AA21 | AA21 | | | | | |
| | | GND | | | T24 | AA24 | AA18 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | T27 | AA27 | V18 | | | | | |
| | | GND | | | T30 | AD24 | V21 | | | | | |
| | | GND | | | T33 | AD27 | R21 | | | | | |
| | | GND | | | V24 | AG27 | R18 | | | | | |
| | | GND | | | AA24 | AG28 | R15 | | | | | |
| | | GND | | | AA27 | B28 | H18 | | | | | |
| | | GND | | | AA30 | E27 | H15 | | | | | |
| | | GND | | | AA33 | H21 | H21 | | | | | |
| | | GND | | | V27 | H24 | E21 | | | | | |
| | | GND | | | V30 | H27 | E18 | | | | | |
| | | GND | | | V33 | L21 | B18 | | | | | |
| | | GND | | | AB19 | L24 | B21 | | | | | |
| | | GND | | | AC12 | L27 | | | | | | |
| | | GND | | | AD7 | M19 | | | | | | |
| | | GND | | | AD8 | N24 | | | | | | |
| | | GND | | | AD9 | N27 | | | | | | |
| | | GND | | | AD10 | P21 | | | | | | |
| | | GND | | | AD11 | R24 | | | | | | |
| | | GND | | | AD12 | R27 | | | | | | |
| | | GND | | | AD15 | U21 | | | | | | |
| | | GND | | | AD18 | V24 | | | | | | |
| | | GND | | | AD21 | V27 | | | | | | |
| | | GND | | | AD24 | W20 | | | | | | |
| | | GND | | | AD27 | W22 | | | | | | |
| | | GND | | | AD30 | Y20 | | | | | | |
| | | GND | | | AD33 | | | | | | | |
| | | GND | | | AG7 | | | | | | | |
| | | GND | | | AG9 | | | | | | | |
| | | GND | | | AG12 | | | | | | | |
| | | GND | | | AG15 | | | | | | | |
| | | GND | | | AG17 | | | | | | | |
| | | GND | | | AG18 | | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | AG21 | | | | | | | |
| | | GND | | | AG24 | | | | | | | |
| | | GND | | | AG27 | | | | | | | |
| | | GND | | | AG30 | | | | | | | |
| | | GND | | | P33 | | | | | | | |
| | | GND | | | AG33 | W8 | AA1 | | | | | |
| | | GND | | | AK7 | W7 | AA3 | | | | | |
| | | GND | | | AK9 | V18 | AA6 | | | | | |
| | | GND | | | AK12 | V15 | T7 | | | | | |
| | | GND | | | AK15 | V12 | V9 | | | | | |
| | | GND | | | AK18 | V10 | AA9 | | | | | |
| | | GND | | | AK21 | AH27 | AA12 | | | | | |
| | | GND | | | AK24 | AG9 | V12 | | | | | |
| | | GND | | | AK27 | AG7 | V15 | | | | | |
| | | GND | | | AK30 | AG24 | AA15 | | | | | |
| | | GND | | | AK33 | AG21 | | | | | | |
| | | GND | | | AN7 | AG18 | | | | | | |
| | | GND | | | AN9 | AG15 | | | | | | |
| | | GND | | | AN12 | AG12 | | | | | | |
| | | GND | | | AN15 | AD9 | | | | | | |
| | | GND | | | AN18 | AD7 | | | | | | |
| | | GND | | | AN21 | AD21 | | | | | | |
| | | GND | | | AN24 | AD18 | | | | | | |
| | | GND | | | AN27 | AD15 | | | | | | |
| | | GND | | | AN30 | AD12 | | | | | | |
| | | GND | | | AN33 | AA9 | | | | | | |
| | | GND | | | AN34 | AA7 | | | | | | |
| | | GND | | | AP33 | AA20 | | | | | | |
| | | GND | | | B7 | AA18 | | | | | | |
| | | GND | | | B9 | AA15 | | | | | | |
| | | GND | | | B12 | AA12 | | | | | | |
| | | GND | | | B15 | | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | B18 | | | | | | | |
| | | GND | | | B21 | | | | | | | |
| | | GND | | | B24 | | | | | | | |
| | | GND | | | B27 | | | | | | | |
| | | GND | | | B30 | | | | | | | |
| | | GND | | | B33 | | | | | | | |
| | | GND | | | B34 | | | | | | | |
| | | GND | | | E7 | | | | | | | |
| | | GND | | | E9 | | | | | | | |
| | | GND | | | E12 | | | | | | | |
| | | GND | | | E15 | | | | | | | |
| | | GND | | | A2 | A2 | D1 | | | | | |
| | | GND | | | A3 | A3 | D2 | | | | | |
| | | GND | | | A6 | A4 | D3 | | | | | |
| | | GND | | | AA1 | A5 | D4 | | | | | |
| | | GND | | | AA2 | A6 | D5 | | | | | |
| | | GND | | | AA3 | AA1 | D6 | | | | | |
| | | GND | | | AA4 | AA2 | E3 | | | | | |
| | | GND | | | AA5 | AA3 | E6 | | | | | |
| | | GND | | | AA6 | AA4 | F1 | | | | | |
| | | GND | | | AA7 | AA5 | F2 | | | | | |
| | | GND | | | AB3 | AA6 | F3 | | | | | |
| | | GND | | | AB6 | AB3 | F4 | | | | | |
| | | GND | | | AB7 | AB6 | F5 | | | | | |
| | | GND | | | AB9 | AC1 | F6 | | | | | |
| | | GND | | | AB10 | AC2 | G3 | | | | | |
| | | GND | | | AB11 | AC3 | G6 | | | | | |
| | | GND | | | AB12 | AC4 | H1 | | | | | |
| | | GND | | | AC1 | AC5 | H2 | | | | | |
| | | GND | | | AC2 | AC6 | H3 | | | | | |
| | | GND | | | AC3 | AD3 | H4 | | | | | |
| | | GND | | | AC4 | AD6 | H5 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | AC5 | AE1 | J2 | | | | | |
| | | GND | | | AC6 | AE2 | J4 | | | | | |
| | | GND | | | AC7 | AE3 | H6 | | | | | |
| | | GND | | | AC8 | AE4 | K2 | | | | | |
| | | GND | | | AD3 | AE5 | K3 | | | | | |
| | | GND | | | AD6 | AE6 | K4 | | | | | |
| | | GND | | | AE1 | AF1 | K5 | | | | | |
| | | GND | | | AE2 | AF2 | K6 | | | | | |
| | | GND | | | AE3 | AF3 | K7 | | | | | |
| | | GND | | | AE4 | AF6 | L1 | | | | | |
| | | GND | | | AE5 | AG1 | L2 | | | | | |
| | | GND | | | AE6 | AG2 | M1 | | | | | |
| | | GND | | | AF3 | AG3 | M2 | | | | | |
| | | GND | | | AF6 | AG4 | N2 | | | | | |
| | | GND | | | AG1 | AG5 | N4 | | | | | |
| | | GND | | | AG2 | AG6 | N5 | | | | | |
| | | GND | | | AG3 | AH2 | N6 | | | | | |
| | | GND | | | AG4 | AH3 | N7 | | | | | |
| | | GND | | | AG5 | AH4 | P2 | | | | | |
| | | GND | | | AG6 | AH5 | P3 | | | | | |
| | | GND | | | AH3 | AH6 | P5 | | | | | |
| | | GND | | | AH5 | B1 | P7 | | | | | |
| | | GND | | | AH6 | B2 | R1 | | | | | |
| | | GND | | | AJ1 | B3 | R2 | | | | | |
| | | GND | | | AJ2 | B4 | R3 | | | | | |
| | | GND | | | AJ3 | B5 | R4 | | | | | |
| | | GND | | | AJ4 | B6 | R5 | | | | | |
| | | GND | | | AJ5 | C1 | R6 | | | | | |
| | | GND | | | AJ6 | C2 | R7 | | | | | |
| | | GND | | | AK3 | C3 | T3 | | | | | |
| | | GND | | | AK6 | C6 | T6 | | | | | |
| | | GND | | | AL1 | D1 | U1 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | AL2 | D2 | U2 | | | | | |
| | | GND | | | AL3 | D3 | U3 | | | | | |
| | | GND | | | AL4 | D4 | U4 | | | | | |
| | | GND | | | AL5 | D5 | U5 | | | | | |
| | | GND | | | AL6 | D6 | U6 | | | | | |
| | | GND | | | AM3 | E3 | V3 | | | | | |
| | | GND | | | AM6 | E6 | V6 | | | | | |
| | | GND | | | AN1 | F1 | W1 | | | | | |
| | | GND | | | AN2 | F2 | W2 | | | | | |
| | | GND | | | AN3 | F3 | W3 | | | | | |
| | | GND | | | AN4 | F4 | W4 | | | | | |
| | | GND | | | AN5 | F5 | W5 | | | | | |
| | | GND | | | AN6 | F6 | W6 | | | | | |
| | | GND | | | AP2 | G3 | | | | | | |
| | | GND | | | AP3 | G6 | | | | | | |
| | | GND | | | AP6 | H1 | | | | | | |
| | | GND | | | B1 | H2 | | | | | | |
| | | GND | | | B2 | H3 | | | | | | |
| | | GND | | | B3 | H4 | | | | | | |
| | | GND | | | B4 | H5 | | | | | | |
| | | GND | | | B5 | H6 | | | | | | |
| | | GND | | | B6 | J3 | | | | | | |
| | | GND | | | C3 | J5 | | | | | | |
| | | GND | | | C6 | J6 | | | | | | |
| | | GND | | | D1 | K1 | | | | | | |
| | | GND | | | D2 | K2 | | | | | | |
| | | GND | | | D3 | K3 | | | | | | |
| | | GND | | | D4 | K4 | | | | | | |
| | | GND | | | D5 | K5 | | | | | | |
| | | GND | | | D6 | K6 | | | | | | |
| | | GND | | | E3 | L3 | | | | | | |
| | | GND | | | E6 | M1 | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | F1 | M2 | | | | | | |
| | | GND | | | F2 | M3 | | | | | | |
| | | GND | | | F3 | M4 | | | | | | |
| | | GND | | | F4 | M5 | | | | | | |
| | | GND | | | F5 | N3 | | | | | | |
| | | GND | | | F6 | N7 | | | | | | |
| | | GND | | | G3 | N8 | | | | | | |
| | | GND | | | G5 | N9 | | | | | | |
| | | GND | | | G6 | N10 | | | | | | |
| | | GND | | | H1 | P1 | | | | | | |
| | | GND | | | H2 | P2 | | | | | | |
| | | GND | | | H3 | P3 | | | | | | |
| | | GND | | | H4 | P4 | | | | | | |
| | | GND | | | H5 | P5 | | | | | | |
| | | GND | | | H6 | P6 | | | | | | |
| | | GND | | | J3 | R1 | | | | | | |
| | | GND | | | J6 | R2 | | | | | | |
| | | GND | | | K1 | R3 | | | | | | |
| | | GND | | | K2 | R4 | | | | | | |
| | | GND | | | K3 | R5 | | | | | | |
| | | GND | | | K4 | T3 | | | | | | |
| | | GND | | | K5 | U1 | | | | | | |
| | | GND | | | K6 | U2 | | | | | | |
| | | GND | | | L3 | U3 | | | | | | |
| | | GND | | | L6 | U4 | | | | | | |
| | | GND | | | M1 | U5 | | | | | | |
| | | GND | | | M2 | U7 | | | | | | |
| | | GND | | | M3 | U8 | | | | | | |
| | | GND | | | M4 | U9 | | | | | | |
| | | GND | | | M5 | U10 | | | | | | |
| | | GND | | | M6 | V3 | | | | | | |
| | | GND | | | M7 | V6 | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | N3 | W1 | | | | | | |
| | | GND | | | N6 | W2 | | | | | | |
| | | GND | | | N7 | W3 | | | | | | |
| | | GND | | | P1 | W4 | | | | | | |
| | | GND | | | P2 | W5 | | | | | | |
| | | GND | | | P3 | W6 | | | | | | |
| | | GND | | | P4 | Y3 | | | | | | |
| | | GND | | | P5 | Y5 | | | | | | |
| | | GND | | | P6 | Y6 | | | | | | |
| | | GND | | | P7 | | | | | | | |
| | | GND | | | P9 | | | | | | | |
| | | GND | | | P10 | | | | | | | |
| | | GND | | | P11 | | | | | | | |
| | | GND | | | P12 | | | | | | | |
| | | GND | | | R3 | | | | | | | |
| | | GND | | | R6 | | | | | | | |
| | | GND | | | R7 | | | | | | | |
| | | GND | | | R8 | | | | | | | |
| | | GND | | | T1 | | | | | | | |
| | | GND | | | T2 | | | | | | | |
| | | GND | | | T3 | | | | | | | |
| | | GND | | | T4 | | | | | | | |
| | | GND | | | T5 | | | | | | | |
| | | GND | | | T6 | | | | | | | |
| | | GND | | | T7 | | | | | | | |
| | | GND | | | U1 | | | | | | | |
| | | GND | | | U2 | | | | | | | |
| | | GND | | | U3 | | | | | | | |
| | | GND | | | U4 | | | | | | | |
| | | GND | | | U5 | | | | | | | |
| | | GND | | | V3 | | | | | | | |
| | | GND | | | V5 | | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | V6 | | | | | | | |
| | | GND | | | V7 | | | | | | | |
| | | GND | | | V9 | | | | | | | |
| | | GND | | | V10 | | | | | | | |
| | | GND | | | V11 | | | | | | | |
| | | GND | | | V12 | | | | | | | |
| | | GND | | | W1 | | | | | | | |
| | | GND | | | W2 | | | | | | | |
| | | GND | | | W3 | | | | | | | |
| | | GND | | | W4 | | | | | | | |
| | | GND | | | W5 | | | | | | | |
| | | GND | | | W6 | | | | | | | |
| | | GND | | | Y3 | | | | | | | |
| | | GND | | | Y6 | | | | | | | |
| | | GND | | | Y7 | | | | | | | |
| | | GND | | | AC10 | | | | | | | |
| | | GND | | | W10 | V8 | | | | | | |
| | | GND | | | R10 | P8 | | | | | | |
| | | GND | | | E18 | A27 | B1 | | | | | |
| | | GND | | | E21 | B12 | B3 | | | | | |
| | | GND | | | E24 | B15 | B6 | | | | | |
| | | GND | | | E27 | B18 | B9 | | | | | |
| | | GND | | | E30 | B21 | E9 | | | | | |
| | | GND | | | E33 | B24 | H7 | | | | | |
| | | GND | | | G17 | B27 | E12 | | | | | |
| | | GND | | | H7 | B7 | B12 | | | | | |
| | | GND | | | H9 | B9 | B15 | | | | | |
| | | GND | | | H12 | E12 | E15 | | | | | |
| | | GND | | | H15 | E15 | | | | | | |
| | | GND | | | H18 | E18 | | | | | | |
| | | GND | | | H21 | E21 | | | | | | |
| | | GND | | | H24 | E24 | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | H27 | E7 | | | | | | |
| | | GND | | | H30 | E9 | | | | | | |
| | | GND | | | H33 | H12 | | | | | | |
| | | GND | | | K7 | H15 | | | | | | |
| | | GND | | | K8 | H16 | | | | | | |
| | | GND | | | K9 | H18 | | | | | | |
| | | GND | | | L10 | H7 | | | | | | |
| | | GND | | | L11 | H9 | | | | | | |
| | | GND | | | L12 | J7 | | | | | | |
| | | GND | | | L15 | L11 | | | | | | |
| | | GND | | | L18 | L15 | | | | | | |
| | | GND | | | L21 | L18 | | | | | | |
| | | GND | | | L24 | | | | | | | |
| | | GND | | | L27 | | | | | | | |
| | | GND | | | L30 | | | | | | | |
| | | GND | | | L33 | | | | | | | |
| | | GND | | | N13 | | | | | | | |
| | | GND | | | N14 | | | | | | | |
| | | GND | | | N15 | | | | | | | |
| | | GND | | | N16 | | | | | | | |
| | | GND | | | N20 | | | | | | | |
| | | GND | | | P24 | | | | | | | |
| | | GND | | | P27 | | | | | | | |
| | | GND | | | P30 | | | | | | | |
| | | GND | | | AA13 | M11 | J12 | | | | | |
| | | GND | | | AA15 | M13 | K12 | | | | | |
| | | GND | | | AA17 | M15 | J11 | | | | | |
| | | GND | | | AA19 | M17 | J9 | | | | | |
| | | GND | | | AA21 | N12 | K10 | | | | | |
| | | GND | | | P14 | N14 | K8 | | | | | |
| | | GND | | | P16 | N16 | L9 | | | | | |
| | | GND | | | P18 | N18 | M8 | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | P20 | P11 | N9 | | | | | |
| | | GND | | | R13 | P13 | P8 | | | | | |
| | | GND | | | R15 | P15 | R9 | | | | | |
| | | GND | | | R17 | P17 | P10 | | | | | |
| | | GND | | | R19 | R12 | R11 | | | | | |
| | | GND | | | R21 | R14 | R12 | | | | | |
| | | GND | | | T14 | R16 | P12 | | | | | |
| | | GND | | | T16 | R18 | N13 | | | | | |
| | | GND | | | T18 | T11 | M12 | | | | | |
| | | GND | | | T20 | T13 | L13 | | | | | |
| | | GND | | | T22 | T15 | L11 | | | | | |
| | | GND | | | U13 | T17 | N11 | | | | | |
| | | GND | | | U15 | U12 | M10 | | | | | |
| | | GND | | | U17 | U14 | | | | | | |
| | | GND | | | U19 | U16 | | | | | | |
| | | GND | | | U21 | U18 | | | | | | |
| | | GND | | | V14 | N19 | | | | | | |
| | | GND | | | V16 | P10 | | | | | | |
| | | GND | | | V18 | P19 | | | | | | |
| | | GND | | | V20 | R19 | | | | | | |
| | | GND | | | W13 | | | | | | | |
| | | GND | | | W15 | | | | | | | |
| | | GND | | | W17 | | | | | | | |
| | | GND | | | W19 | | | | | | | |
| | | GND | | | W21 | | | | | | | |
| | | GND | | | Y14 | | | | | | | |
| | | GND | | | Y16 | | | | | | | |
| | | GND | | | Y18 | | | | | | | |
| | | GND | | | Y20 | | | | | | | |
| | | GND | | | Y22 | | | | | | | |
| | | GND | | | AB13 | | | | | | | |
| | | GND | | | AB14 | | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | GND | | | AB15 | | | | | | | |
| | | GND | | | P13 | | | | | | | |
| | | GND | | | P22 | | | | | | | |
| | | GND | | | R12 | | | | | | | |
| | | GND | | | V22 | | | | | | | |
| | | GND | | | Y13 | | | | | | | |
| | | VCCPD2 | | | R24 | P20 | L14 | | | | | |
| | | VCCPD2 | | | R25 | | | | | | | |
| | | VCCPD1 | | | W24 | T20 | P14 | | | | | |
| | | VCCPD1 | | | W25 | | | | | | | |
| | | VCCPD8 | | | AD19 | Y16 | R13 | | | | | |
| | | VCCPD8 | | | AD20 | | | | | | | |
| | | VCCPD7 | | | AD16 | Y12 | R8 | | | | | |
| | | VCCPD7 | | | AD17 | | | | | | | |
| | | VCCPD4 | | | L16 | J13 | J8 | | | | | |
| | | VCCPD4 | | | L17 | | | | | | | |
| | | VCCPD3 | | | L19 | J17 | J13 | | | | | |
| | | VCCPD3 | | | L20 | | | | | | | |
| | | NC | | | AB16 | AE23 | | | | | | |
| | | NC | | | AB17 | AB20 | | | | | | |
| | | NC | | | AB22 | AA19 | | | | | | |
| | | NC | | | AC17 | Y15 | | | | | | |
| | | NC | | | AJ29 | AB18 | | | | | | |
| | | NC | | | AJ30 | AA17 | | | | | | |
| | | NC | | | AK31 | AB16 | | | | | | |
| | | NC | | | AK32 | AA11 | | | | | | |
| | | NC | | | AK34 | K14 | | | | | | |
| | | NC | | | AL32 | G17 | | | | | | |
| | | NC | | | AL33 | J18 | | | | | | |
| | | NC | | | AL34 | K19 | | | | | | |
| | | NC | | | D32 | L19 | | | | | | |
| | | NC | | | D33 | J20 | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | NC | | | E31 | | | | | | | |
| | | NC | | | E32 | | | | | | | |
| | | NC | | | F30 | | | | | | | |
| | | NC | | | G30 | | | | | | | |
| | | NC | | | G31 | | | | | | | |
| | | NC | | | H29 | | | | | | | |
| | | NC | | | K22 | | | | | | | |
| | | NC | | | M13 | | | | | | | |
| | | NC | | | N19 | | | | | | | |
| | | NC | | | N22 | | | | | | | |
| | | NC | | | W7 | | | | | | | |
| | | NC | | | W8 | | | | | | | |
| | | NC | | | W12 | | | | | | | |
| | | NC | | | AK29 | | | | | | | |
| | | NC | | | AD23 | | | | | | | |
| | | NC | | | AD22 | | | | | | | |
| | | NC | | | AE22 | | | | | | | |
| | | NC | | | AG23 | | | | | | | |
| | | NC | | | AC19 | | | | | | | |
| | | NC | | | AH22 | | | | | | | |
| | | NC | | | AG13 | | | | | | | |
| | | NC | | | AE13 | | | | | | | |
| | | NC | | | AF10 | | | | | | | |
| | | NC | | | H13 | | | | | | | |
| | | NC | | | M14 | | | | | | | |
| | | NC | | | J14 | | | | | | | |
| | | NC | | | G18 | | | | | | | |
| | | NC | | | G19 | | | | | | | |
| | | NC | | | M20 | | | | | | | |
| | | NC | | | M22 | | | | | | | |
| | | NC | | | L22 | | | | | | | |
| | | NC | | | L23 | | | | | | | |

| Bank Number | VREF Group | Pin Name/Function | Optional Function(s) | Configuration Function | EP1AGX60EF1152 | EP1AGX60DF780 | EP1AGX60CF484 | x8/x9 Mode | | x16/x18 Mode | | x32/x36 Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) | DQ group for DQS mode (F780, F484) (Note 1) | DQ group for DQS mode (F1152) |
| | | NC | | | M24 | | | | | | | |

**Note:**

1. The DQS/DQ mode shown in this column applies to the largest device package in the pin list.
   Smaller packages may not have the pins to support some of the DQS groups.
   To determine the supported DQS/DQ groups, check the pin availability for the target device package.
   For example, for the EP1AGX60CF484 package, there are only two x8 groups, but no x9 group.

| Pin Name | Pin Type (1st, 2nd, and 3rd Functions) | Pin Description |
|---|---|---|
| | ***Supply and Reference Pins*** | |
| VCCINT | Power | 1.2-V internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HSTL, SSTL, differential HSTL, and differential SSTL I/O standards. |
| VCCIO[1..4,7,8] | Power | I/O supply voltage pins for banks 1-4, 7, and 8. Each bank can support a different voltage level. Supported voltages are 1.5V, 1.8V, 2.5V, and 3.3V. VCCIO[4,7,8] also support 1.2V for 1.2V HSTL operation.For specific I/O standards supported by Arria GX FPGA refer to the Arria GX Handbook. |
| VCCPD[1..4,7,8] | Power | Dedicated power pins. This 3.3-V supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and the JTAG pins. VCCPD powers the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. |
| GND | Ground | Device ground pins. |
| VREFB[1..4,7,8]N[2..0] | Input | Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for that bank. All the VREF pins within a bank are shorted together. |
| VCC_PLL5_OUT | Power | External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p, and PLL5_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL5 in bank 9 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin. |
| VCC_PLL6_OUT | Power | External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p, and PLL6_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL6 in bank 10 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin. |
| VCC_PLL11_OUT | Power | External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p, and PLL11_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL11 in bank 11 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin. |
| VCC_PLL12_OUT | Power | External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p, and PLL12_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL12 in bank 12 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin. |
| VCCA_PLL[1,2,5..8,11,12] | Power | 1.2-V analog power for PLL[1,2,5..8,11,12]. |
| VCCD_PLL[1,2,5..8,11,12] | Power | 1.2-V digital power for PLL[1,2,5..8,11,12]. |
| GNDA_PLL[1,2,5..8,11,12] | Ground | Analog ground for PLL[1,2,5..8,11,12]. |
| NC | No Connect | Do not drive any signals into this pin. |
| | ***Dedicated Configuration/JTAG Pins*** | |

| Pin Name | Pin Type (1st, 2nd, and 3rd Functions) | Pin Description |
|---|---|---|
| nIO_PULLUP | Input | Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns it on. |
| VCCSEL | Input | Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input), DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory. |
| DCLK | Input (PS, FPP)<br>Output (AS) | Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Arria GX device. In AS mode, DCLK is an output from the Arria GX device that provides timing for the configuration interface. |
| MSEL[3..0] | Input | Configuration input pins that set the Arria GX device configuration scheme. |
| nCE | Input | Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCONFIG | Input | Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic-high level initiates reconfiguration. |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin. |
| nCEO | Output | Output that drives low when device configuration is complete. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin. |
| PORSEL | Input | Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects a POR time of about 12 ms and a logic low selects a POR time of about 100 ms. |
| ***Optional/Dual-Purpose Configuration Pins*** | | |
| nCSO | I/O, Output | Output control signal from the Arria GX FPGA to the serial configuration device in AS mode that enables the configuration device. |
| ASDO | I/O, Output | Control signal from the Arria GX FPGA to the serial configuration device in AS mode used to read out configuration data. |

| Pin Name | Pin Type (1st, 2nd, and 3rd Functions) | Pin Description |
|---|---|---|
| CRC_ERROR | I/O, Output | Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled. |
| DEV_CLRn | I/O, Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. |
| DEV_OE | I/O, Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. |
| DATA0 | I/O, Input | Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete. |
| DATA[6..1] | I/O, Input | Dual-purpose configuration input data pins. The DATA[7..0] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration. |
| DATA7 | I/O, Bidirectional | In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the nRS signal is strobed low. |
| INIT_DONE | I/O, Output (open-drain) | This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. |
| nCS, CS | I/O, Input | These are chip-select inputs that enable the Arria GX device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active-high enable, use the CS pin and drive the nCS pin low. If a design requires an active-low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration. |
| nRS | I/O, Input | Read strobe input pin. A low input directs the device to drive the RDYnBSY signal on the DATA7 pin. In non-PPA schemes, it functions as a user I/O during configuration, which means it is tri-stated. This pin can be used as a user I/O pin after configuration. |
| nWS | I/O, Input | Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. |
| RDYnBSY | I/O, Output | Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration. |
| PGM[2..0] | I/O, Output | These output pins control one of eight pages in the memory (either flash or enhanced configuration device) when using a remote system update mode. When not using remote update or local update configuration modes, these pins are user I/O pins. |

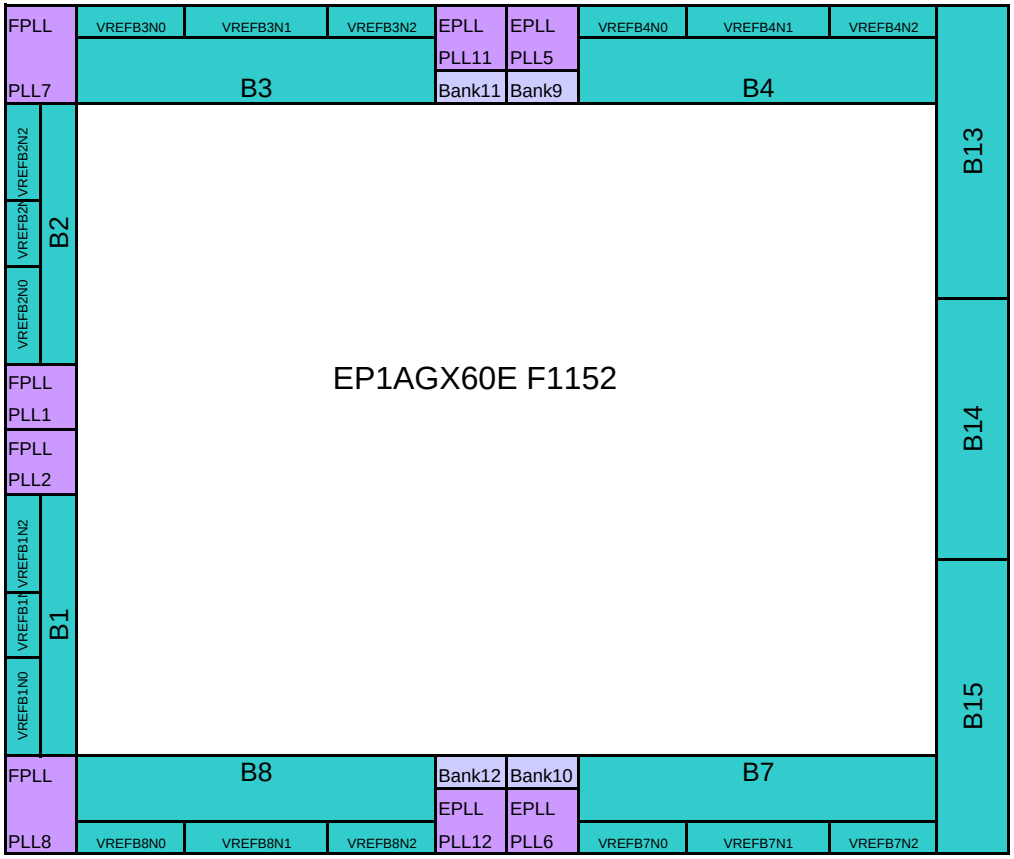
| Pin Name | Pin Type (1st, 2nd, and 3rd Functions) | Pin Description |
|---|---|---|
| RUnLU | I/O, Input | Input that selects between remote update and local update. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects remote update and a logic low selects local update. When not using remote update or local update configuration modes, this pin is available as general-purpose user I/O pin. |
| TCK | Input | Dedicated JTAG input pin. |
| TMS | Input | Dedicated JTAG input pin. |
| TDI | Input | Dedicated JTAG input pin. |
| TDO | Output | Dedicated JTAG output pin. |
| TRST | Input | Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit. |
| ***Clock and PLL Pins*** | | |
| CLK[1,3]p | Clock, Input | Dedicated clock input pins 1 and 3 that can also be used for data inputs. These pins do not support OCT Rd and cannot be used as output pins. The programmable weak pull up resistor is not supported on these pins. |
| CLK[1,3]n | Clock, Input | Dedicated negative clock input pins for differential clock input that can also be used for data inputs. These pins do not support OCT Rd and cannot be used as output pins. The programmable weak pull up resistor is not supported on these pins. |
| CLK[2,0]p/DIFFIO_RX_C[1,0]p | I/O, Clock | These pins can be used as I/O pins, clock input pins, or positive terminal data pins of differential receiver channels. |
| CLK[2,0]n/DIFFIO_RX_C[1,0]n | I/O, Clock | These pins can be used as I/O pins, negative clock input pins for differential clock input, or negative data pins of differential receiver channels. |
| CLK[4-7,12-15]p | I/O, Clock | These pins can be used as I/O pins or clock input pins. |
| CLK[4-7,12-15]n | I/O, Clock | These pins can be used as I/O pins or negative clock input pins for differential clock inputs. |
| PLL_ENA | Input | Dedicated input pin that drives the optional pllena port of all or a set of PLLs. |
| FPLL[8..7]CLKp | Clock, Input | Dedicated positive clock inputs for fast PLLs (PLLs 7 and 8), which can also be used for data inputs. These pins do not support OCT Rd and cannot be used as output pins. The programmable weak pull up resistor is not supported on these pins. |
| FPLL[8..7]CLKn | Clock, Input | Dedicated negative clock inputs associated with the FPLL[7,8]CLKp pins, which can also be used for data inputs. These pins do not support OCT Rd and cannot be used as output pins. The programmable weak pull up resistor is not supported on these pins. |
| PLL5_OUT[1,0]p | Output | Optional positive external clock outputs [1,0] from enhanced PLL5. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL5). |
| PLL5_OUT[1,0]n | Output | Optional negative external clock outputs [1,0] from enhanced PLL5. If the clock outputs are single-ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase. |
| PLL6_OUT[1,0]p | Output | Optional positive external clock outputs [1,0] from enhanced PLL6. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL6). |

| Pin Name | Pin Type (1st, 2nd, and 3rd Functions) | Pin Description |
|---|---|---|
| PLL6_OUT[1,0]n | Output | Optional negative external clock outputs [1,0] from enhanced PLL6. If the clock outputs are single-ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase. |
| PLL11_OUT[1,0]p | Output | Optional positive external clock outputs [1,0] from enhanced PLL11. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL11). |
| PLL11_OUT[1,0]n | Output | Optional negative external clock outputs [1,0] from enhanced PLL11. If the clock outputs are single-ended, then each pair of pins (i.e., PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase. |
| PLL12_OUT[1,0]p | Output | Optional positive external clock outputs [1,0] from enhanced PLL12. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL12). |
| PLL12_OUT[1,0]n | Output | Optional negative external clock outputs [1,0] from enhanced PLL12. If the clock outputs are single-ended, then each pair of pins (i.e., PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase. |
| PLL[6..5]_FBp/OUT2p | I/O, Input, Output | These pins can be used as I/O pins, positive external feedback input pins, or external clock outputs for PLL[6,5]. |
| PLL[6..5]_FBn/OUT2n | I/O, Input, Output | These pins can be used as I/O pins, negative external feedback input PLL[6,5]_FBp, or negative terminal clock output pins for differential clock output. |
| PLL[12..11]_FBp/OUT2p | I/O, Input, Output | These pins can be used as I/O pins, positive external feedback input pins, or positive external clock outputs for PLL[12..11]. |
| PLL[12..11]_FBn/OUT2n | I/O, Input, Output | These pins can be used as I/O pins, negative external feedback input PLL[12..11]_FBp, or negative external clock output pins for differential clock output. |
| ***Dual-Purpose Differential and External Memory Interface Pins*** | | |
| DIFFIO_RX[50..1]p | IO, Input | Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. |
| DIFFIO_RX[50..1]n | IO, Input | Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. |
| DIFFIO_TX[51..0]p | IO, Output | Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. |
| DIFFIO_TX[51..0]n | IO, Output | Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. |
| DQS[17..0][T,B] | DQS | Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic. |

| Pin Name | Pin Type (1st, 2nd, and 3rd Functions) | Pin Description |
|---|---|---|
| DQ[17..0][T,B] | DQ | Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list. |
| ***Transceiver (I/O Banks) Pins*** | | |
| VCCP | Power | GX bank [15..13] PCS power. This power is connected to 1.2 V. |
| VCCR | Power | GX bank [15..13] receiver analog power. This power is connected to 1.2 V. |
| VCCT_B[15..13] | Power | GX bank [15..13] transmitter analog power. This power is connected to 1.2 V. |
| VCCA | Power | GX bank [15..13] analog power. This power is connected to 3.3 V. |
| VCCH_B[15..13] | Power | GX bank [15..13] transmitter driver analog power. This power is connected to 1.2 V or 1.5 V. |
| VCCL_B[15..13] | Power | GX bank [15..13] VCO analog power. This power is connected to 1.2 V. |
| GXB_RX[11..0]p | I, Input | High-speed positive differential receiver channels. |
| GXB_RX[11..0]n | I, Input | High-speed negative differential receiver channels. |
| GXB_TX[11..0]p | O, Output | High-speed positive differential transmitter channel. |
| GXB_TX[11..0]n | O, Output | High-speed negative differential transmitter channels. |
| REFCLK[0,1]_B[15..13]p | I, Input | High-speed differential I/O reference clock positive. This pin is powered by 1.2-V VCCT_B[15..13]. |
| REFCLK[0,1]_B[15..13]n | I, Input | High-speed differential I/O reference clock negative. This pin is powered by 1.2-V VCCT_B[15..13]. |
| RREFB[15..13] | I, Input | Reference resistor for GX side banks. |

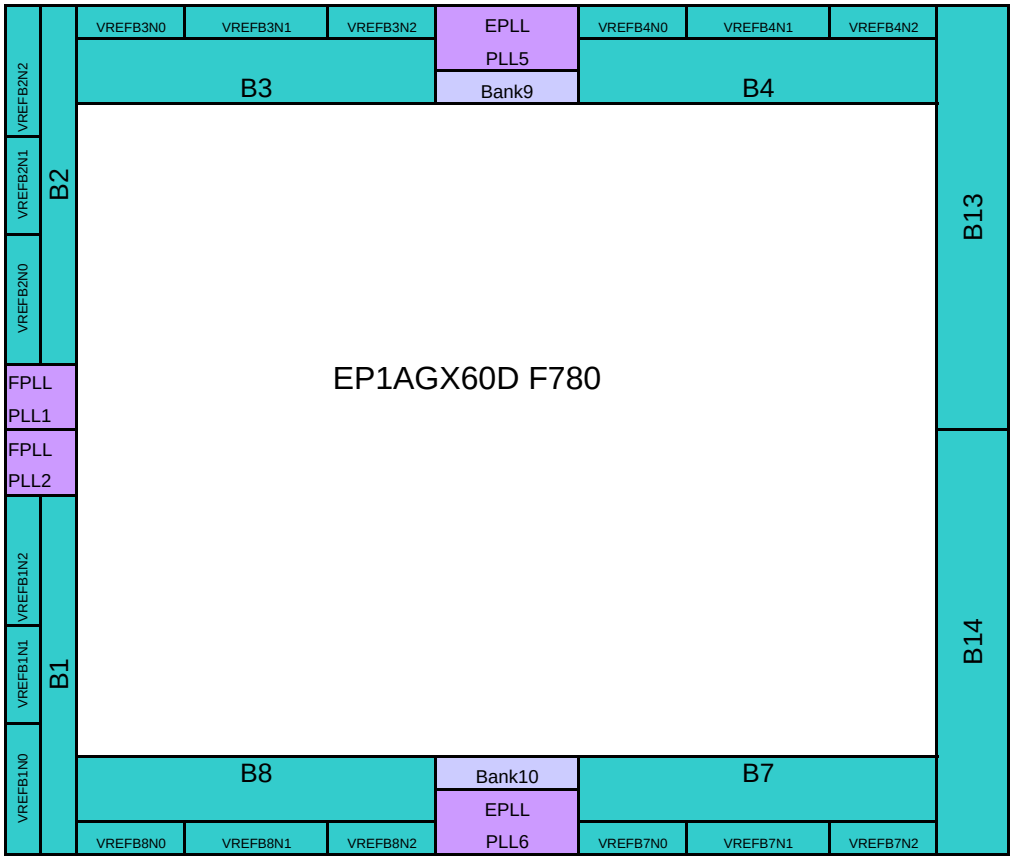
**Note:**

1) These descriptions are created based on the Arria GX device with the largest density, EP1AGX90E.

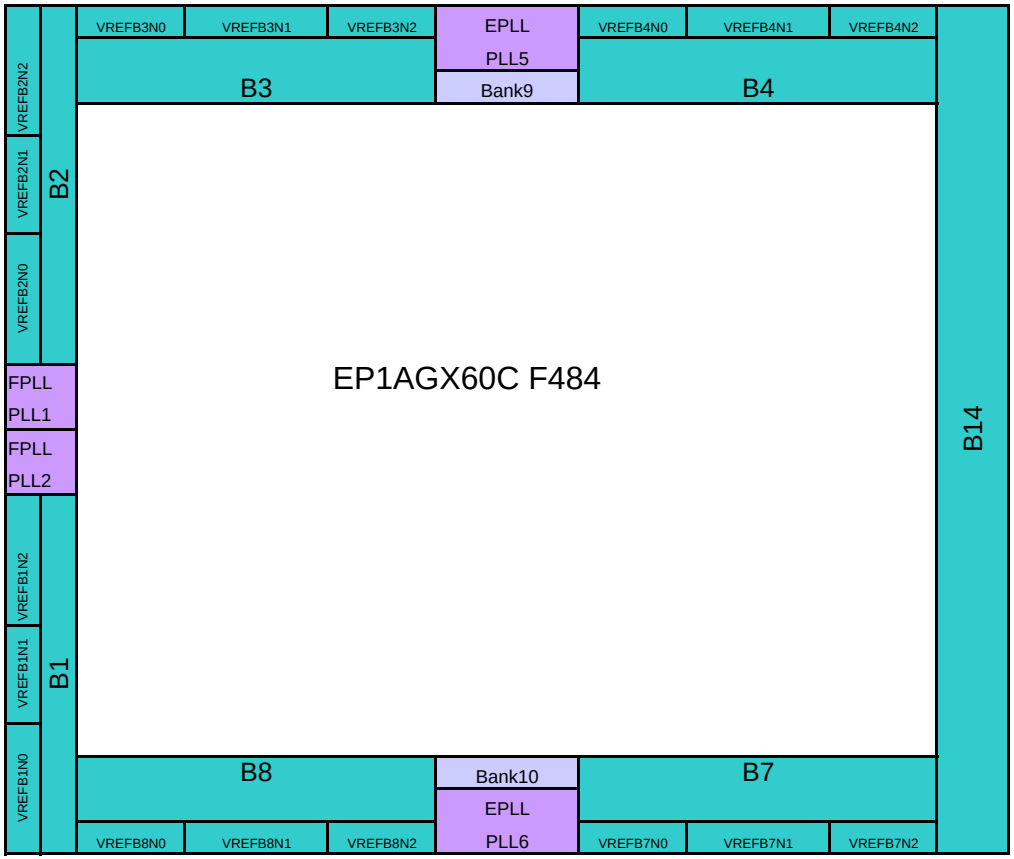



**Notes:**

1. This is a top view of the silicon die. For flip-chip packages, the die is mounted upsided-down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus ® II software for exact locations.




**Notes:**
1. This is a top view of the silicon die. For flip-chip packages, the die is mounted upsided-down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus II software for exact locations.




**Notes:**
1. This is a top view of the silicon die. For flip-chip packages, the die is mounted upsided-down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus II software for exact locations.

| Version History | Date | Changes Made |
|---|---|---|
| 1.0 | 6/22/2007 | Initial release |
| 1.1 | 7/27/2007 | Added F484 package |
| 1.2 | 12/21/2007 | Updated pin descriptions for VCCINT, VCCIO, TEMPDIODEp and TEMPDIODEn |
| | | Removed Bank 7 reference for GND pin AF7 (F1152)/ AC7 (F780)/ Y2 (F484) in Pin List |
| 1.3 | 9/8/2008 | Removed RUP4,RUP7,RDN4,RDN7 from Pin List and Pin Definitions |
| 1.4 | 5/21/2009 | Removed TEMPDIODEp and TEMPDIODEn from Pin List and Pin Definitions |
| | | |
| | | |
| | | |
| | | |