

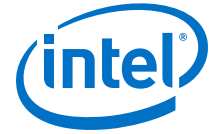
# Intel<sup>®</sup> Agilex<sup>™</sup> Device Family Pin Connection Guidelines



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## 1. Intel® Agilex™ Device Family Pin Connection Guidelines

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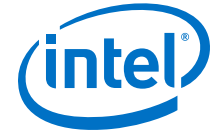
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## 1.1. Intel® Agilex™ FPGA Core Pins

### 1.1.1. Clock and PLL Pins

**Note:** Intel® recommends that you create an Intel Quartus® Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 1. Clock and PLL Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK_[T,B]_2[A,B,C,D]_[0:1][p,n] CLK_[T,B]_3[A,B,C,D]_[0:1][p,n]	I/O, Clock Input	Dedicated high speed clock input pins that can be used for data inputs or outputs. Differential input OCT Rd, single-ended input OCT Rt, and single-ended output OCT Rs are supported on these pins. When you do not use these pins as dedicated clock pins, you can use them as regular I/O pins. Supported I/O standards: <ul style="list-style-type: none"> <li>• 1.2V</li> <li>• 1.5V True Differential Signaling</li> </ul> Maximum clock frequency is 400MHz. Edge rate is 250ps at 20–80%. These pins have an internal 10-kΩ pull up.	Tie the unused pins to GND. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.
PLL_[2] [A,B,C,D]_[T,B]_FB[0:1] PLL_[3] [A,B,C,D]_[T,B]_FB[0:1]	I/O, Clock	Dual-purpose I/O pins that can be used as single-ended inputs, single-ended outputs, or external feedback input pins. For more information about the supported pins, refer to the device pin-out file. Supported I/O standards: <ul style="list-style-type: none"> <li>• 1.2V</li> <li>• 1.5V True Differential Signaling</li> </ul> Maximum clock frequency is 400MHz. Edge rate is 250ps at 20–80%.	Tie the unused pins to GND. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.

*continued...*



Pin Name	Pin Functions	Pin Description	Connection Guidelines
		These pins have an internal 10-kΩ pull up.	
PLL_[2] [A,B,C,D]_[T,B]_CLKOU T[0:1][p,n] PLL_[3] [A,B,C,D]_[T,B]_CLKOU T[0:1][p,n]	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair. For more information about the supported pins, refer to the device pin-out file. Supported I/O standards: <ul style="list-style-type: none"> <li>• 1.2V</li> <li>• 1.5V True Differential Signaling</li> </ul> Maximum clock frequency is 400MHz. Edge rate is 250ps at 20–80%. These pins have an internal 10-kΩ pull up.	Tie the unused pins to GND. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.

### 1.1.2. Dedicated Configuration/JTAG Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 2. Dedicated Configuration/JTAG Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
TCK	Input	Dedicated JTAG test clock input pin located in the Secure Device Manager (SDM) bank. This pin can also be used to access the HPS JTAG chain. For more information, refer to the <a href="#">HPS JTAG Pins</a> on page 34. This pin support the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-down resistor. The maximum VIH is VCCIO + 5%. JTAG clock speed is 33 MHz for JTAG split mode. In the JTAG split mode, the SDM JTAG mode is independent of the HPS JTAG.	Connect this pin through a 1-kΩ pull-down resistor to GND. If the JTAG interface is not used, connect this pin through a 1-kΩ pull-down resistor to GND.
<i>continued...</i>			



Pin Name	Pin Functions	Pin Description	Connection Guidelines
		JTAG clock speed is 22 MHz for JTAG daisy-chain mode. In the JTAG daisy-chain mode, the HPS DAP TAP is daisy chained with the SDM mTAP.	
TMS	Input	Dedicated JTAG test mode select input pin located in the SDM bank. This pin can also be used to access the HPS JTAG chain. For more information, refer to the <a href="#">HPS JTAG Pins</a> on page 34. This pin support the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor. The maximum VIH is VCCIO + 5%.	Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCPGM supply. If the JTAG interface is not used, connect the TMS pin to the VCCPGM supply using a 1-kΩ resistor.
TDO	Output	Dedicated JTAG test data output pin located in the SDM bank. This pin can also be used to access the HPS JTAG chain. For more information, refer to the <a href="#">HPS JTAG Pins</a> on page 34. This pin support the 1.8-V single-ended I/O standard.	If the JTAG interface is not used, leave the TDO pin unconnected.
TDI	Input	Dedicated JTAG test data input pin located in the SDM bank. This pin can also be used to access the HPS JTAG chain. For more information, refer to the <a href="#">HPS JTAG Pins</a> on page 34. This pin support the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor. The maximum VIH is VCCIO + 5%.	Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCPGM supply. If the JTAG interface is not used, connect the TDI pin to the VCCPGM supply using a 1-kΩ resistor.
nSTATUS	Output	Configuration status pin. This pin is used to report configuration status after the configuration source has been selected. This pin can be used in GPIO, DTS, I2C, and LOANIO modes. This pin support the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor. The drive strength is 8 mA.	When you are using the Avalon®-ST configuration scheme, connect this pin to the configuration host. For other configuration schemes, you can use this pin to monitor the configuration status. This pin must be pulled up through a 10-kΩ resistor to VCCIO_SDM for all configuration schemes.
nCONFIG	Input	By default, this pin indicates configuration status. This pin can also be configured as a GPIO pin. This pin support the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor. The drive strength is 8 mA. Open-drain configuration pin.	When you use the Avalon-ST configuration scheme, connect this pin directly to the configuration host. When you use other configuration schemes, pull this pin to VCCIO_SDM through an external 10-KΩ pull-up resistor. When you use other configuration schemes, this pin can be used to restart configuration by driving it low and then high again.
OSC_CLK_1	Input	Reference clock source for SDM PLL.	You must provide an external clock source to this pin if you are using transceivers.
<i>continued...</i>			



Pin Name	Pin Functions	Pin Description	Connection Guidelines
		<p>This pin is used as the clock for device configuration and transceiver calibration.</p> <p>This pin support the 1.8-V single-ended I/O standard.</p> <p>This pin has an internal 20-kΩ pull-down resistor.</p> <p>The drive strength is 8 mA.</p>	<p>If you choose to use the external clock source for configuration and/or instantiate any transceivers in your design, you must provide a 25-MHz, 100-MHz, or 125-MHz free-running clock source to this pin and enable it in the Intel Quartus Prime software when you compile your design.</p> <p>If you are using the internal oscillator for configuration and do not instantiate any transceivers in your design, leave this pin unconnected.</p>

### 1.1.3. Optional/Dual-Purpose Configuration Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 3. Optional/Dual-Purpose Configuration Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
SDM_MISSION_DATA[31:0]	I/O, Input	<p>Dual-purpose configuration data input pins.</p> <p>Use SDM_MISSION_DATA[15:0] pins for Avalon Streaming Interface (Avalon-ST) x16 mode, SDM_MISSION_DATA [31:0] pins for Avalon-ST x32 mode, or as regular I/O pins.</p> <p>This pin support the 1.2-V I/O standard.</p>	<p>If these pins are not used as the dual-purpose pins and they are not used as I/O pins, leave these pins unconnected.</p>
AVST_READY(SDM bank)	I/O, Input	<p>Dual-purpose (SDM pin) Avalon-ST interface data ready input pin. This pin is used for the Avalon-ST x8 configuration scheme.</p> <p>This pin can also be used as a user I/O pin after configuration.</p> <p>This pin supports the 1.8-V single-ended I/O standard.</p> <p>This pin has a 20-kΩ internal pull-up resistor.</p>	<p>Connect this pin to the ready signal output of the external configuration controller when configuring using the Avalon-ST x8 interface.</p>
AVST_READY(3A bank)	I/O, Input	<p>Dual-purpose Avalon-ST interface data ready input pin. This pin is used for the Avalon-ST x16 and x32 configuration schemes for both MCP and non-MCP parts.</p> <p>This pin supports the SSTL 1.2V I/O standard.</p> <p>This pin has a 10-kΩ internal pull-up resistor.</p>	<p>Connect this pin to the ready signal output of the external configuration controller when configuring using the Avalon-ST x16 or x32 interface.</p>
<i>continued...</i>			





Pin Name	Pin Functions	Pin Description	Connection Guidelines
SDM_MISSION_CLK (3A bank)	I/O, Input	Dual-purpose Avalon-ST interface clock input pin. This pin is used for the Avalon-ST x16 and x32 configuration schemes. This pin can also be used as a user I/O pin after configuration. This pin supports the SSTL 1.2V I/O standard. This pin has a 10-kΩ internal pull-up resistor.	Connect this pin to the clock signal of the external configuration controller when configuring using the Avalon-ST x16 or x32 interface. Connect unused pins as defined in the Intel Quartus Prime software.
SDM_MISSION_DATA_VALID (3A bank)	I/O, Input	Dual-purpose configuration data valid pin. This pin is used for the Avalon-ST x16 and x32 configuration schemes. This pin can also be used as a user I/O pin after configuration. This pin supports the SSTL 1.2V I/O standard. This pin has a 10-kΩ internal pull-up resistor.	Connect this pin to the data valid signal of the external configuration controller when configuring using the Avalon-ST x16 or x32 interface. Connect unused pins as defined in the Intel Quartus Prime software.
AVST_CLK (SDM bank)	I/O, Input	Dual-purpose (SDM pin) Avalon-ST interface clock input pin. This pin is used for the Avalon-ST x16 and x32 configuration schemes. This pin can also be used as a user I/O pin after configuration. This pin support the 1.8-V single-ended I/O standard. When the device is powered, this pin has an internal 20-kΩ pull-up resistor.	Connect this pin to the clock signal of an external configuration controller when configuring using the Avalon-ST x16 or x32 interface.
AVST_VALID (SDM bank)	I/O, Input	Dual-purpose (SDM pin) Avalon-ST interface data valid input pin. This pin can also be used for Avalon-ST x16 and x32 configuration schemes. This pin can also be used as a user I/O pin after configuration. This pin support the 1.8-V single-ended I/O standard. When the device is powered, this pin has an internal 20-kΩ pull-up resistor.	Connect this pin to the data valid signal of an external configuration controller when configuring using the Avalon-ST x16 or x32 interface.
I_PIN_PERST_N_U10_P I_PIN_PERST_N_U20_P	Input	PCI Express* (PCIe*) Platform reset.	Connect these pins using the PCIe Card Electromechanical (CEM) specifications.

### 1.1.4. Differential I/O Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.



**Table 4. Differential I/O Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DIFF_RX[2][A,B,C,D] [1:24][p,n] DIFF_RX[3][A,B,C,D] [1:24][p,n]	I/O, RX channel	These are differential receiver channels on column I/O banks. If these pins are not used as RX differential signals, these pins are available as user I/O pins. Supported I/O standards: <ul style="list-style-type: none"> <li>• 1.5-V I/O standard for differential input</li> <li>• 1.2-V I/O standard for single-ended voltage referenced and non-voltage referenced I/O</li> <li>• 1.2-V I/O standard for differential voltage referenced I/O</li> </ul> These pins have an internal 10-kΩ pull-up resistor.	Connect unused pins as defined in the Intel Quartus Prime software.
DIFF_TX[2][A,B,C,D] [1:24][p,n] DIFF_TX[3][A,B,C,D] [1:24][p,n]	I/O, TX channel	These are differential transmitter channels on column I/O banks. If these pins are not used as TX differential signals, these pins are available as user I/O pins. Supported I/O standards: <ul style="list-style-type: none"> <li>• 1.5-V I/O standard for differential output</li> <li>• 1.2-V I/O standard for single-ended voltage referenced and non-voltage referenced I/O</li> <li>• 1.2-V I/O standard for differential voltage referenced I/O</li> </ul> These pins have an internal 10-kΩ pull-up resistor.	Connect unused pins as defined in the Intel Quartus Prime software.

### 1.1.5. External Memory Interface Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 5. External Memory Interface Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DQS[0:63]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.

*continued...*



Pin Name	Pin Functions	Pin Description	Connection Guidelines
		Supported I/O standards: <ul style="list-style-type: none"> <li>• POD 1.2-V I/O standard</li> <li>• SSTL 1.2-V I/O standard</li> </ul>	
DQSn[0:63]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry. Supported I/O standards: <ul style="list-style-type: none"> <li>• POD 1.2-V I/O standard</li> <li>• SSTL 1.2-V I/O standard</li> </ul>	Connect unused pins as defined in the Intel Quartus Prime software.
DQ[0:63]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, if you plan on migrating to a different memory interface that has a different DQ bus width, you need to reevaluate your pin assignments. Analyze the available DQ pins across all pertinent DQS columns in the device pin-out file. Supported I/O standards: <ul style="list-style-type: none"> <li>• POD 1.2-V I/O standard</li> <li>• SSTL 1.2-V I/O standard</li> </ul>	Connect unused pins as defined in the Intel Quartus Prime software.

### 1.1.6. Voltage Sensor and Voltage Reference Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 6. Voltage Sensor and Voltage Reference Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VREFP_ADC	Input	Dedicated precision analog voltage reference.	Tie these pins to GND for the Intel Agilex™ ES device.
VREFN_ADC	Input		
VSIGP_[0,1]	Input	Analog differential inputs pins used with the voltage sensor inside the FPGA to monitor external analog voltages.	Tie these pins to GND for the Intel Agilex ES device.
VSIGN_[0,1]	Input		



### 1.1.7. Remote Temperature Sensing Diode Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 7. Remote Temperature Sensing Diode Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
TEMPDIODE0[A,C][p,n]	Input	These pins connect to the internal temperature sensing diodes in the FPGA core and corner areas of the FPGA.	Connect this pin to an external temperature sensing device to allow sensing of the FPGA's temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave this pin unconnected.  For more information about the locations and channel numbers of the temperature sensors, refer to the <i>Intel Agilix Sensor Monitoring System</i> chapter in the <i>Intel Agilix Power Management User Guide</i> .
TEMPDIODE[1,4][p,n]	Input	These pins connect to the internal temperature sensing diodes in the E-tile and P-tile transceivers.	Connect this pin to an external temperature sensing device to allow sensing of the E-tile and P-tile temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave this pin unconnected.  For more information about the locations and channel numbers of the temperature sensors, refer to the <i>Intel Agilix Sensor Monitoring System</i> chapter in the <i>Intel Agilix Power Management User Guide</i> .

### 1.1.8. Reference Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.



**Table 8. Reference Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RZQ_[T,B]_2[A,B,C,D] RZQ_[T,B]_3[A,B,C,D]	I/O, bidirectional	Reference pins for I/O banks. The RZQ pins share the same VCCIO_PIO with the I/O bank where they are located. Connect the external precision resistor to the designated pin within the bank. If not required, this pin is a regular I/O pin. These pins support 1.2-V I/O standard. These pins have an internal 10-kΩ pull-up resistor.	When using OCT, tie these pins to GND through a 240-Ω resistor, depending on the desired OCT impedance. When you do not use these pins as dedicated input for the external precision resistor or as I/O pins, leave these pins unconnected.

### 1.1.9. No Connect and DNU Pins

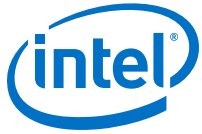
*Note:* Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 9. No Connect and DNU Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, GND, or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration, you have the option to connect these pins to either power, GND, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.

### 1.1.10. Power Supply Pins

*Note:* Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.



**Note:** Intel recommends you to generate a **.pin** file from the Intel Quartus Prime Fitter to verify power pin assignment. Intel also recommends using this **.pin** file to determine if it is safe to power down or ground certain power supplies for your specific design. This step will inform you to make the appropriate design choices for unused power supplies for your design.

**Table 10. Power Supply Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCP	Power	VCCP supplies power to the periphery.	VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. For details about the recommended operating conditions, refer to the <i>Electrical Characteristics</i> section in the <i>Intel Agilex Device Data Sheet</i> . Use the Intel Agilex Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCCP and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board.
VCC	Power	VCC supplies power to the core.	VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. For details about the recommended operating conditions, refer to the <i>Electrical Characteristics</i> section in the <i>Intel Agilex Device Data Sheet</i> . Use the Intel Agilex Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board.
VCCPT	Power	Power supply for the programmable power technology and I/O pre-drivers.	Connect VCCPT to a 1.8V low noise switching regulator. You have the option to source the following from the same regulator as VCCPT: <ul style="list-style-type: none"> <li>VCCA_PLL, VCCPLL_SDM, VCCPLL_HPS, and VCCADC with proper isolation filtering</li> </ul> For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i> . For the power rail sharing, refer to the <i>Power Supply Sharing Guidelines for Intel Agilex Devices</i> .
			<b>continued...</b>



Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCR_CORE	Power	For use in Intel Agilex production devices only (placed here for migration purposes).	For Intel Agilex production devices, tie this pin to a 1.2-V supply. You have the option to source VCCR_CORE from the same regulator as VCCIO_PIO.
VCCH	Power	Analog Interface Bridge (AIB) and digital transceiver power supply.	Connect all VCCH pins to a 0.9V low noise switching power supply. For more details, refer to the <i>Intel Agilex Device Data Sheet</i> .
VCCH_SDM	Power	VCCH voltage rail sense.	Connect this pin to the VCCH voltage rail.
VCCA_PLL	Power	PLL Analog power.	For Intel Agilex ES devices, connect VCCA_PLL to a 1.8V low noise switching regulator. You have the option to source VCCA_PLL from the same regulator as VCCPT with proper isolation filtering. For Intel Agilex ES devices, the VCCA_PLL rail must reside in Group 2 power rails. For Intel Agilex production devices, connect VCCA_PLL to a 1.2V low noise switching regulator. You have the option to source VCCA_PLL from the same regulator as VCCIO_PIO with proper isolation filtering. For Intel Agilex production devices, the VCCA_PLL rail must reside in Group 3 power rails.
VCCIO_PIO[2][A,B,C,D] VCCIO_PIO[3][A,B,C,D]	Power	These are the supply voltage pins for the I/O banks. Each bank can support a different voltage level. Supported VCCIO standards include the following: <ul style="list-style-type: none"> <li>• 1.2-V LVCMOS</li> <li>• SSTL12/Diff SSTL12</li> <li>• HSTL12/ Diff HSTL12</li> <li>• HSUL12/ Diff HSUL12</li> <li>• POD12/ Diff POD12</li> <li>• 1.5-V True Differential Signaling</li> </ul>	Connect these pins to a 1.2-V or 1.5-V supplies, depending on the I/O standard required by the specific bank. You have the option to power down unused I/O banks by connecting their VCCIO_PIO pin to GND. During the power-up sequence only, a transient current whose magnitude is less than the VCCIO_PIO operating static current may be observed as the VCCIO_PIO transistors become operational. This is the expected behavior and will neither cause any functional failure nor reliability concerns to the device if the power-up or power-down sequence is followed. For more details, refer to the <i>Intel Agilex Sensor Monitoring System</i> chapter in the <i>Intel Agilex Power Management User Guide</i> . For the power rail sharing, refer to the <i>Power Supply Sharing Guidelines for Intel Agilex Devices</i> .
VCCIO_PIO_SDM	Power	VCCIO_PIO voltage rail sense line.	Connect these pins to bank VCCIO_PIO 3A.

**continued...**



Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCIO_SDM	Power	Configuration pins power supply.	Connect these pins to a 1.8-V power supply. When dual-purpose configuration pins are used for configuration, tie VCCIO_PIO of the bank where the dual-purpose configuration pins reside to the same regulator as VCCIO_SDM. For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i> . For the power rail sharing, refer to the <i>Power Supply Sharing Guidelines for Intel Agilex Devices</i> .
VCCPLLDIG_SDM	Power	SDM block PLL power pins.	VCCPLLDIG_SDM must be sourced from the same regulator as VCCL_SDM with proper isolation filtering.
VCCL_SDM	Power	SDM power supply.	Connect these pins to a 0.8-V power supply.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	When using the design security volatile key, connect this pin to a non-volatile battery power source in the range of 1.0V – 1.8V. When not using the volatile key, tie this pin to the 1.8-V VCCPT. This pin must be properly powered as per the recommended voltage range as the power-on reset (POR) circuitry of the Intel Agilex devices monitors VCCBAT. Provide a minimum decoupling of 47nF for the VCCBAT power rail near the VCCBAT pin. For the power rail sharing, refer to the <i>Power Supply Sharing Guidelines for Intel Agilex Devices</i> .
VCCPLL_SDM	Power	VCCPLL_SDM supplies analog power to the SDM block PLLs.	With proper isolation filtering, you have the option to source VCCPLL_SDM from the same regulator as VCCPT. Decoupling for these pins depends on the design decoupling requirements of the specific board.
GND	Ground	Device ground pins.	Connect all GND pins to the board ground plane.
VREFB [ 2 ] [ AN0 , BN0 , CN0 , DN0 ] VREFB [ 3 ] [ AN0 , BN0 , CN0 , DN0 ]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then use these pins as voltage-reference pins for the bank.	If VREF pins are not used, connect them to GND.
VCCLSENSE	Output	Differential sense line to external regulator.	VCCLSENSE and GNDSENSE are differential remote sense pins for the VCC power. Connect your regulators' differential remote sense lines to the respective VCCLSENSE and
GNDSENSE			

**continued...**





Pin Name	Pin Functions	Pin Description	Connection Guidelines
			GNDSENSE pins. This compensates for the DC IR drop associated with the PCB and device package from the VCC power. Route these connections as differential pair traces and keep them isolated from any other noise source. You must connect the VCCLSENSE and GNDSENSE lines to the regulator's remote sense inputs.
VCCADC	Power	ADC power pin for the voltage sensors.	You must supply a low noise 1.8-V power supply to this pin if you are using the internal voltage sensors of the Intel Agilex device. When you are using the voltage sensors, tie this pin to VCCPT with proper isolation filtering. Tie this pin to VCCA_PLL.
VCCFUSEWR_SDM	Power	The required power supply to program (write) the optional, one-time programmable eFuses. These eFuses are an integral part of the Intel Agilex security architecture. For more information, refer to the <i>Intel Agilex Configuration User Guide</i> .	This voltage rail can be set anywhere between 1.4V and 2.4V.

### 1.1.11. Secure Device Manager (SDM) Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 11. SDM Pins—Preliminary**

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
RREF_SDM	Reference resistor input for the PLLs of the SDM interface.	—	Input	Connect a 2kΩ +/-1% resistor to GND.
SDM_IO0	This pin is pulled low internally by a 20-kΩ resistor when the device is powered up.	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.

*continued...*



Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
SDM_IO1	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA2	Connect this pin to the data2 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_DATA1	Connect this pin to the data1 pin of the QSPI flash device when configuring from the QSPI flash device.
		3'b100	SDMMC_CFG_DATA1	Connect this pin to the data1 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO2	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA0	Connect this pin to the data0 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_CLK	Connect this pin to the clock input of the QSPI flash device when configuring from the QSPI flash device.
		3'b100	SDMMC_CFG_DATA0	Connect this pin to the data0 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO3	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA3	Connect this pin to the data3 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_DATA2	Connect this pin to the data2 pin of the QSPI flash device when configuring from the QSPI flash device.

*continued...*



Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
		3'b100	SDMMC_CFG_DATA2	Connect this pin to the data2 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO4	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA1	Connect this pin to the data1 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_DATA0	Connect this pin to the data0 pin of the QSPI flash device when configuring from the QSPI flash device.
		3'b100	SDMMC_CFG_CMD	Connect this pin to the command input of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO5	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin will function as MSEL[0] during power up and reset to determine the configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected. For more information, refer to the <i>Intel Agilex Configuration User Guide</i> .	—	MSEL[0]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCS00	Connect this pin to the nCS input of the first QSPI flash device when configuring from QSPI flash devices.
		3'b100	SDMMC_CFG_CCLK	Connect this pin to the clock input of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.

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Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
SDM_IO6	<p>This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.</p> <p>This pin functions differently depending on the configuration scheme used by setting the MSEL pins.</p>	3'b110	AVSTx8_DATA4	Connect this pin to the data4 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_DATA3	Connect this pin to the data3 pin of the QSPI flash device when configuring from the QSPI flash device.
		3'b100	SDMMC_CFG_DATA3	Connect this pin to the data3 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO7	<p>This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.</p> <p>This pin will function as MSEL[1] during power up to determine the configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected.</p> <p>For more information, refer to the <i>Intel Agilex Configuration User Guide</i>.</p>	—	MSEL[1]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCS02	Connect this pin to the nCS input of the third QSPI flash device when you use cascaded QSPI flash devices for HPS application.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO8	<p>This pin is pulled low internally by a 20-kΩ resistor when the device is powered up.</p> <p>This pin functions differently depending on the configuration scheme used by setting the MSEL pins.</p>	3'b110	AVSTx8_READY	Connect this pin to the ready signal output of the external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_nCS03	Connect this pin to the nCS input of the fourth QSPI flash device when you use cascaded QSPI flash devices for HPS application. Connect with a 1-kΩ pull-up resistor to VCCIO_SDM.

**continued...**



Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
		3'b100	SDMMC_CFG_DATA4	Connect this pin to the data4 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO9	<p>This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.</p> <p>This pin will function as MSEL[2] during power up to determine the configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected.</p> <p>For more information, refer to the <i>Intel Agilex Configuration User Guide</i>.</p>	—	MSEL[2]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCS01	Connect this pin to the nCS input of the second QSPI flash device when you use cascaded QSPI flash devices for HPS application.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO10	<p>This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.</p> <p>This pin functions differently depending on the configuration scheme used by setting the MSEL pins.</p>	3'b110	AVSTx8_DATA7	Connect this pin to the data7 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b100	SDMMC_CFG_DATA7	Connect this pin to the data7 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO11	<p>This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.</p> <p>This pin functions differently depending on the configuration scheme used by setting the MSEL pins.</p>	3'b110	AVSTx8_VALID	Connect this pin to the data valid pin of an external configuration controller when configuring using the Avalon-ST x8 interface.

*continued...*



Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO12	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.	—	Any MSEL setting	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO13	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA5	Connect this pin to the data5 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b100	SDMMC_CFG_DATA5	Connect this pin to the data5 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO14	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_CLK	Connect this pin to the clock output of an external configuration controller when configuring using the Avalon-ST x8 interface.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO15	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA6	Connect this pin to the data6 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.

*continued...*



Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
		3'b100	SDMMC_CFG_DATA6	Connect this pin to the data6 pin of the SD/MMC card flash device when configuring from the SD/MMC flash.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.
SDM_IO16	This pin is pulled low internally by a 20-kΩ resistor when the device is powered up.	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the <a href="#">Secure Device Manager (SDM) Optional Signal Pins</a> on page 23.

### 1.1.12. Secure Device Manager (SDM) Optional Signal Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 12. SDM Optional Signal Pins—Preliminary**

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
PWRMGT_SCL	PMBus Power Management Clock. This pin is used as the clock pin for the PMBus interface.	This pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. Connect this pin to the PMBus clock pin of your regulator. When a -V device is used, you must enable the SmartVID connection between the device	SDM_IO0 SDM_IO14	SDM_IO0	SDM_IO0 SDM_IO14	SDM_IO0 SDM_IO14

*continued...*



Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
		and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the external master controller for the PMBus slave mode.				
PWRMGT_SDA	PMBus Power Management Serial Data. This pin is used as the data pin for the PMBus interface.	This pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. Connect this pin to the PMBus data pin of your regulator. When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the external master controller for the PMBus slave mode.	SDM_IO11 SDM_IO12 SDM_IO16	SDM_IO12 SDM_IO16	SDM_IO11 SDM_IO12 SDM_IO16	SDM_IO11 SDM_IO12 SDM_IO16
PWRMGT_ALERT	PMBus Power Management Alert.	This pin requires a pull-up resistor to the 1.8V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ	SDM_IO0 SDM_IO12	SDM_IO0 SDM_IO9 SDM_IO12	SDM_IO0 SDM_IO9 SDM_IO12	SDM_IO0 SDM_IO12

*continued...*





Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
	This pin is used as the ALERT function for the PMBus interface when the Intel Agilex -V device is the PMBus slave.	<p>depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. Connect this pin to the PMBus ALERT pin of the external master controller.</p> <p>When using the SmartVID feature with the Intel Agilex -V device as a PMBus slave, you must connect the PWRMGT_ALERT signal along with the PWRMGT_SCL and PWRMGT_SDA signals to the PMBus master device to complete the SmartVID power management interface. The PMBus master device reads the VID codes from the Intel Agilex slave and programs the voltage regulator to output the correct VID voltage.</p>				
CONF_DONE	The CONF_DONE pin indicates all configuration data has been received.	<p>By default, Intel recommends using the SDM_IO16 pin to implement the CONF_DONE function.</p> <p>If SDM_IO16 is unavailable, the CONF_DONE function can also be implemented using any unused SDM_IO pins.</p> <p>Except for SDM_IO0 and SDM_IO16, other SDM_IO pins are required to connect to an external 4.7-kΩ pull-down resistor for the CONF_DONE signal.</p> <p>Connect the CONF_DONE pin to the external configuration controller when configuring using the Avalon-ST (AVST) interface.</p>	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO6 SDM_IO7 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16

*continued...*



Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
		You have an option to monitor this signal with an external component if you are using the active serial (AS) x4 configuration scheme.				
INIT_DONE	<p>The INIT_DONE pin indicates the device has enter user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Intel Quartus Prime software.</p> <p>When the INIT_DONE function is enabled, this pin will drive high when configuration is completed and the device goes into user mode.</p>	<p>Intel recommends you to use SDM_IO0 or SDM_IO16 to implement the INIT_DONE function when available as it has an internal weak pull-down for the correct function of INIT_DONE during power up.</p> <p>If SDM_IO0 and SDM_IO16 are unavailable, SDM_IO5 can also be used for the INIT_DONE function when the configuration mode is set to Avalon-ST x8 or Avalon-ST x32 (AVST x8 or AVST x32) as these modes require an external 4.7-kΩ pull-down resistor.</p> <p>If SDM_IO0, SDM_IO5, and SDM_IO16 are unavailable, the INIT_DONE function can also be implemented using any unused SDM_IO pins provided that an external 4.7-kΩ pull-down resistor is provided for the INIT_DONE signal.</p>	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO6 SDM_IO7 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16
CvP_CONFDONE	<p>The CvP_CONFDONE pin indicates the device has received the complete bitstream during configuration via protocol (CvP) core image configuration.</p> <p>When used for this purpose, enable this pin using the Intel Quartus Prime software.</p>	<p>Connect this output pin to an external logic device that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.</p>	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	—	—

*continued...*



Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
SEU_ERROR	<p>The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.</p> <p>The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software.</p>	Connect this output pin to an external logic device that monitors the SEU event.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16
HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad serial peripheral interface (quad SPI) devices.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16
Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose	Connect this input pin to an external logic device that manages the remote system upgrade of the device. By	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3



Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
	between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.	default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.	SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO12 SDM_IO16	SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16

## 1.2. Intel Agilex E-Tile Pins

### 1.2.1. E-Tile Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 13. E-Tile Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCH_GXE (L1 ,R1 )	Power	Analog power, block level transmitter buffers for E-tile, specific to the left (L) side or right (R) side of the device.	Connect VCCH_GXE to a 1.1V low noise switching regulator. VCCH_GXE must be powered up even when the E-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i> .
VCCRT_GXE (L1 ,R1 )	Power	Analog power, used for the high-speed circuitry for the E-tile, specific to the left (L) side or right (R) side of the device.	VCCRT_GXE can be connected to a 0.9V low noise switching regulator.

*continued...*



Pin Name	Pin Functions	Pin Description	Connection Guidelines
			<p>You must connect VCCRT_GXE to VCCH through an LC filter. For more information about the LC filter design, refer to the <i>Intel Agilex Power Management User Guide</i>.</p> <p>VCCRT_GXE must be powered up even when the E-tile transceivers are not used.</p> <p>For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i>.</p>
VCCRTPLL_GXE(L1,R1)	Power	Analog power, used for the high-speed circuitry for the E-tile, specific to the left (L) side or right (R) side of the device.	<p>You must source the VCCRTPLL_GXE from the VCCH with proper isolation filtering.</p> <p>Filtering may be optional if this voltage rail can meet the noise mask requirement. For more information about the noise mask requirements, refer to the <i>Intel Agilex Power Management User Guide</i>.</p> <p>VCCRTPLL_GXE must be powered up even when the E-tile transceivers are not used.</p> <p>For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i>.</p>
VCCCLK_GXE(L1,R1)	Power	I/O power, specific to the E-tile reference clock buffers.	<p>Connect VCCCLK_GXE to a 2.5V low noise switching regulator.</p> <p>VCCCLK_GXE must be powered up even when the E-tile transceivers are not used.</p> <p>For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i>.</p>
VCC_HSSI_GXE(L1,R1)	Power	Primary digital supply for all digital signals, specific to E-tile.	<p>Connect VCC_HSSI_GXE to a 0.9V low noise switching regulator. This voltage rail must be shared with VCCH using proper isolation filtering.</p> <p>VCC_HSSI_GXE must be powered up even when the E-tile transceivers are not used.</p>
GXE(L8,R9)_RX_CH[0:23] [p,n]	Input	<p>High speed differential serial inputs to receiver circuitry. Specific to the E-tile transceiver on the left (L) side or right (R) side of the device.</p> <p>Supported I/O standard:</p> <ul style="list-style-type: none"> <li>• CML -56G PAM4</li> <li>• 30G NRZ</li> </ul>	<p>No off-chip AC-coupling capacitor is required if the RX input common mode is between VCCRT_GXE and GND, and the RX input amplitude difference is &lt;1200mVp-p. The absolute maximum input to E-Tile SerDes is VCCRT_GXE + 300mV to prevent forward biasing of the ESD diodes.</p>

**continued...**



Pin Name	Pin Functions	Pin Description	Connection Guidelines
			When using external AC-coupling capacitors, the RX termination is to the VCCH_GXE supply. For more information about the external AC-coupling, refer to the <i>Intel Agilex E-Tile Transceiver PHY User Guide</i> . Leave unused pins floating.
GXE(L8,R9)_TX_CH[0:23] [p,n]	Output	High speed differential serial outputs from the transmitter circuitry. Specific to the E-tile transceiver on the left (L) side or right (R) side of the device. Supported I/O standard: <ul style="list-style-type: none"> <li>• CML -56G PAM4</li> <li>• 30G NRZ</li> </ul>	Leave all unused pins floating.
REFCLK_GXE(L8,R9)_CH[0:8] :8][p,n]	Input	High speed differential reference clock receiver channels, specific to each E-tile transceiver of the left (L) side or right (R) side of the device. REFCLK_GXE can be supplied to both RX and TX independently. REFCLK_GXE can be used as dedicated clock input pins for core clock generation even when the transceiver channel is not available. Supported I/O standard: <ul style="list-style-type: none"> <li>• LVPECL</li> </ul>	No off-chip AC-coupling capacitor is required. The default internal REFCLK inputs are 2.5V LVPECL with a 50Ω termination. Optional external termination is 2.5V LVPECL or 3.3V LVPECL. For more information about the external AC-coupling, refer to the <i>Intel Agilex E-Tile Transceiver PHY User Guide</i> . When implementing Dynamic Reconfiguration clock pin, REFCLK_GXE_CH1p/n must be bonded out. For more details, refer to the <i>Intel Agilex E-Tile Transceiver PHY User Guide</i> . Tie each unused REFCLK pin to GND through a 1kΩ resistor.
IO_AUX_RREF(10,20)	Input	Precision reference resistor for the AIB auxiliary channel.	Connect to a 2kΩ resistor (±1%) to GND.

### 1.3. Intel Agilex P-Tile Pins

#### 1.3.1. P-Tile Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.



**Table 14. P-Tile Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCH_GXP[L1,R1]	Power	Secondary high-voltage analog supply for transceivers, and on-die PLL specific to P-tile.	Connect VCCH_GXP to a 1.8V low noise switching regulator. This voltage rail can be shared with VCCPT using proper isolation filtering.  To minimize regulator switching noise impact on channel jitter performance, keep the regulator switching frequency below 1MHz.  VCCH_GXP must be powered up even when the P-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i> .
VCCRT_GXP[L1,R1]	Power	Primary analog supply for the TX and RX channels, specific to P-tile.	Connect VCCRT_GXP to a 0.9V low noise switching regulator. This voltage rail can be shared with VCCH using proper isolation filtering.  VCCRT_GXP must be powered up even when the P-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i> .
VCCCLK_GXP[L1,R1]	Power	LVC MOS I/O buffer supply rail, specific to P-tile.	Connect VCCCLK_GXP to a 1.8V low noise switching regulator. This voltage rail can be shared with VCCPT using proper isolation filtering.  VCCCLK_GXP must be powered up even when the P-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i> .
VCCFUSE_GXP	Power	Required power supply for the firmware to read internal settings for the one-time programmable eFuses.	Connect this voltage rail to a 0.9V power supply. This rail must be shared with VCC_HSSI_GXP.  VCCFUSE_GXP must be powered up even when the P-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the <i>Intel Agilex Platform Design Guide</i> .
VCC_HSSI_GXP(L1,R1)	Power	Primary digital supply for all digital signals, specific to P-tile.	Connect VCC_HSSI_GXP to a 0.9V low noise switching regulator. This voltage rail must be shared with VCCH.  VCC_HSSI_GXP must be powered up even when the P-tile transceivers are not used.
GXP[L10A,R11A]_RX_CH[19:0][p,n]	Input	PCIe Gen4-based receiver pins, specific to the P-tile transceivers on the left (L) side or right (R) side of the device.	When these pins are not used, they can be floating.

**continued...**



Pin Name	Pin Functions	Pin Description	Connection Guidelines
		For PCIe Gen4 mode, use the lower 16 bits [15:0]. These pins also support NRZ encoding up to 16Gbps.	
GXP[L10A,R11A]_TX_CH[19:0][p,n]	Output	PCIe Gen4-based transmitter pins, specific to the P-tile transceivers on the left (L) side or right (R) side of the device. For PCIe Gen4 mode, use the lower 16 bits [15:0]. These pins also support NRZ encoding up to 16Gbps.	Transmitter pins must be AC coupled. The capacitor value ranges from 176nF to 256nF per PCIe Gen4 specification. When these pins are not used, they can be floating.
REFCLK_GXP[L10A,R11A]_CH[0,2][p,n]	Input	Standard PCIe HCSL reference clock input pins, specific to the P-tile transceivers on the left (L) side or right (R) side of the device.	For HCSL I/O standard, it only supports DC coupling. In the PCIe configuration, DC coupling is allowed on the REFCLK if the selected REFCLK I/O standard is the HCSL I/O standard. You must connect a 100MHz reference clock to both reference clock inputs for x16 and 4x4 modes. These reference clocks must be derived from the same clock source. A fan-out buffer can be used but must meet a $\pm 300$ ppm requirement. For 2x8 modes, you can connect both reference clock inputs to the same clock source or connect to two independent clock sources. If the P-tile is completely unused but still has power applied, tie both REFCLK inputs to GND.
IO_AUX_RREF[10,20]_P	Input	Reference resistor for the Embedded Multi-Die-Interconnect Bridge (EMIB) of the P-tile transceivers.	Connect each IO_AUX_RREF to a 2k $\Omega$ resistor ( $\pm 1\%$ ) to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed such that it avoids any aggressor signals.
U[10,20]_P_IO_RESREF_0	Input	Transceiver reference resistor connection for PMA circuitry to provide termination for calibration.	Connect each pin to a 200 $\Omega$ 1% (100 ppm/ $^{\circ}$ C) precision resistor this pin and GND. Place this resistor very close to the IO_RESREF pin. Avoid routing any noisy signals next to this reference resistor or its traces. Tie resistor to GND plane through a via placed very close to the reference resistor. External reference resistor parasitic capacitance load must be less than 14pF. Maximum parasitic capacitance includes external loading of PHY count, package trace, and PCB trace. Each PHY connected to the IO_RESREF pin adds an additional 1.5pF of loading.
I_PIN_PERST_N_U[10,20]_P	Input	PCI Express (PCIe) Platform reset pin.	In a PCI Express (PCIe) adapter card implementation, connect the PCIe nPERST signal from the PCIe edge connector to each P-tile transceiver bank I_PIN_PERST_N input.





Pin Name	Pin Functions	Pin Description	Connection Guidelines
			<p>Use a level translator to fan out and change the 3.3V open-drain nPERST signal from the PCIe connector to the 1.8V I_PIN_PERST_N input of each P-tile transceiver that is used on the board.</p> <p>Provide a 1.8V pull-up resistor to the I_PIN_PERST_N input as the nPERST signal from the PCIe connector is an open-drain signal. You must pull up the 3.3V PCIe nPERST signal on the adapter card.</p> <p>For non-PCIe systems, connect the system's master reset signal to the I_PIN_PERST_N input pin. If the master reset is not 1.8V, use a level shifter to meet the 1.8V I_PIN_PERST_N input requirement. For open-drain master reset driving the I_PIN_PRST_N input, provide a 1.8V pull-up resistor. Ensure all power to the device as well as the PCIe clock is stable prior to releasing the reset to the I_PIN_PRST_N pin.</p> <p>This input pin does not have an internal pull-up resistor, you need to add an external 5kΩ – 10kΩ pull-up resistor if the voltage translator does not provide an active driver.</p> <p>If the tile is unused, tie to GND.</p>

## 1.4. Intel Agilex Hard Processor System (HPS) Pins

### 1.4.1. HPS Supply Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 15. HPS Supply Pins—Preliminary**

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCL_HPS	Power	VCCL_HPS supplies power to the HPS core.	The VCCL_HPS power supply voltage could vary from 0.685V to 0.85V with VID or 0.9V non-VID supply (voltage boost).

*continued...*



Pin Name	Pin Functions	Pin Description	Connection Guidelines
			VCCL_HPS can be shared with VCC if they are at the same VID voltage level.
VCCIO_HPS	Power	The HPS dedicated I/Os support 1.8V voltage level.	Connect these pins to 1.8V power supply. You have the option to source VCCIO_HPS pins from the same regulator as VCCIO_SDM.
VCCPLL_HPS	Power	VCCPLL_HPS supplies analog power to the HPS PLLs.	Connect these pins to a 1.8V. You have the option to share VCCPLL_HPS with the same regulator as VCCIO_SDM.
VCCPLLDIG_HPS	Power	Digital power supply of the PLL in HPS.	Connect this to the VCCL_HPS with proper isolation filtering.

### 1.4.2. HPS Oscillator Clock Input Pin

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 16. HPS Oscillator Clock Input Pin—Preliminary**

You must provide one input clock source to the HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
HPS_OSC_CLK	Clock input pin that drives the main PLL. Connect a single-ended clock source to this pin. The I/O standard of the clock source must be compatible with VCCIO_HPS.	Input	Select one of the 48 HPS dedicated I/O.

### 1.4.3. HPS JTAG Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.



**Table 17. HPS JTAG Pins—Preliminary**

You have the option to connect HPS JTAG pins to the HPS Dedicated I/O using the following assignments.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
JTAG_TCK	HPS JTAG test clock input pin. Connect this pin through a 1-kΩ – 10-kΩ pull-down resistor to GND. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_9
JTAG_TMS	HPS JTAG test mode select input pin. Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_HPS supply. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_10
JTAG_TDO	HPS JTAG test data output pin. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Output	HPS_IOB_11
JTAG_TDI	HPS JTAG test data input pin. Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_HPS supply. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_12

#### 1.4.4. HPS GPIO Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.



**Table 18. HPS GPIO Pins—Preliminary**

There are two GPIO controllers (GPIO0 and GPIO1) for the Intel Agilex HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
GPIO0_IO[0..23]	General purpose input output. Ensure that the I/O standard used is compatible with VCCIO_HPS.	I/O	HPS_IOA_[1..24] HPS_IOB_[1..24]
GPIO1_IO[0..23]			

### 1.4.5. HPS SDMMC Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 19. HPS SDMMC Pins—Preliminary**

Intel recommends adding a 1-kΩ to 10-kΩ pull-up resistor to every SDMMC data signal that is used.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
SDMMC_CCLK	SDMMC clock out	Output	HPS_IOA_1	HPS_IOB_15
SDMMC_CMD	SDMMC command line. Pull this pin high on the board with a weak pull-up resistor. For example, a 10-kΩ to VCCIO_HPS.	I/O	HPS_IOA_2	HPS_IOB_14
SDMMC_DATA0	SDMMC Data 0	I/O	HPS_IOA_3	HPS_IOB_13
SDMMC_DATA1	SDMMC Data 1	I/O	HPS_IOA_4	HPS_IOB_16
SDMMC_DATA2	SDMMC Data 2	I/O	HPS_IOA_5	HPS_IOB_17
SDMMC_DATA3	SDMMC Data 3 When using SD card, there is an existing 50-kΩ pull-up on SDMMC Data Bit 3 which can be disabled in the HPS software by using the	I/O	HPS_IOA_6	HPS_IOB_18

*continued...*



HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
	SET_CLR_CARD_DETECT (ACMD42) command. This is not applicable to the eMMC flash.			
SDMMC_DATA4	SDMMC Data 4	I/O	HPS_IOA_7	HPS_IOB_19
SDMMC_DATA5	SDMMC Data 5	I/O	HPS_IOA_8	HPS_IOB_20
SDMMC_DATA6	SDMMC Data 6	I/O	HPS_IOA_9	HPS_IOB_21
SDMMC_DATA7	SDMMC Data 7	I/O	HPS_IOA_10	HPS_IOB_22
SDMMC_PWR_EN	SDMMC Power Enable	Output	HPS_IOA_11	HPS_IOB_23

### 1.4.6. HPS NAND Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 20. HPS NAND Pins—Preliminary**

HPS Pin Functions	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
NAND_ADQ0	NAND Data Bit 0	I/O	HPS_IOA_1	HPS_IOB_1
NAND_ADQ1	NAND Data Bit 1	I/O	HPS_IOA_2	HPS_IOB_2
NAND_WE_N	NAND Write Enable. This is an active-low signal.	Output	HPS_IOA_3	HPS_IOB_3
NAND_RE_N	NAND Read Enable. This is an active-low signal.	Output	HPS_IOA_4	HPS_IOB_4
NAND_WP_N	NAND Write Protect	Output	HPS_IOA_5	HPS_IOB_5
NAND_ADQ2	NAND Data Bit 2	I/O	HPS_IOA_6	HPS_IOB_6

*continued...*



HPS Pin Functions	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
NAND_ADQ3	NAND Data Bit 3	I/O	HPS_IOA_7	HPS_IOB_7
NAND_CLE	NAND Command Latch Enable	Output	HPS_IOA_8	HPS_IOB_8
NAND_ADQ4	NAND Data Bit 4	I/O	HPS_IOA_9	HPS_IOB_9
NAND_ADQ5	NAND Data Bit 5	I/O	HPS_IOA_10	HPS_IOB_10
NAND_ADQ6	NAND Data Bit 6	I/O	HPS_IOA_11	HPS_IOB_11
NAND_ADQ7	NAND Data Bit 7	I/O	HPS_IOA_12	HPS_IOB_12
NAND_ALE	NAND Address Latch Enable	Output	HPS_IOA_13	HPS_IOB_13
NAND_RB	NAND Ready/Busy. Connect this pin through a 1-kΩ to 10-kΩ pull-up resistor to VCCIO_HPS.	Input	HPS_IOA_14	HPS_IOB_14
NAND_CE_N	NAND Chip Enable. This is an active-low signal.	Output	HPS_IOA_15	HPS_IOB_15
NAND_ADQ8	NAND Data Bit 8	I/O	HPS_IOA_17	HPS_IOB_17
NAND_ADQ9	NAND Data Bit 9	I/O	HPS_IOA_18	HPS_IOB_18
NAND_ADQ10	NAND Data Bit 10	I/O	HPS_IOA_19	HPS_IOB_19
NAND_ADQ11	NAND Data Bit 11	I/O	HPS_IOA_20	HPS_IOB_20
NAND_ADQ12	NAND Data Bit 12	I/O	HPS_IOA_21	HPS_IOB_21
NAND_ADQ13	NAND Data Bit 13	I/O	HPS_IOA_22	HPS_IOB_22
NAND_ADQ14	NAND Data Bit 14	I/O	HPS_IOA_23	HPS_IOB_23
NAND_ADQ15	NAND Data Bit 15	I/O	HPS_IOA_24	HPS_IOB_24



### 1.4.7. HPS USB Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 21. HPS USB Pins—Preliminary**

There are two USB controllers (USB0 and USB1) for the Intel Agilex HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
USB0_CLK	USB0 Clock	Input	HPS_IOA_1
USB0_STP	USB0 Stop Data	Output	HPS_IOA_2
USB0_DIR	USB0 Direction	Input	HPS_IOA_3
USB0_DATA0	USB0 Data Bit 0	I/O	HPS_IOA_4
USB0_DATA1	USB0 Data Bit 1	I/O	HPS_IOA_5
USB0_NXT	USB0 Next Data	Input	HPS_IOA_6
USB0_DATA2	USB0 Data Bit 2	I/O	HPS_IOA_7
USB0_DATA3	USB0 Data Bit 3	I/O	HPS_IOA_8
USB0_DATA4	USB0 Data Bit 4	I/O	HPS_IOA_9
USB0_DATA5	USB0 Data Bit 5	I/O	HPS_IOA_10
USB0_DATA6	USB0 Data Bit 6	I/O	HPS_IOA_11
USB0_DATA7	USB0 Data Bit 7	I/O	HPS_IOA_12
USB1_CLK	USB1 Clock	Input	HPS_IOA_13
USB1_STP	USB1 Stop Data	Output	HPS_IOA_14
USB1_DIR	USB1 Direction	Input	HPS_IOA_15
USB1_DATA0	USB1 Data Bit 0	I/O	HPS_IOA_16
USB1_DATA1	USB1 Data Bit 1	I/O	HPS_IOA_17

*continued...*



HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
USB1_NXT	USB1 Next Data	Input	HPS_IOA_18
USB1_DATA2	USB1 Data Bit 2	I/O	HPS_IOA_19
USB1_DATA3	USB1 Data Bit 3	I/O	HPS_IOA_20
USB1_DATA4	USB1 Data Bit 4	I/O	HPS_IOA_21
USB1_DATA5	USB1 Data Bit 5	I/O	HPS_IOA_22
USB1_DATA6	USB1 Data Bit 6	I/O	HPS_IOA_23
USB1_DATA7	USB1 Data Bit 7	I/O	HPS_IOA_24

### 1.4.8. HPS EMAC Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 22. HPS EMAC Pins—Preliminary**

There are three EMAC controllers (EMAC0, EMAC1, and EMAC2) for the Intel Agilex HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC0_TX_CLK	EMAC0 Transmit Clock	Output	HPS_IOA_13
EMAC0_TX_CTL	EMAC0 Transmit Control	Output	HPS_IOA_14
EMAC0_RX_CLK	EMAC0 Receive Clock	Input	HPS_IOA_15
EMAC0_RX_CTL	EMAC0 Receive Control	Input	HPS_IOA_16
EMAC0_TXD0	EMAC0 Transmit Data Bit 0	Output	HPS_IOA_17
EMAC0_TXD1	EMAC0 Transmit Data Bit 1	Output	HPS_IOA_18
EMAC0_RXD0	EMAC0 Receive Data Bit 0	Input	HPS_IOA_19

*continued...*





HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC0_RXD1	EMAC0 Receive Data Bit 1	Input	HPS_IOA_20
EMAC0_TXD2	EMAC0 Transmit Data Bit 2	Output	HPS_IOA_21
EMAC0_TXD3	EMAC0 Transmit Data Bit 3	Output	HPS_IOA_22
EMAC0_RXD2	EMAC0 Receive Data Bit 2	Input	HPS_IOA_23
EMAC0_RXD3	EMAC0 Receive Data Bit 3	Input	HPS_IOA_24
EMAC1_TX_CLK	EMAC1 Transmit Clock	Output	HPS_IOB_1
EMAC1_TX_CTL	EMAC1 Transmit Control	Output	HPS_IOB_2
EMAC1_RX_CLK	EMAC1 Receive Clock	Input	HPS_IOB_3
EMAC1_RX_CTL	EMAC1 Receive Control.	Input	HPS_IOB_4
EMAC1_TXD0	EMAC1 Transmit Data Bit 0	Output	HPS_IOB_5
EMAC1_TXD1	EMAC1 Transmit Data Bit 1	Output	HPS_IOB_6
EMAC1_RXD0	EMAC1 Receive Data Bit 0	Input	HPS_IOB_7
EMAC1_RXD1	EMAC1 Receive Data Bit 1	Input	HPS_IOB_8
EMAC1_TXD2	EMAC1 Transmit Data Bit 2	Output	HPS_IOB_9
EMAC1_TXD3	EMAC1 Transmit Data Bit 3	Output	HPS_IOB_10
EMAC1_RXD2	EMAC1 Receive Data Bit 2	Input	HPS_IOB_11
EMAC1_RXD3	EMAC1 Receive Data Bit 3	Input	HPS_IOB_12
EMAC2_TX_CLK	EMAC2 Transmit Clock	Output	HPS_IOB_13
EMAC2_TX_CTL	EMAC2 Transmit Control	Output	HPS_IOB_14
EMAC2_RX_CLK	EMAC2 Receive Clock	Input	HPS_IOB_15
EMAC2_RX_CTL	EMAC2 Receive Control	Input	HPS_IOB_16
EMAC2_TXD0	EMAC2 Transmit Data Bit 0	Output	HPS_IOB_17
EMAC2_TXD1	EMAC2 Transmit Data Bit 1	Output	HPS_IOB_18
			<i>continued...</i>



HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC2_RXD0	EMAC2 Receive Data Bit 0	Input	HPS_IOB_19
EMAC2_RXD1	EMAC2 Receive Data Bit 1	Input	HPS_IOB_20
EMAC2_TXD2	EMAC2 Transmit Data Bit 2	Output	HPS_IOB_21
EMAC2_TXD3	EMAC2 Transmit Data Bit 3	Output	HPS_IOB_22
EMAC2_RXD2	EMAC2 Receive Data Bit 2	Input	HPS_IOB_23
EMAC2_RXD3	EMAC2 Receive Data Bit 3	Input	HPS_IOB_24

### 1.4.9. HPS I2C\_EMAC and MDIO Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

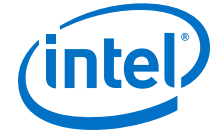
There are three sets of I2C\_EMAC interfaces that can be used as I2C interfaces or as the MDIO pins for the EMACs. Please take note that the I2C\_EMAC and MDIO modules must be used with the corresponding EMAC interfaces. For example, you can use either I2C\_EMAC0\_SDA and I2C\_EMAC0\_SCL or MDIO0\_MDIO and MDIO0\_MDC with EMAC0.

The I2C protocol requires pull-up resistors to VCCIO\_HPS on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7-kΩ or lower.

Typically the MDIO pin requires an external pull-up resistor to VCCIO\_HPS in the range of 1.0-kΩ to 4.7-kΩ.

**Table 23. HPS I2C\_EMAC and MDIO Pins—Preliminary**

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
I2C_EMAC2_SDA	I2C EMAC2 Serial Data	I/O	HPS_IOA_7	HPS_IOB_9	HPS_IOB_21
I2C_EMAC2_SCL	I2C EMAC2 Serial Clock	I/O	HPS_IOA_8	HPS_IOB_10	HPS_IOB_22
I2C_EMAC1_SDA	I2C EMAC1 Serial Data	I/O	HPS_IOA_9	HPS_IOB_19	—
<i>continued...</i>					



HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
I2C_EMAC1_SCL	I2C EMAC1 Serial Clock	I/O	HPS_IOA_10	HPS_IOB_20	—
I2C_EMAC0_SDA	I2C EMAC0 Serial Data	I/O	HPS_IOA_11	HPS_IOB_11	HPS_IOB_23
I2C_EMAC0_SCL	I2C EMAC0 Serial Clock	I/O	HPS_IOA_12	HPS_IOB_12	HPS_IOB_24
MDIO2_MDIO	EMAC2 MDIO	I/O	HPS_IOA_7	HPS_IOB_9	—
MDIO2_MDC	EMAC2 MDC	Output	HPS_IOA_8	HPS_IOB_10	—
MDIO1_MDIO	EMAC1 MDIO	I/O	HPS_IOA_9	HPS_IOB_19	—
MDIO1_MDC	EMAC1 MDC	Output	HPS_IOA_10	HPS_IOB_20	—
MDIO0_MDIO	EMAC0 MDIO	I/O	HPS_IOA_11	HPS_IOB_11	HPS_IOB_23
MDIO0_MDC	EMAC0 MDC	Output	HPS_IOA_12	HPS_IOB_12	HPS_IOB_24

### 1.4.10. HPS I2C Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

In addition to the three I2C\_EMAC controllers, there are two additional I2C controllers (I2C0 and I2C1) for dedicated I2C usage in the Intel Agilex HPS.

The I2C protocol requires pull-up resistors to VCCIO\_HPS on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7-kΩ or lower.



**Table 24. HPS I2C Pins—Preliminary**

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)			
			Group 1	Group 2	Group 3	Group 4
I2C0 _SDA	I2C0 Serial Data	I/O	HPS_IOA_5	HPS_IOA_23	HPS_IOB_3	—
I2C0 _SCL	I2C0 Serial Clock	I/O	HPS_IOA_6	HPS_IOA_24	HPS_IOB_4	—
I2C1 _SDA	I2C1 Serial Data	I/O	HPS_IOA_3	HPS_IOA_21	HPS_IOB_7	HPS_IOB_13
I2C1 _SCL	I2C1 Serial Clock	I/O	HPS_IOA_4	HPS_IOA_22	HPS_IOB_8	HPS_IOB_14

### 1.4.11. HPS SPI Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 25. HPS SPI Pins—Preliminary**

There are two SPI Master (SPIM0 and SPIM1) and two SPI Slave (SPIS0 and SPIS1) controllers for the Intel Agilex HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the group)		
			Group 1	Group 2	Group 3
SPIM0_CLK	SPIM0 Clock	Output	HPS_IOA_5	HPS_IOB_21	HPS_IOB_21
SPIM0_MOSI	SPIM0 Master Out Slave In	Output	HPS_IOA_6	HPS_IOB_22	HPS_IOB_22
SPIM0_MISO	SPIM0 Master In Slave Out	Input	HPS_IOA_7	HPS_IOB_19	HPS_IOB_23
SPIM0_SS0_N	SPIM0 Slave Select 0 This is an active-low signal.	Output	HPS_IOA_8	HPS_IOB_20	HPS_IOB_24
SPIM0_SS1_N	SPIM0 Slave Select 1 This is an active-low signal.	Output	HPS_IOA_1	HPS_IOB_18	HPS_IOB_18
SPIM1_CLK	SPIM1 Clock	Output	HPS_IOA_9	HPS_IOA_21	HPS_IOB_1

*continued...*



HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the group)		
			Group 1	Group 2	Group 3
SPIM1_MOSI	SPIM1 Master Out Slave In	Output	HPS_IOA_10	HPS_IOA_22	HPS_IOB_2
SPIM1_MISO	SPIM1 Master In Slave Out	Input	HPS_IOA_11	HPS_IOA_23	HPS_IOB_3
SPIM1_SS0_N	SPIM1 Slave Select 0 This is an active-low signal.	Output	HPS_IOA_12	HPS_IOA_24	HPS_IOB_4
SPIM1_SS1_N	SPIM1 Slave Select 1 This is an active-low signal.	Output	HPS_IOA_2	HPS_IOA_20	HPS_IOB_5
SPIS0_CLK	SPIS0 Clock	Input	HPS_IOA_1	HPS_IOA_21	HPS_IOB_9
SPIS0_MOSI	SPIS0 Master Out Slave In	Input	HPS_IOA_2	HPS_IOA_22	HPS_IOB_10
SPIS0_MISO	SPIS0 Master In Slave Out	Output	HPS_IOA_4	HPS_IOA_24	HPS_IOB_12
SPIS0_SS0_N	SPIS0 Slave Select 0 This is an active-low signal.	Input	HPS_IOA_3	HPS_IOA_23	HPS_IOB_11
SPIS1_CLK	SPIS1 Clock	Input	HPS_IOA_9	HPS_IOB_5	HPS_IOB_21
SPIS1_MOSI	SPIS1 Master Out Slave In	Input	HPS_IOA_10	HPS_IOB_6	HPS_IOB_22
SPIS1_MISO	SPIS1 Master In Slave Out	Output	HPS_IOA_12	HPS_IOB_8	HPS_IOB_24
SPIS1_SS0_N	SPIS1 Slave Select 0 This is an active-low signal.	Input	HPS_IOA_11	HPS_IOB_7	HPS_IOB_23

### 1.4.12. HPS UART Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

**Table 26. HPS UART Pins—Preliminary**

There are two UART (UART0 and UART1) controllers for the Intel Agilex HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
UART0_CTS_N	UART0 Clear to Send This is an active-low signal.	Input	HPS_IOA_1	HPS_IOA_21	HPS_IOB_1
UART0_RTS_N	UART0 Request to Send This is an active-low signal.	Output	HPS_IOA_2	HPS_IOA_22	HPS_IOB_2
UART0_TX	UART0 Transmit	Output	HPS_IOA_3	HPS_IOA_23	HPS_IOB_3
UART0_RX	UART0 Receive	Input	HPS_IOA_4	HPS_IOA_24	HPS_IOB_4
UART1_CTS_N	UART1 Clear to Send This is an active-low signal.	Input	HPS_IOA_5	HPS_IOB_5	HPS_IOB_17
UART1_RTS_N	UART1 Request to Send This is an active-low signal.	Output	HPS_IOA_6	HPS_IOB_6	HPS_IOB_18
UART1_TX	UART1 Transmit	Output	HPS_IOA_7	HPS_IOB_7	HPS_IOB_15
UART1_RX	UART1 Receive	Input	HPS_IOA_8	HPS_IOB_8	HPS_IOB_16

### 1.4.13. HPS Trace Pins

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.



**Table 27. HPS Trace Pins—Preliminary**

You can select up to 16 trace output pins in the Intel Agilex HPS. These pins do not have to be located in the same quadrant.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
Trace_CLK	Trace Clock	Output	HPS_IOA_20
			HPS_IOB_20
Trace_D0	Trace Data 0	Output	HPS_IOA_21
			HPS_IOB_21
Trace_D1	Trace Data 1	Output	HPS_IOA_22
			HPS_IOB_22
Trace_D2	Trace Data 2	Output	HPS_IOA_23
			HPS_IOB_23
Trace_D3	Trace Data 3	Output	HPS_IOA_24
			HPS_IOB_24
Trace_D4	Trace Data 4	Output	HPS_IOA_19
			HPS_IOA_7
			HPS_IOB_19
			HPS_IOB_7
Trace_D5	Trace Data 5	Output	HPS_IOA_18
			HPS_IOA_6
			HPS_IOB_18
			HPS_IOB_6
Trace_D6	Trace Data 6	Output	HPS_IOA_17
			HPS_IOA_5
			HPS_IOB_17
			HPS_IOB_5

*continued...*



HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
Trace_D7	Trace Data 7	Output	HPS_IOA_16
			HPS_IOA_4
			HPS_IOB_16
			HPS_IOB_4
Trace_D8	Trace Data 8	Output	HPS_IOA_15
			HPS_IOA_3
			HPS_IOB_15
			HPS_IOB_3
Trace_D9	Trace Data 9	Output	HPS_IOA_14
			HPS_IOA_2
			HPS_IOB_14
			HPS_IOB_2
Trace_D10	Trace Data 10	Output	HPS_IOA_13
			HPS_IOA_1
			HPS_IOB_13
			HPS_IOB_1
Trace_D11	Trace Data 11	Output	HPS_IOA_12
			HPS_IOB_12
Trace_D12	Trace Data 12	Output	HPS_IOA_11
			HPS_IOB_11
Trace_D13	Trace Data 13	Output	HPS_IOA_10
			HPS_IOB_10
Trace_D14	Trace Data 14	Output	HPS_IOA_9

*continued...*





HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
			HPS_IOB_9
Trace_D15	Trace Data 15	Output	HPS_IOA_8 HPS_IOB_8

## 1.5. Intel Agilex Power Supply Sharing Guidelines

Intel Agilex devices have specific power-up and power-down sequence requirements. For more information, refer to the *AN692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria® 10, and Intel Stratix® 10 Devices* and *Intel Agilex Power Management User Guide*.

**Note:** Intel recommends you to generate a **.pin** file from the Intel Quartus Prime Fitter to verify power pin assignment. Intel also recommends using this **.pin** file to determine if it is safe to power down or ground certain power supplies for your specific design. This step will inform you to make the appropriate design choices for unused power supplies for your design.

### 1.5.1. Example 1—Intel Agilex

**Table 28. Power Supply Sharing Guidelines for Intel Agilex Device—Preliminary**

Example Requiring 9 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID <sup>(1)</sup> , 0.8V	± 3%	Switcher <sup>(2)</sup>	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. You have the option to connect VCCL_HPS to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG_HPS power to
VCCP					Share	
VCCL_HPS					Share	
VCCPLLDIG_HPS					Filter	

*continued...*

(1) For the SmartVID voltage range, refer to the *Intel Agilex Device Data Sheet*.

(2) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 4 of the *Notes to Intel Agilex Pin Connection Guidelines*.



Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
						<p>the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering.</p> <p>When implementing a filtered supply topology, you must consider the IR drop across the filter.</p> <p>If you do not intend to utilize the HPS in the Intel Agilex device, you must still provide power to these power supply pins. Do not leave the VCCL_HPS and VCCPLLDIG_HPS power supply pins floating or connected to GND.</p>
VCCH	2	0.9V	± 30mV	Switcher <sup>(2)</sup>	Share	<p>Connect the VCCH to a dedicated 0.9V power supply.</p> <p>When implementing a filtered supply topology, you must consider the IR drop across the filter.</p>
VCC_HSSI_GXE					Share	
VCCFUSE_GXP					Share	
VCC_HSSI_GXP					Share	
VCCH_SDM					Share	
VCCRT_GXE					Filter	
VCCRTPLL_GXE					Filter	
VCCRT_GXP					Filter	
VCCL_SDM	3	0.8V	± 3%	Switcher <sup>(2)</sup>	Share	<p>Connect the VCCL_SDM to a dedicated 0.8V power supply.</p> <p>When implementing a filtered supply topology, you must consider the IR drop across the filter.</p>
VCCPLLDIG_SDM					Filter	
VCCH_GXE	4	1.1V	± 3%	Switcher <sup>(2)</sup>	Isolate	Connect the VCCH_GXE to a dedicated 1.1V power supply.
VCCCLK_GXE	5	2.5V	± 5%	Switcher <sup>(2)</sup>	Isolate	Connect the VCCCLK_GXE to a dedicated 2.5V power supply.
VCCPT	6	1.8V	± 3%	Switcher <sup>(2)</sup>	Share	<p>Connect VCCPT to a dedicated 1.8V power supply. Connect VCCADC, VCCPLL_SDM, VCCPLL_HPS, and VCCCLK_GXP to the same power plane with proper isolation filtering. Depending</p>
VCCADC					Filter	
VCCPLL_SDM					Filter	

**continued...**



Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCPLL_HPS					Filter	on the regulator capabilities, you have the option to share this supply with multiple Intel Agilex devices. If you do not intend to utilize the HPS in the Intel Agilex device, you must still provide power to the HPS power supply pins. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCCLK_GXP					Filter	
VCCH_GXP					Filter	
VCCIO_PIO <sup>(3)</sup>	7	1.2V	± 5%	Switcher <sup>(2)</sup>	Share	Connect VCCIO_PIO, VCCIO_PIO_SDM, and VCCR_CORE to dedicated 1.2V power supply. Connect VCCA_PLL to the VCCIO_PIO supply with proper isolation filtering.
VCCIO_PIO_SDM					Share	
VCCA_PLL					Filter	
VCCR_CORE					Share	
VCCIO_SDM	8	1.8V	± 5%	Switcher <sup>(2)</sup>	Share	Connect VCCIO_SDM, VCCIO_HPS, and VCCBAT to dedicated 1.8V power supply.
VCCIO_HPS					Share	
VCCBAT					Share	
VCCFUSEWR_SDM	9	2.4V	± 50mV	Switcher <sup>(2)</sup>	Isolate	A 2.4V power supply is required on this pin if field-programming of the eFuses is required. If field-programming of the eFuses is not required, tie this pin to VCCPT or leave it unconnected (floating). Do not tie this pin to GND.  If field-programming of the eFuses is required, Intel recommends using an adjustable regulator set to 2.4V output when programming the eFuses and 1.8V otherwise.

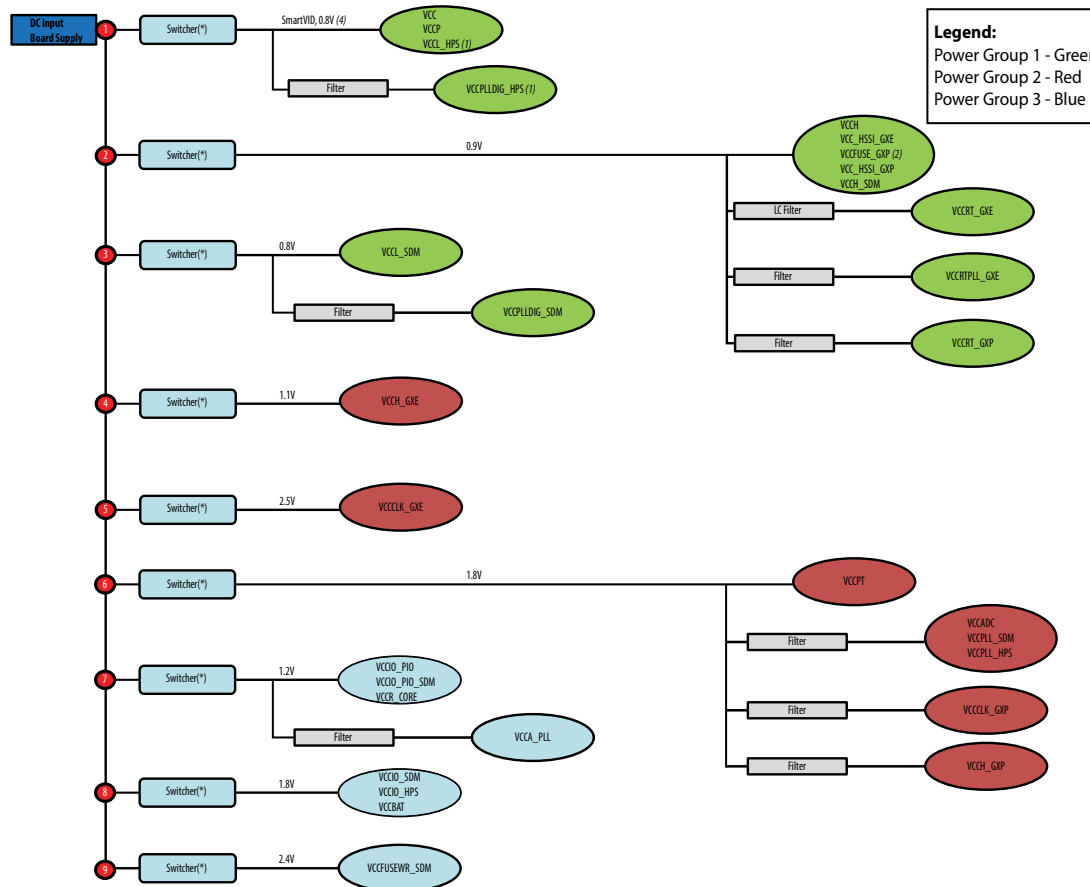
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Agilex device is provided in Figure 1.

The voltage level for each power rail is preliminary.

<sup>(3)</sup> The supported tolerance for the VCCIO\_PIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Agilex Device Data Sheet*. Use the Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.



Figure 1. Example Power Supply Sharing Guidelines for Intel Agilex Device –Preliminary



Notes:

- (1) VCCL\_HPS and VCCPLLIG\_HPS can run at 0.93V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator.
- (2) VCCFUSE\_GXP in this configuration does not support eFuse programming.
- (3) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT\_SCL and PWRMGT\_SDA pin functions.
- (4) When selecting a voltage regulator controller for SmartVID operation, you must choose a controller with the PMBus capability, a feedback node, and a selectable VID format. For example, 4 to 6 bits pattern.



## 1.6. Notes to Intel Agilex Device Family Pin Connection Guidelines

**Note:** Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. Use the Intel Agilex Early Power Estimator (EPE) to determine the preliminary current requirements for VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
2. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
3. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express (PCIe) protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
4. Low Noise Switching Regulator—defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response. The switching frequency range is not an Intel requirement.
5. There are no dedicated PR\_REQUEST, PR\_ERROR, and PR\_DONE pins. If required, you can use user I/O pins for these functions.
6. The device orientation is die view (bottom of chip view).

### Related Information

- [Intel Agilex Power Supply Sharing Guidelines](#) on page 49
- [Intel Agilex General Purpose I/O and LVDS SERDES User Guide](#)

## 1.7. Document Revision History for the Intel Agilex Device Family Pin Connection Guidelines

Document Version	Changes
2019.06.10	Initial release.