Sub-Bank	Package Name	Index within I/O Bank	Index within I/O Sub-Bank	DDR4 Scheme 1: Component and DIMM (Supports Supports up to 4 ranks for UDIMM/RDIMM/SO-DIMM/Component)	DDR4 Scheme 1A: Component, LRDIMM and RDIMM (with base component x16Gb x4DQ/DQS group)	DDR4 Scheme 2: Component and DIMM (Supports up to 2 ranks for UDIMM/RDIMM/SO-DIMM/Component). Used for HPS EMIF	DDR4 Scheme 3: Component and DIMM, with 3DS (Support 3DS; Supports ; Supports up to 4 ranks for UDIMM/RDIMM/SO-DIMM/Component)	DDR4 Scheme 3A: Component and DIMM, with 3DS (Support 3DS; Supports ; Supports up to 4 ranks for UDIMM/RDIMM/SO-DIMM/Component)	RLDRAM3 Scheme 1	QDR-IV Scheme 1
Lane 3	LVDSXX_1N	47	11	CK_N_1	CK_N_1	Not used by Address/Command pins in this scheme; usable as Data pins. In HPS mode, ECC pins must be placed here.	CK_N_1	CK_N_1	Not used by Address/Command or Data Pins	LBK1_N_0
	LVDSXX_1P	46	10	CK_1	CK_1		CK_1	CK_1		LBK0_N_0
	LVDSXX_2N	45	9	CK_N_3						A_24
	LVDSXX_2P	44	8	CK_3	ALERT_N			ALERT_N		A_23
	LVDSXX_3N	43	7	CK_N_2			CS_3	CS_3		
	LVDSXX_3P	42	6	CK_2			CS_2	CS_2		AP
	LVDSXX_4N	41	5	CKE_3			CKE_3	CKE_3		
	LVDSXX_4P	40	4	CKE_2			CKE_2	CKE_2		
	LVDSXX_5N	39	3	ODT_3			ODT_3	ODT_3		A_22
	LVDSXX_5P	38	2	ODT_2			ODT_2	ODT_2		A_21
	LVDSXX_6N	37	1	CS_N_3			C_1	C_1		A_20
	LVDSXX_6P	36	0	CS_N_2			C_0	C_0		A_19
Lane 2	LVDSXX_7N	35	11	BG_0	BG_0	BG_0	BG_0	BG_0	BA_2	A_18
	LVDSXX_7P	34	10	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	A_17
	LVDSXX_8N	33	9	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	A_16
	LVDSXX_8P	32	8	ALERT_N	A_17	ALERT_N	ALERT_N	A_17	A_17	A_15
	LVDSXX_9N	31	7	A_16	A_16	A_16	A_16	A_16	A_16	PE_N
	LVDSXX_9P	30	6	A_15	A_15	A_15	A_15	A_15	A_15	A_14
	LVDSXX_10N	29	5	A_14	A_14	A_14	A_14	A_14	A_14	
	LVDSXX_10P	28	4	A_13	A_13	A_13	A_13	A_13	A_13	
	LVDSXX_11N	27	3	A_12	A_12	A_12	A_12	A_12	A_12	A_13
	LVDSXX_11P	26	2	RZQ Site						
	LVDSXX_12N	25	1	Differential "N-Side" Reference Clock Input Site (LVDS Reference Clock Only)						
	LVDSXX_12P	24	0	Single-Ended or Differential "P-Side" PLL Reference Clock Input Site						
Lane 1	LVDSXX_13N	23	11	A_11	A_11	A_11	A_11	A_11	A_11	A_12
	LVDSXX_13P	22	10	A_10	A_10	A_10	A_10	A_10	A_10	A_11
	LVDSXX_14N	21	9	A_9	A_9	A_9	A_9	A_9	A_9	A_10
	LVDSXX_14P	20	8	A_8	A_8	A_8	A_8	A_8	A_8	A_9
	LVDSXX_15N	19	7	A_7	A_7	A_7	A_7	A_7	A_7	RESET_N_0
	LVDSXX_15P	18	6	A_6	A_6	A_6	A_6	A_6	A_6	A_8
	LVDSXX_16N	17	5	A_5	A_5	A_5	A_5	A_5	A_5	
	LVDSXX_16P	16	4	A_4	A_4	A_4	A_4	A_4	A_4	
	LVDSXX_17N	15	3	A_3	A_3	A_3	A_3	A_3	A_3	A_7
	LVDSXX_17P	14	2	A_2	A_2	A_2	A_2	A_2	A_2	A_6
	LVDSXX_18N	13	1	A_1	A_1	A_1	A_1	A_1	A_1	A_5
	LVDSXX_18P	12	0	A_0	A_0	A_0	A_0	A_0	A_0	A_4
Lane 0	LVDSXX_19N	11	11	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	REF_N_0	A_3
	LVDSXX_19P	10	10	CS_N_1	CS_N_1	CS_N_1	CS_N_1	CS_N_1		A_2
	LVDSXX_20N	9	9	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	A_1
	LVDSXX_20P	8	8	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	A_0
	LVDSXX_21N	7	7	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	WE_N_0	CFG_N_0
	LVDSXX_21P	6	6	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	A_20	AINV_0
	LVDSXX_22N	5	5	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	A_19	CK_N_0
	LVDSXX_22P	4	4	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	A_18	CK_0
	LVDSXX_23N	3	3	ACT_N_0	ACT_N_0	ACT_N_0	ACT_N_0	ACT_N_0	CS_N_1	LDB_N_0
	LVDSXX_23P	2	2	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	LDA_N_0
	LVDSXX_24N	1	1	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RWB_N_0
	LVDSXX_24P	0	0	BG_1	BG_1	BG_1	BG_1	BG_1	BA_3	RWA_N_0

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Date	Version	Changes Made
July 2019	2019.07.17	Initial release.

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