Altera's 28 nm Device Portfolio

ALTERA®

MEASURABLE ADVANTAGE™

One Size Does Not Fit All

What do you do when system performance demands threaten to increase power consumption and cost? What happens if you've got the power you need but not the performance?

Wouldn't it be great if you didn't have to sacrifice one benefit to gain another?

That's the thinking behind the Altera® 28 nm device portfolio. Whether you need the highest performance, the lowest cost, or something in between, our process strategy is tailored to your design needs. So you'll get just what you need to differentiate your products without any tradeoffs.

The portfolio includes:

- **Cyclone® V FPGAs**: The industry's lowest system cost and power, along with performance levels ideal for differentiating high-volume applications
- **Arria® V FPGAs**: The optimal balance of power, performance, and system cost for midrange applications
- **Stratix® V FPGAs**: The highest bandwidth, density, and performance at the lowest total power for high-end designs
- **Cyclone V and Arria V SoCs:** The performance, power, and cost savings of hard logic with the flexibility and time-to-market benefits of programmable logic

In our newest devices, you get abundant hard intellectual property (IP) blocks. You'll be able to reduce design time, related soft costs, and power, while getting the performance you need. What's more, you also get a broad set of soft and hard embedded processor cores from Altera (Nios® II processor), and partners (such as Freescale's V1 ColdFire), all using a common design flow.

Low-Cost CPLD Family

In addition to 28 nm FPGAs, Altera's MAX® V CPLDs provide the industry's best value with their mix of low price, low power, and robust features for general-purpose and portable applications. You'll get:

- A non-volatile architecture for fast performance of "boot loader" functions
- Up to 50 percent lower total power versus competing CPLDs, with static power as low as 45 µW
- Packages as small as 20 mm^2

Our latest programmable devices are supported by rich design resources and meet your unique needs.

Why Process Matters

Altera's 28 nm devices were developed on two different processes from Taiwan Semiconductor Manufacturing Corporation (TSMC). Because each process is optimized for a specific set of advantages, the portfolio of devices is capable of meeting a wide range of design requirements.

- TSMC's 28 nm Low Power (28LP) process is optimized for lowest power and cost, delivering up to 50 percent lower dynamic power versus the previous generation. The Cyclone V and Arria V FPGAs are manufactured on the 28LP process.
- TSMC's 28 nm High Performance (28HP) process is optimized for highest bandwidth without exceeding your power budget, yielding 35 percent faster devices versus the 28LP process. The Stratix V and FPGAs are manufactured on the 28HP process.

Devices for All Your Needs

We've pushed the envelope in device architecture, transceiver technology, and hard IP blocks. The result? An array of differentiated devices to meet your design requirements.

Cyclone V FPGAs: Lowest Cost and Power

- Includes three variants:
  - Cyclone V E FPGA with logic only
  - Cyclone V GX FPGA with 3.125 Gbps transceivers
  - Cyclone V GT FPGA with 6.144 Gbps transceivers
- 3.3 V I/Os
- Multifunction PCI Express® (PCIe®) Gen2 x2
- Hard memory controllers for DDR3 (400 MHz), Mobile DDR2, and LPDDR2
- Most designs under 5 W of power

Arria V FPGAs: Balanced Power, Performance, and System Cost

- Includes three variants:
  - Arria V GX FPGA with 6.5536 Gbps transceivers
  - Arria V GT FPGA with 10.3125 Gbps transceivers
  - Arria V GZ FPGA with 12.5 Gbps transceivers
- Variable-precision DSP blocks
- Hard PCIe Gen2 x4 and Gen1 x8 with multifunction support in Arria V GX and GT FPGAs, up to Gen3 x8 in Arria V GZ FPGAs
- Hard memory controller (DDR3 at 500 MHz) or soft memory controller (DDR3 at 667 MHz) for Arria V GX and GT FPGAs, soft memory controller (DDR3 at 800 MHz) for Arria V GZ FPGAs
- Three power rails for simple power network design in Arria V GX and GT FPGAs

Stratix V FPGAs: Highest Bandwidth, Density, and Performance

- Includes four variants:
  - Stratix V E FPGA with logic only
  - Stratix V GS FPGA with 14.1 Gbps transceivers, optimized for DSP applications
  - Stratix V GX FPGA with 14.1 Gbps transceivers, optimized for logic applications
  - Stratix V GT FPGA with 28.05 Gbps and 14.1 Gbps transceivers
- High-performance memory controllers for DDR3 at 1066 MHz/2132 Gbps, RLDRAMII, and QDR II+ SRAM
- Embedded hard IP for PCIe Gen3
- Highest flexibility variable-precision digital signal processing (DSP) blocks

Cyclone V and Arria V SoCs: Extending the Portfolio

- Industry-leading integration with an ARM®-based hard processor subsystem (HPS)
- Rich software development ecosystem inherited from ARM Cortex™-A9 MPCore™ processors includes software development tools, operating systems, and middleware
- Efficient 8-input adaptive logic module (ALM)
- New 10 Kb internal memory blocks (M10K)
- New 640 bit memory logic array blocks (MLABs)
- Variable-precision DSP blocks
- Fractional phase-locked loops (PLLs) to reduce external oscillator needs
- Highly flexible clocking network
- Power-optimized MultiTrack routing architecture
- Includes three Cyclone SoC variants:
  - Cyclone V SE SoC with ARM-based HPS and logic
  - Cyclone V SX SoC with with ARM-based HPS and 3.125 Gbps transceivers
  - Cyclone V ST SoC with with ARM-based HPS and 5 Gbps transceivers
- Includes two Arria SoC variants:
  - Arria V SX SoC with ARM-based HPS and 6.375 Gbps transceivers
  - Arria V ST SoC with ARM-based HPS and 10.3125 Gbps transceivers

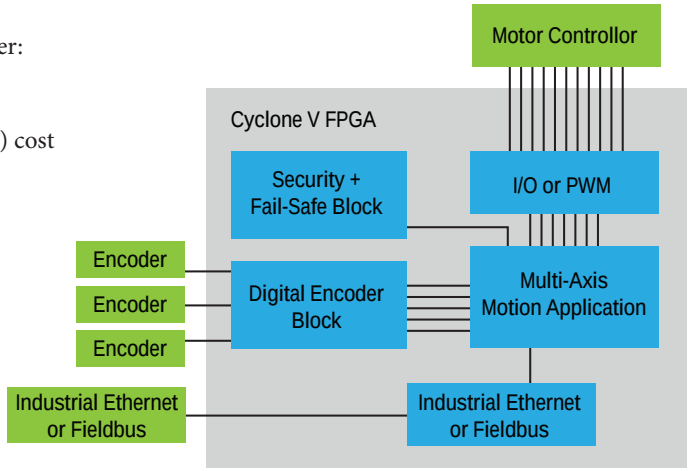
Where You Can Use Our Newest Devices

Here's a sampling of applications where you can take advantage of the capabilities in our newest device families.

Motor Controller

For motor control applications, Cyclone V FPGAs deliver:

- <5-W power
- Fewer components for reduced bill of materials (BOM) cost
- Native floating-point support in all DSP blocks
- Ability for you to quickly adapt to evolving Industrial Ethernet protocols
- User-friendly partial reconfiguration, which lets you change core and transceiver functionality on the fly while other portions of your design are running
- >15-year life cycle, supporting long life spans of industrial equipment

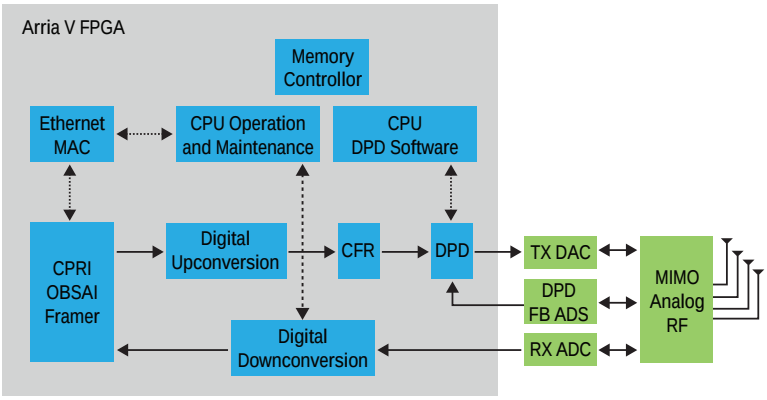


- Integrated security to protect your design from cloning and reverse engineering
- Single event upset (SEU) detection and mitigation

Remote Radio Head

For remote radio heads, Arria V FPGAs deliver:

- <10 W power
- Up to 35 transceivers at up to 6.375 Gbps on GX variant; 90 mW per transceiver channel at 6.375 Gbps
- Up to six transceivers at up to 10.3125 Gbps on GT variant; 135 mW per transceiver channel at 10.3125 Gbps
- Native support for finite impulse response (FIR) filters in variable-precision DSP blocks
- Hard memory controller with support for DDR3 at 533 MHz

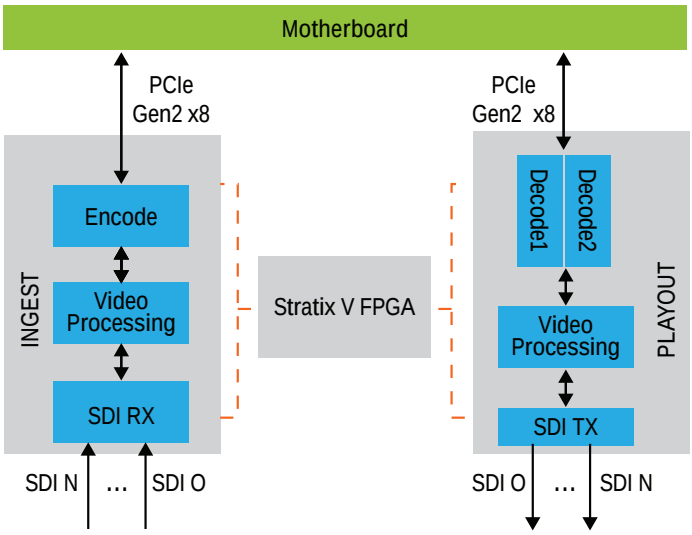


- Efficient resource utilization via two full 18x19-bit paths on each DSP block

Studio Video Server

For studio video servers, Stratix V FPGAs deliver:

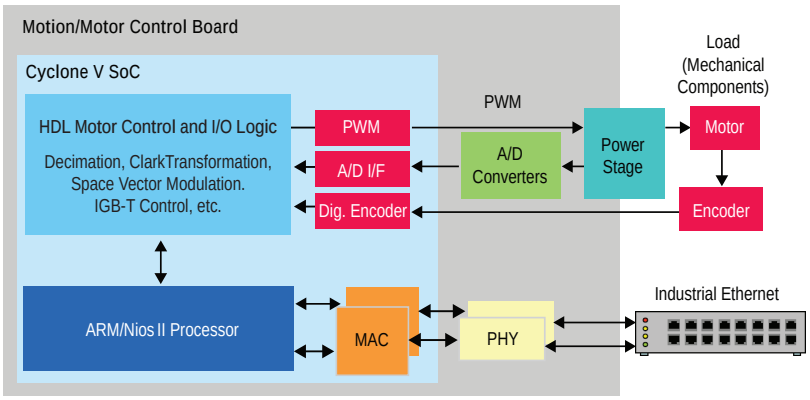
- Support for multiple coder/decoders (CODECs) through user-friendly partial reconfiguration
- Native 10 bit memory support for faster video buffering of larger and more frames
- Efficient video processing with high ratio of multipliers and memory to logic
- Productivity-enhancing solution supported by Video and Image Processing Suite of IP cores



Industrial Networking

For industrial networking applications, Cyclone V SoCs deliver:

- Higher bandwidth and performance at a lower total cost of ownership (TCO)
- A single hardware platform that can support multiple Industrial Ethernet and fieldbus protocol standards
- Ability to reconfigure the FPGA during manufacturing or even in the field to accommodate any changes in Ethernet specifications

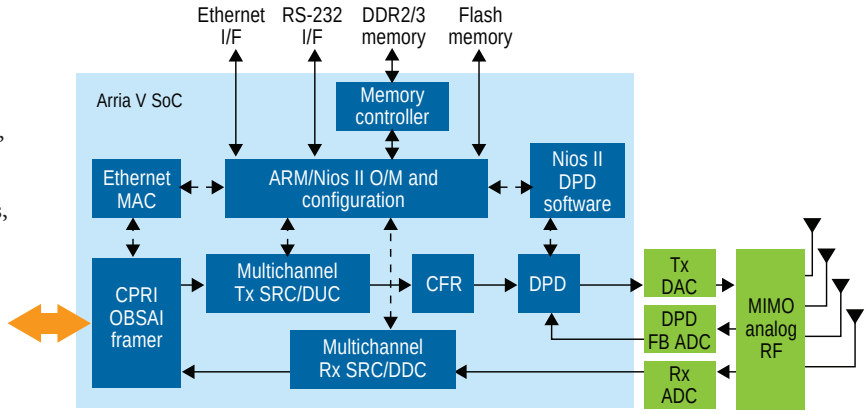


- Support for different standards without the need for multiple dedicated adapter cards

LTE RF Card Solutions

For wireless applications, Arria V SoCs deliver:

- High-performance, power-efficient, scalable silicon platform
- Sample rate converter (SRC) blocks, such as digital upconverter (DUC), digital downconverter (DDC), crest-factor reduction (CFR), and digital predistortion (DPD) blocks, can be implemented efficiently
- Future proofing via support for in-field programmability.



Notes:
1. O&M = Operation and maintenance
2. CPRI = Common Public Radio Interface
3. OBSAI = Open Base Station Standard Initiative

Common Design Toolset = Better Productivity

Our 28-nm device families are supported by a common, productivity-enhancing design environment. A set of common software tools and design resources equip you to swiftly turn your concepts into revenue-generating applications:

- **Quartus® II software, including the Qsys system integration tool and PowerPlay power analysis tool:** Quartus II software is number one in performance and productivity for CPLD, FPGA, and SoC designs, providing the fastest path to convert your concept into reality. Quartus II software also supports many third-party tools in synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.
- **Embedded processors:** For efficient implementation of software-oriented features. Our multi-vendor, multi-CPU architecture system-on-a-chip (SoC) platform includes ARM, MIPS, and Nios II processor options to offer the industry's broadest selection of soft processors, software development tools, OS support, and embedded IP cores. Choose from Altera's customizable processor portfolio to meet your real-time, safety, and power- and cost-sensitive processing needs.
- **Soft IP functions:** For quick and easy implementation of hardware functions. Altera and partners provide a wide variety of IP blocks of differing size and complexity, from the basic arithmetic blocks to transceivers, memory controllers, microprocessors, signal processing, and protocol interfaces.
- **Development kits, daughter cards, and programming hardware:** Altera provides a variety of hardware solutions and tools to accelerate the design process. Together with selected partners, Altera offers a wide range of development kits and daughter cards that contain everything an engineer needs to create and implement a design in hours.
- **Instructor-led, virtual, and online classes:** Altera offers an extensive curriculum of classes to deepen your expertise. Our classes are beneficial whether you're new to FPGA and CPLD design, or are an advanced user wanting an update on the latest tools, tips, and tricks.

Measurable Advantage

When system performance, power, and cost requirements clash, you've got a solution in our 28 nm device portfolio. Create differentiated products with less time and effort.

Get more details about our 28 nm device portfolio by contacting your local Altera® sales representative or FAE or by visiting **www.altera.com/28nmportfolio**.

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1494 602000

Altera Japan Ltd.
Shinjuku i-Land Tower 32F
6-5-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.
Unit 11-18, 9/F
Millennium City 1, Tower 1
388 Kwun Tong Road
Kwun Tong
Kowloon, Hong Kong
Telephone: (852) 2945 7000

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