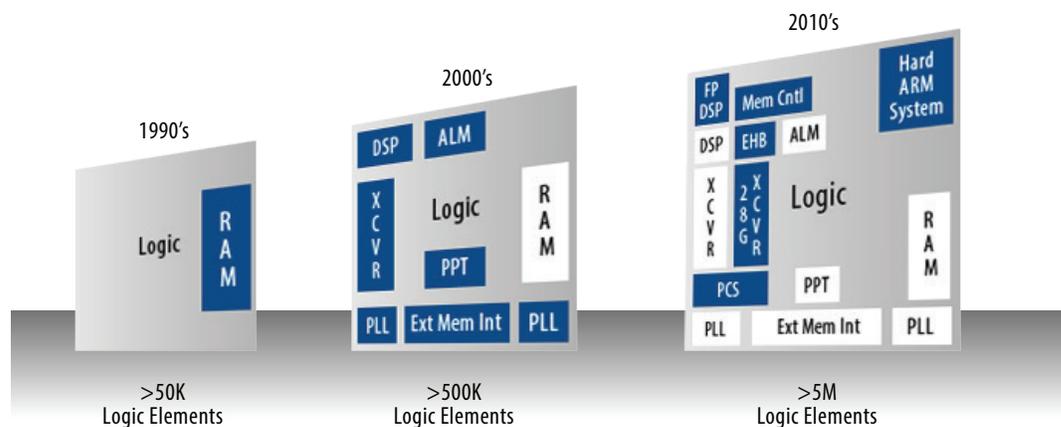




## Spectra-Q Engine



FPGAs and SoCs have taken huge leaps with next-generation capabilities. These include multi-million logic elements, complex interface protocols, features such as PowerPlay Technology, Embedded hard blocks, and hard intellectual property (IP) blocks, including digital signal processor (DSP) and micro-processors. Designers need new software tools to reduce overall design time, risks, and costs, while dramatically improving design productivity and time-to-market for next-generation programmable devices. Traditionally, FPGA design tools have focused on reducing compile times. This dimension, while important, is not sufficient to reduce time-to-market challenges for the next decade.

- Spectra-Q™ adds a second dimension to design productivity—reducing the number of design iterations – while also dramatically reducing absolute compile time. Spectra-Q is a new engine that features: A new set of synthesis, placement, routing, and timing analysis algorithms. These algorithms utilize the hierarchical database and modern computing platforms to provide compile time improvements of up to 8X.
- A new, hierarchical database that enables preservation of design implementation at any stage — from synthesis to route. Design iterations are drastically reduced due to a “compile-once” IP or design block methodology.
- A unified compiler technology that enables different design entry tools. These design entry tools offer support for a wide variety of design languages including OpenCL, C/C++ etc. With the wide offering of design entry tools, designers can target FPGAs with greater efficiency in the language or design environment they prefer.

## Faster Compile Times

The Spectra-Q engine reduces compilation time of a design by up to 8X. This dramatic reduction is enabled by the new hierarchical database and the powerful algorithms that utilize the database. Spectra-Q tackles compile time along three separate angles - a new set of faster and improved Synthesis, Placement, Routing and Timing algorithms which speed up compiles by 2X, a new incrementally optimized flow reduces full compile times by 2X and finally, distributed compile, which makes use of advanced multi-core processor and computer farm or cloud technologies to provide a further 2X boost.

### Faster Algorithms

The Spectra-Q engine features improved Synthesis, Place, Route and Timing algorithms that take advantage of multi-core workstations resulting in a 2X compile time speed up. Each of these compiler stages has been re-written to make it faster and more scalable. For example:

- The new synthesis engine has improved language support as well as a 2x speed up in synthesis compile time.
- The new placement flow utilizes a hybrid placement technique – a combination of an initial analytical placement based on mathematical equations, followed by simulated annealing techniques for finer grained placement. This hybrid placement technique provides overall improved quality and predictability of results at high utilization and is designed to scale beyond 5M+ logic elements.
- Spectra-Q introduces updated routing algorithms which are now composed of a phase of Global Routing followed by traditional Detailed Routing. This router provides improved results for congested designs, and ensures that the algorithm can scale to handle larger devices.
- Finally, the updated timing algorithms are highly parallel, taking advantage of multi-core CPUs and are designed for 16-CPU's and beyond. These highly parallelized timing algorithms provide a significant speed up of 2X.

### Incremental Optimizations

In addition to the above algorithm improvements, the Spectra-Q engine allows you to reduce or even avoid full design recompiles by running granular compiles. If you need to run a certain stage of the compilation again – synthesis, placement, routing or timing, you have the ability to do just that without going through an entire compilation, making the compilation flow more granular and allowing you to incrementally optimize your design at each stage. Precise control over the compilation process is achieved by stopping the compiler, fine-tuning your design and incrementally run the compilation stage. An average of 2X compile time improvement is enabled by these incremental optimizations.

For smaller design changes (<5% change) on non-critical paths, Spectra-Q also allows you to preserve the placement, routing and timing for the rest of your unchanged design. For example, the Spectra-Q engine powers the Rapid Recompile feature, which reuses synthesis and place-and-route information to streamline processing for small, incremental design changes. Rapid Recompile results in up to 3X faster compilation for pre-synthesis HDL changes, and up to 4X faster compilation for post-fit SignalTap™ II Logic Analyzer modifications.

## Distributed Compile



As we look at the growing complexity and size of FPGA applications, distributed computing will become essential to solve these challenges. The hierarchical database of the Spectra-Q engine allows for efficient distributed compilation of a single design. Distributed compilations allow you to partition your design and compile each of these partitions in parallel over multiple computers in a server farm, dramatically reducing your overall compilation time.

## Reduced Design Iterations

The new Spectra-Q engine contains tools and capabilities to reduce the number of design iterations across the I/O design, debug, and timing closure stages. The Spectra-Q engine includes a hierarchical database, allowing you to fully preserve your IP once it is compiled, resulting in fewer design iterations. Reducing the number of design iterations helps bring your product to market faster.

### BluePrint Reduces Iterations by 10X

Built on top of the Spectra-Q engine is an industry first tool called BluePrint Platform Designer that allows you to perform architectural exploration and assign interfaces with much greater efficiency. In the past, one had to wait for a full compile and only once the fitter check was done, would the complex error messages show up, indicating illegal assignments. The BluePrint Platform Designer enables you to explore a device's peripheral architecture and efficiently assign interfaces. It prevents illegal pin assignments by performing fitter and legal checks in real time eliminating complex error messages and the need to wait for a full compile, speeding up your I/O design by 10X. The tool also includes a clock-planning feature that greatly reduces the number of design iterations needed for timing closure.

BluePrint enables dragging and dropping entire interfaces (for example: a DDR4 by 72 interface) on the chip floor plan (or on the package view) into a set of legal locations that is computed live, in seconds. BluePrint provides guidance on pin assignments by performing legal, fitter checks in real time. The graphical, legal placement eliminates the debug of complex error messages, and also the need to wait for a full compile, significantly speeding up your I/O design.

### **Hierarchical Design Reduces Iterations by 3X**

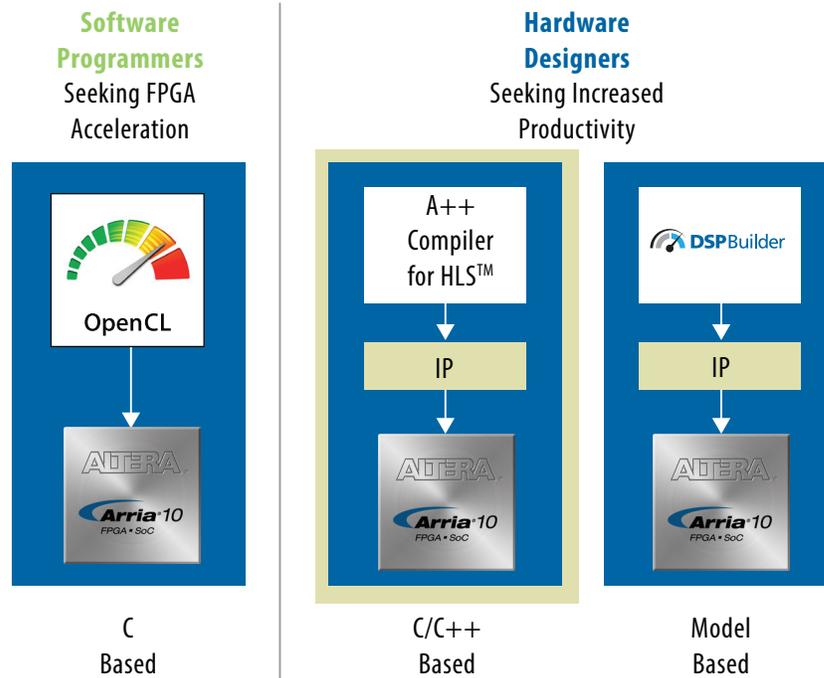
Multi-million logic element (LE) designs provide the equivalent of tens of millions of ASIC gates. Designs of this complexity benefit from hierarchical methodology. A typical top-down design flow may involve designs that are partitioned into 3 to 10 blocks that can be physically floor planned with associated timing constraints for each block. In the previous approach, once an IP was compiled, the compiler used a net list that came with placement and routing assignments to place the IP – this placement information was often modified to accommodate additional placement requirements of the logic elements, requiring a complete recompile with the new modifications. With the Spectra-Q hierarchical database, each partition can now be fully preserved with detailed routing and post-route information. The new database does not require a recompile when the partitions are integrated at the top level. Timing of each partition is fully preserved and undisturbed during top-level integration or when other partitions need to be recompiled due to a register transfer level (RTL) change. The Spectra-Q hierarchical design flow reduces full compile iterations by 3X.

### **Faster Design Entry**

The Spectra-Q engine provides a unified compiler technology enabling a quick deployment of multiple design entry methods. The technology fast-tracks design entry for hardware, software, and digital signal processing (DSP) designers. The first step in the flow translates your design into a common, intermediate format, followed by an optimization step that generates HDL for the Quartus Prime software. With multiple design entry methods, designers can target FPGAs with greater efficiency in the language they prefer. Designers can choose to develop in their preferred development environments (or IDEs - Integrated Development Environments).

- C or C++ based - The Spectra-Q engine is designed to support Altera's new A++ Compiler for high-level synthesis to create IP cores from C or C++, which significantly boosts productivity through faster architecture exploration, development and simulation.
- C-based (Open Computing Language (OpenCL™)) - Software developers can use a familiar C-based design flow with the Altera SDK for OpenCL. The SDK supports a software development flow that abstracts away traditional FPGA hardware flows.
- Model-based - The DSP Builder tool supports a model-based design flow to generate HDL from your DSP algorithms directly from within the MathWorks Simulink software.

In addition to the above, Spectra-Q includes a new HDL synthesis engine that supports all standard HDL languages, including SystemVerilog and VHDL-2008.



## Conclusion

The Spectra-Q engine provides a powerful platform for your most complex designs. New tools provide more control and predictability at all stages of design planning and implementation. Spectra-Q successfully tackles the productivity challenge by not only decreasing compile times, but also reducing the total number of design iterations.