AN 792: Intel FPGA JESD204B IP Core and ADI AD9371 Hardware Checkout Report
Contents

Intel FPGA JESD204B IP Core and ADI AD9371 Hardware Checkout Report................. 3
  Hardware Requirements................................................................................................................ 3
  Hardware Setup......................................................................................................................... 4
  AD9371 EVM Software Setup................................................................................................. 6
  Hardware Checkout Methodology for JESD204B Transmitter............................................... 10
    Transmitter Data Link Layer........................................................................................................ 10
    Transmitter Transport Layer....................................................................................................... 13
    Scrambling.............................................................................................................................. 13
  JESD204B IP Core and DAC Configurations........................................................................... 14
  Hardware Checkout Methodology for JESD204B Receiver.................................................... 15
    Receiver Data Link Layer........................................................................................................... 15
    Receiver Transport Layer.......................................................................................................... 18
    Descrambling.......................................................................................................................... 18
  JESD204B IP Core and Main ADC Configurations................................................................. 19
  Deterministic Latency (Subclass 1)............................................................................................ 20
  Test Results.............................................................................................................................. 22
  Test Result Comments.............................................................................................................. 26
  Document Revision History for AN 792: Intel FPGA JESD204B IP Core and ADI AD9371
    Hardware Checkout Report...................................................................................................... 27
Intel FPGA JESD204B IP Core and ADI AD9371 Hardware Checkout Report

The Intel FPGA JESD204B IP Core is a high-speed point-to-point serial interface intellectual property (IP).

The JESD204B IP core has been hardware-tested with a number of selected JESD204B-compliant ADC (analog-to-digital converter) DAC (digital-to-analog) devices.

This report highlights the interoperability of the JESD204B IP core with the AD9371 converter evaluation module (EVM) from Analog Devices Inc. (ADI). The following sections describe the hardware checkout methodology and test results.

The AD9371 is a wideband RF transceiver offering dual channel transmitters and receivers, integrated synthesizers, and digital signal processing functions. Its high speed JESD204B interface supports lane rates up to 6144 Mbps.

Related Links
JESD204B IP Core User Guide

Hardware Requirements

The hardware checkout test requires the following hardware and software tools:

- Intel® Arria® 10 GX FPGA Development Kit
- ADI AD9371-PCBZ EVM
- Mini-USB cables
- SMA Cables
- Oscilloscope/Spectrum Analyzer
- Clock source capable of generating 122.88MHz

Related Links
Arria 10 GX FPGA Development Kit
Development kit information and ordering code.
Hardware Setup

An Intel Arria 10 GX Development Kit is used with the ADI AD9371 daughter card module installed to the FMC connector A of the development board.

- The AD9371 EVM derives power from FMC pins.
- The clock generator AD9528 is available on the EVM. The reference clock for AD9528 is sourced from external clock.
- The device clocks for both converter and FPGA are generated by AD9528.
- The FPGA device clock is supplied through FMC pins. The link and frame clocks are generated from this device clock using Intel IOPLL.
- For subclass 1, AD9528 clock generator on the EVM generates SYSREF for both FPGA and AD9371. The sysref for FPGA is supplied through FMC pins.
- The sync_n signal is transmitted from
  - the DAC of AD9371 to FPGA through FMC.
  - the FPGA to ADC of AD9371 through FMC.
Figure 1. Hardware Setup

The following system-level diagram shows how the different modules connect in this design.
Figure 2. System Diagram

Note: The IOPLL input reference clock is sourcing from device clock through the global clock network. Sourcing reference clock from a cascaded PLL output, global clock or core clock network might introduce additional jitter to the IOPLL and transceiver PLL output. Refer to this KDB Answer for a workaround you should apply to the IP core in your design.

In this setup, the maximum data rate of transceiver lanes is 6.144Gbps. The clock generator available on the EVM is used for clocking both the EVM and the FPGA. The SPI master in FPGA programs both AD9371 registers and AD9528 clock generator registers available on the EVM through 4 wire SPI interface via FMC pins. The reference clock for this clock generator has to be provided by an external clock source. The converter device clock, FPGA device clock, and SYSREF (for both FPGA and converters) are generated by AD9528. FPGA receives these clocks through FMC pins. The converters operate in a single JESD link in all configurations with a maximum of 4 lanes.

AD9371 EVM Software Setup

The AD9371 Transceiver evaluation software is used to generate the setup files for the AD9371 device and AD9528 clock generator for JESD204B link operation. For more information about AD9371 Transceiver evaluation software, visit the Analog website.

Setup files for each of the parameter configurations are included in the software installation in the form of predefined profiles. You need to generate the C scripts using the profiles with correct settings for the JESD204B link to operate at the targeted data rate and JESD204B link parameters.

Follow these steps to generate the configuration C scripts via the AD9371 Transceiver evaluation software graphical user interface (GUI):

1. Start the AD9371 Transceiver Evaluation Software (TES). Figure 3 on page 7 shows the opening page of TES.
2. In the case when evaluation hardware is not connected, the user can still use the software in demonstration mode by following these steps:
   a. Click Connect (top left corner).
   b. The Zynq board is disconnected message appears; click OK. After clicking OK, the software enters demonstration mode in which a subset of all features is displayed as shown in Figure 4 on page 8.

3. The first tab displayed is the Configuration tab. Selecting this tab opens the initial screen, as shown in Figure 4 on page 8. The following selections are available from this tab:
   a. Device clock frequency
   b. Number of active Rx channels
   c. Number of active Tx channels
   d. Select observation/Sniffer input
   e. Select profiles for Rx, Tx, ORx, and Sniffer Rx
   f. Select Rx, Tx, and SnRx/ORx RF frequency

4. The AD9371 provides a observation receiver (ORx ADC). The SERDES for main receiver datapath and observation receiver datapath are shared, but they have independent JESD204B framers (For more information, refer to the AD9371 User Guide). In this interoperability report, only the main ADC datapath has been considered.
5. Set the Configurations based on the requirements and move to JESD204b setup tab, which appears as shown in Figure 5 on page 9.

6. In this tab, set the required JESD link parameters and lane rate for both Tx Deframer (DAC) and Rx Framer (Main ADC).
7. After configuring the GUI with required settings, the C scripts for configuring the EVM can be generated by clicking on Tools -> Create Script -> C script as shown in Figure 6 on page 9. Save the file with name “myk_config” so that the existing software makefiles can be used for compiling the scripts.

Related Links
- AD9371 Transceiver evaluation software
- AD9371 User Guide
Hardware Checkout Methodology for JESD204B Transmitter

The following section describes the test objectives, procedure, and the passing criteria for JESD204B transmitter.

- Transmitter data link layer
- Transmitter transport layer
- Scrambling
- Deterministic latency (Subclass 1)

Transmitter Data Link Layer

This test area covers the test cases for code group synchronization (CGS) and initial lane alignment sequence (ILAS).

On link start up, the receiver issues a synchronization request and the transmitter transmits /K/ (K28.5) characters. The Signal Tap Logic Analyzer tool monitors the transmitter data link layer operation.

Code Group Synchronization (CGS)

Table 1. CGS Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX_CGS.1</td>
<td>Check that /K/ characters are transmitted when sync_n is asserted.</td>
<td>The following signals in &lt;ip_variant_name&gt;_inst_phy.v are tapped:</td>
<td>• /K/ character or K28.5 (0xBC) is transmitted at each octet of the jesd204_tx_pcs_data bus when the receiver asserts the sync_n signal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• jesd204_tx_pcs_data[[(L*32)-1:0]</td>
<td>• The jesd204_tx_pcs_kchar_data signal is asserted whenever control characters like /K/ characters are transmitted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• jesd204_tx_pcs_kchar_data[[(L*4)-1:0]</td>
<td>• The jesd204_tx_int is deasserted if there is no error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The txlink_clk is used as the sampling clock for the Signal Tap.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Each lane is represented by 32-bit data bus in jesd204_tx_pcs_data. The 32-bit data bus for is divided into 4 octets.</td>
<td></td>
</tr>
<tr>
<td>TX_CGS.2</td>
<td>Check that /K/ characters are transmitted after sync_n is deasserted but before the start of multiframe.</td>
<td>The following signals in &lt;ip_variant_name&gt;_inst_phy.v are tapped:</td>
<td>• The /K/ character transmission continues for at least 1 frame plus 9 octets.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• jesd204_tx_pcs_data[[(L*32)-1:0]</td>
<td>• The sync_n and jesd204_tx_int signals are deasserted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• jesd204_tx_pcs_kchar_data[[(L*4)-1:0]</td>
<td>• On reading status using 'MYKONOS_deframerGetIrq' API, &quot;Not-in-table error&quot;, &quot;Bad Disparity error&quot;, and &quot;Unknown K character error&quot; registers should not be set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The txlink_clk is used as the sampling clock for the Signal Tap.</td>
<td></td>
</tr>
</tbody>
</table>

(1) L is the number of lanes.
<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
|           |           | Each lane is represented by 32-bit data bus in the jesd204_tx_pcs_data signal. The 32-bit data bus is divided into 4 octets. Check the following status and error in the AD9371 register: | • 8b/10b Not-in-Table Error  
• 8b/10b Disparity Error  
• Unknown K character Error |
Initial Frame and Lane Synchronization

Table 2. Initial Frame and Lane Synchronization Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| TX_ILA.1  | Check that the /R/ and /A/ characters are transmitted at the beginning and end of each multiframe. Verify that four multiframe are transmitted in ILAS phase and receiver detects the initial lane alignment sequence correctly. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
  - jesd204_tx_pcs_data[(L*32)-1:0]  
  - jesd204_tx_pcs_kchar_data[(L*4)-1:0]  
The following signals in `<ip_variant_name>_v` are tapped:  
  - sync_n  
  - jesd204_tx_int  
The txlink_clk is used as the sampling clock for the Signal Tap. Each lane is represented by 32-bit data bus in jesd204_tx_pcs_data. The 32-bit data bus for is divided into 4 octets. Check the following status in the AD9371 registers:  
  - Frame Synchronization | The /R/ character or K28.0 (0x1C) is transmitted at the jesd204_tx_pcs_data bus to mark the beginning of multiframe.  
  - The /A/ character or K28.3 (0x7C) is transmitted at the jesd204_tx_pcs_data bus to mark the end of each multiframe.  
  - The sync_n and jesd204_tx_int signals are deasserted.  
  - The jesd204_tx_pcs_kchar_data signal is asserted whenever control characters like /K/, /R/, /Q/, or /A/ are transmitted.  
  - On reading status using `MYKONOS_readDeframerStatus` API, No framing error bits should be set. bits[2:0] if set indicate framing errors. |
| TX_ILA.2  | Check the JESD204B configuration parameters are transmitted in the second multiframe. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
  - jesd204_tx_pcs_data[(L*32)-1:0]  
The following signal in `<ip_variant_name>_v` is tapped:  
  - jesd204_tx_int  
The txlink_clk is used as the sampling clock for the Signal Tap. The Nios® console accesses the following JESD204B CSR registers:  
  - ilas_data1  
  - ilas_data2  
The content of 14 configuration octets in second multiframe is stored in the above 32-bit registers. Check the following status and error in the AD9371 register:  
  - Good Checksum  
  - Configuration Mismatch Error | The /R/ character is followed by /Q/ character or K28.4 (0x9C) in the jesd204_tx_pcs_data at the beginning of second multiframe.  
  - The jesd204_tx_int is deasserted if there is no error.  
  - The JESD204B parameters read from ilas_data1, ilas_data2 registers are the same as the parameters set in the JESD204B IP Core Platform Designer parameter editor.  
  - On reading status using `MYKONOS_jesd204bIlasCheck` API, bit 15 which indicates ILAS configuration mismatch, should not be asserted. |
| TX_ILA.3  | Check the constant pattern of transmitted user data after the end of 4th multiframe. Verify that the receiver successfully enters user data phase. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
  - jesd204_tx_pcs_data[(L*32)-1:0]  
The following signals in `<ip_variant_name>_v` are tapped:  
  - jesd204_tx_int  
The txlink_clk is used as the sampling clock for the Signal Tap. The Nios console accesses the JESD204B CSR register - tx_err. Check the following errors in the AD9371 register:  
  - Lane FIFO pointer delta | When scrambler is turned off, the first user data is transmitted after the last /A/ character, which marks the end of the 4th multiframe transmitted.  
  - Bits 2 and 3 of the JESD204B tx_err register are not set to “1”.  
  - The “Lane FIFO Full” and “Lane FIFO Empty” in the AD9371 registers 0x30C and 0x30D should not be asserted.  
  - The jesd204_tx_int is deasserted if there is no error. |
Transmitter Transport Layer

To verify the data integrity of the payload data stream through the JESD204B transmitter IP core and transport layer and to verify that data from the FPGA digital domain is successfully sent to the DAC analog domain, the FPGA is configured to generate a monotone sine wave. Connect an oscilloscope/spectrum analyzer to observe the waveform/spectrum of a singletone at the DAC analog channels.

The AD9371 upconverts signal to RF frequency. This RF frequency is tunable by the user and specified to AD9371 as LO frequency. Depending on the phase of I and Q streams, the output frequency at DAC analog channels will be LO frequency ± monotone frequency. In our configuration the output frequency will be observed to be LO frequency – monotone frequency.

Figure 7. Data Integrity Check Using Sine Wave

The following figure shows the conceptual test setup for data integrity checking.

![Conceptual test setup](image)

The Signal Tap II Logic Analyzer tool monitors the operation of the transmitter transport layer.

Table 3. Transport Layer Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX_TL.1</td>
<td>Verify the data transfer from digital to analog domain.</td>
<td>Enable sine wave generator in the FPGA and observe the DAC analog channel output on the oscilloscope.</td>
<td>A monotone sine wave is observed on the oscilloscope.</td>
</tr>
</tbody>
</table>

Scrambling

The test setup is similar to test case TX_TL.1 except that the scrambler at the JESD204B transmitter IP core and the descrambler at the DAC JESD core are enabled.

The Signal Tap II Logic Analyzer tool monitors the operation of the transmitter transport layer.

(2) L is the number of lanes.

(3) When scrambler is turned on, your data pattern cannot be recognized after the 4th multiframe in ILAS phase.
Table 4. Scrambler Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX_SCR.1</td>
<td>Verify the data transfer from digital to analog domain.</td>
<td>Enable descrambler at the DAC JESD core and scrambler at the JESD204B transmitter IP core. Enable sine wave generator in the FPGA and observe the DAC analog channel output on the oscilloscope.</td>
<td>A monotone sine wave is observed on the oscilloscope.</td>
</tr>
</tbody>
</table>

JESD204B IP Core and DAC Configurations

The JESD204B IP Core parameters (L, M, and F) in this hardware checkout are natively supported by the AD9371 device's configuration registers. The transceiver data rate, sampling clock frequency, and other JESD204B parameters comply with the AD9371 operating conditions.

The hardware checkout testing implements the JESD204B IP Core with the following parameter configuration.

Table 5. Parameter Configuration

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMF</td>
<td>124</td>
<td>222</td>
<td>421</td>
<td>148</td>
<td>244</td>
<td>442</td>
</tr>
<tr>
<td>HD</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>N'</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>CS</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CF</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Subclass</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Lane Rate (Gbps)</td>
<td>6.144</td>
<td>6.144</td>
<td>3.072</td>
<td>6.144</td>
<td>6.144</td>
<td>6.144</td>
</tr>
<tr>
<td>DAC IQ rate (MSPS)</td>
<td>153.6</td>
<td>307.2</td>
<td>307.2</td>
<td>76.8</td>
<td>153.6</td>
<td>307.2</td>
</tr>
<tr>
<td>AD9371 Device Clock (MHz)</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
</tr>
<tr>
<td>FPGA Device Clock (MHz) (4)</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
</tr>
<tr>
<td>FPGA Management Clock (MHz)</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>FPGA Frame Clock (MHz) (5)</td>
<td>153.6</td>
<td>307.2</td>
<td>76.8</td>
<td>76.8</td>
<td>153.6</td>
<td>153.6</td>
</tr>
<tr>
<td>FPGA Link Clock (MHz) (5)</td>
<td>153.6</td>
<td>153.6</td>
<td>76.8</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
</tr>
</tbody>
</table>

(4) The device clock is used to clock the transceiver.

(5) The frame clock and link clock are derived from the device clock using an internal PLL.
Hardware Checkout Methodology for JESD204B Receiver

The following section describes the test objectives, procedure, and the passing criteria for JESD204B receiver.

The test covers the following areas:
- Receiver data link layer
- Receiver transport layer
- Descrambling
- Deterministic latency (Subclass 1)

**Receiver Data Link Layer**

This test area covers the test cases for code group synchronization (CGS) and initial frame and lane synchronization.

On link start up, the receiver issues a synchronization request and the transmitter transmits /K/ (K28.5) characters. The Signal Tap Logic Analyzer tool monitors the receiver data link layer operation.

---

(6) Sine wave pattern is used in TX_TL.1 and TX_SCR.1 test cases to verify that pattern generated in the FPGA transport layer is transmitted by DAC analog channel.

(7) Single pulse and sinc patterns are used in deterministic latency measurement test cases DL.3 and DL.4 only.
## Code Group Synchronization (CGS)

### Table 6. CGS Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| RX_CGS.1  | Check whether sync request is deasserted after correct reception of four successive /K/ characters. | The following signals in `<ip_variant_name>_<inst_phy>.v` are tapped:  
  - jesd204_rx_pcs_data[(L*32)-1:0]  
  - jesd204_rx_pcs_data_valid[L-1:0]  
  - jesd204_rx_pcs_kchar_data[(L*4)-1:0]  
  The following signals in `<ip_variant_name>.v` are tapped:  
  - rx_dev_sync_n  
  - jesd204_rx_int  
  The rxlink_clk is used as the sampling clock for the Signal Tap.  
  Each lane is represented by 32-bit data bus in jesd204_rx_pcs_data. The 32-bit data bus for is divided into 4 octets. |  
  - /K/ character or K28.5 (0xBC) is observed at each octet of the jesd204_rx_pcs_data bus.  
  - The jesd204_rx_pcs_data_valid signal is asserted to indicate data from the PCS is valid.  
  - The jesd204_rx_pcs_kchar_data signal is asserted whenever control characters like /K/, /R/, /Q/, or /A/ characters are observed.  
  - The rx_dev_sync_n signal is deasserted after correct reception of at least four successive /K/ characters.  
  - The jesd204_rx_int signal is deasserted if there is no error. |
| RX_CGS.2  | Check full CGS at the receiver after correct reception of another four 8B/10B characters. | The following signals in `<ip_variant_name>_<inst_phy>.v` are tapped:  
  - jesd204_rx_pcs_errdetect[(L*4)-1:0]  
  - jesd204_rx_pcs_disperr[(L*4)-1:0]  
  The following signals in `<ip_variant_name>.v` are tapped:  
  - jesd204_rx_int  
  The rxlink_clk is used as the sampling clock for the Signal Tap. |  
  The following signals should not be asserted during CGS phase:  
  - jesd204_rx_pcs_errdetect  
  - jesd204_rx_pcs_disperr  
  - jesd204_rx_int |

(8) L is the number of lanes.
### Initial Frame and Lane Synchronization

#### Table 7. Initial Frame and Lane Synchronization Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| RX_ILA.1  | Check whether the initial frame synchronization state machine enters FS_DATA state upon receiving non /K/ characters. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
jesd204_rx_pcs_data[(L*32)-1:0]  
jesd204_rx_pcs_data_valid[L-1:0]  
jesd204_rx_pcs_kchar_data[(L*4)-1 :0] (9)  
The following signals in `<ip_variant_name>.v` are tapped:  
rx_dev_sync_n  
jesd204_rx_int  
The rxlink_clk is used as the sampling clock for the Signal Tap.  
Each lane is represented by 32-bit data bus in jesd204_rx_pcs_data. The 32-bit data bus for is divided into 4 octets. |  
• /R/ character or K28.0 (0x1C) is observed after /K/ character at the jesd204_rx_pcs_data bus.  
The jesd204_rx_pcs_data_valid signal must be asserted to indicate that data from the PCS is valid.  
The rx_dev_sync_n and jesd204_rx_int signals are deasserted.  
Each multiframe in ILAS phase ends with /A/ character K28.3 (0x7C).  
The jesd204_rx_pcs_kchar_data signal is asserted whenever control characters like /K/, /R/, /Q/, or /A/ are observed. |
| RX_ILA.2  | Check the JESD204B configuration parameters from ADC in second multiframe. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
jesd204_rx_pcs_data[(L*32)-1:0]  
jesd204_rx_pcs_data_valid[L-1:0] (9)  
The following signal in `<ip_variant_name>.v` is tapped:  
jesd204_rx_int  
The rxlink_clk is used as the sampling clock for the Signal Tap.  
The Nios console accesses the following registers:  
ilas_octet0  
ilas_octet1  
ilas_octet2  
ilas_octet3  
The content of 14 configuration octets in second multiframe is stored in these 32-bit registers - ilas_octet0, ilas_octet1, ilas_octet2 and ilas_octet3. |  
• /R/ character is followed by /Q/ character or K28.4 (0x9C) at the beginning of second multiframe.  
The jesd204_rx_int is deasserted if there is no error.  
Octets 0-13 read from these registers match with the JESD204B parameters in each test setup. |
| RX_ILA.3  | Check the lane alignment | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
jesd204_rx_pcs_data[(L*32)-1:0]  
jesd204_rx_pcs_data_valid[L-1:0] (9)  
The following signals in `<ip_variant_name>.v` are tapped:  
rx_somf[3:0]  
dev_lane_aligned  
jesd204_rx_int  
The rxlink_clk is used as the sampling clock for the Signal Tap. |  
• The dev_lane_aligned is asserted upon the last /A/ character of the ILAS is received, which is followed by the first data octet.  
The rx_somf marks the start of multiframe in user data phase.  
The jesd204_rx_int is deasserted if there is no error. |

(9) L is the number of lanes.
**Receiver Transport Layer**

To check the data integrity of the payload data stream through the JESD204B receiver IP Core and transport layer, the ADC is fed with a monotone sine wave test data pattern. The ADC is also set to operate with the same configuration as set in the JESD204B IP Core.

The AD9371 downconverts from RF frequency to monotone frequency. This RF frequency is tunable by the user and specified to AD9371 as LO frequency. Depending on the required phase of I and Q streams, the input frequency at ADC analog channels should be LO frequency ± monotone frequency. In our configuration the input frequency of LO frequency – monotone frequency is used. This is easily available at AD9371 DAC analog output and the same waveform is looped back to ADC through SMA cable.

**Figure 8. Data Integrity Check Using Sine Wave**

The following figure shows the conceptual test setup for data integrity checking.

![Data Integrity Check Using Sine Wave Diagram](image)

**Table 8. Transport Layer Test Cases**

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| RX_TL.1   | Check the transport layer mapping using Sine test pattern. | The following signals in `altera_jesd204_transport_rx_top.sv` are tapped: • `jesd204_rx_data_valid`
The following signals in `jesd204b_ed.sv` are tapped: • `data_error`
• `jesd204_rx_int`
The `rxframe_clk` is used as the sampling clock for the Signal Tap II. | • The `jesd204_rx_data_valid` signal is asserted.
• The `jesd204_rx_int` signals are deasserted.
• Monotone sine wave with frequency same as that of transmitted monotone is observed in Signal Tap II when DAC analog output is looped back to ADC analog input. |

**Descrambling**

The test setup is similar to test case RX_TL.1 except that the descrambler at the JESD204B receiver IP core and the scrambler at the ADC JESD transmitter core are enabled.

The Signal Tap II Logic Analyzer tool monitors the operation of the receiver transport layer.
Table 9. Descrambler Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX_SCR.1</td>
<td>Check the functionality of the descrambler using sine wave test pattern.</td>
<td>Enable scrambler at the ADC and descrambler at the JESD204B receiver IP Core. The signals that are tapped in this test case are similar to test case TL.1</td>
<td>• The jesd204_rx_data_valid signal is asserted. • The jesd204_rx_int signals are deasserted. • Monotone sine wave with frequency same as that of transmitted monotone is observed in Signal Tap II when DAC analog output is looped back to ADC analog input.</td>
</tr>
</tbody>
</table>

JESD204B IP Core and Main ADC Configurations

The JESD204B IP Core parameters (L, M, and F) in this hardware checkout are natively supported by the AD9371 device. The transceiver data rate, sampling clock frequency, and other JESD204B parameters comply with the AD9371 operating conditions.

The hardware checkout testing implements the JESD204B IP Core with the following parameter configuration.

Table 10. Main ADC Parameter Configuration

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMF</td>
<td>124</td>
<td>222</td>
<td>421</td>
<td>148</td>
<td>244</td>
<td>442</td>
</tr>
<tr>
<td>HD</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>N’</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>CS</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CF</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Subclass</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Lane Rate (Gbps)</td>
<td>6.144</td>
<td>3.072</td>
<td>1.536</td>
<td>6.144</td>
<td>6.144</td>
<td>3.072</td>
</tr>
<tr>
<td>ADC IQ rate(MSPS)</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>76.8</td>
<td>153.6</td>
<td>153.6</td>
</tr>
<tr>
<td>AD9371 Device Clock (MHz)</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
</tr>
<tr>
<td>FPGA Device Clock (MHz) (11)</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
<td>153.6</td>
</tr>
</tbody>
</table>

(10) JESD204B Mode with LMF=421 cannot be interoperated with Intel Arria 10 devices because the lane rate supported by Intel Arria 10 devices are 2 Gbps-15 Gbps. Because of limited ADC IQ rate, the mode LMF=421 can only reach 1.536 Gbps in the converter side.

(11) The device clock is used to clock the transceiver.
The figure below shows a block diagram of the deterministic latency test setup. AD9528 clock generator on the EVM provides periodic SYSREF pulses for both the AD9371 and JESD204B IP Core. The period of SYSREF pulses is configured to be an integer multiple of Local Multi Frame Clocks (LMFC). The SYSREF pulse restarts the LMF counter and realigns it to the LMFC boundary.

The link latency for DAC and ADC is measured collectively by performing external loopback at RF level using SMA cable. The time difference between rising edge of pattern transmitted at transmitter transport layer and rising edge of pattern received back at receiver transport layer gives us the link latency. This latency has to remain constant across multiple power cycles of the system.

While performing the loopback delay measurement, the transmitter and receiver are both configured with same JESD204B configurations. The only exception is the JESD204B receiver mode with LMF = 421, which cannot be implemented in Intel Arria 10 FPGA because of unsupported data rate. In this mode, the ADC and FPGA are configured with LMF=222 configuration and the data rate is 3.072 Gbps. The FPGA and DAC JESD transmitter are configured with LMF = 421 configuration and the data rate is 3.072 Gbps. This enables us to perform delay measurement for this mode.

(12) The frame clock and link clock are derived from the device clock using an internal PLL.

(13) Sine wave pattern is used in RX_TL.1 and RX_SCR.1 test cases to verify that pattern generated into ADC analog channel is converted into same pattern in the FPGA transport layer and at same frequency.

(14) Single pulse and sinc pattern are used in deterministic latency measurement test cases DL.3 and DL.4 only.

Deterministic Latency (Subclass 1)
The FPGA can generate a 16-bit digital sample for single pulse or sinc pattern at the transport layer. Either waveform can be used to measure the loopback latency. The transmitted pulse and received pulse are both plotted in Signal Tap Logic Analyzer. The time difference between the 2 pulses gives us the loopback latency which includes both transmitter link latency and receiver link latency.

### Table 11. Deterministic Latency Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL.1</td>
<td>Check the FPGA SYSREF single detection.</td>
<td>Check that the FPGA detects the first rising edge of SYSREF pulse. Read the status of sysref_singledet (bit[2]) identifier in syncn_sysref_ctrl register at address 0x54.</td>
<td>The value of sysref_singledet identifier should be zero.</td>
</tr>
<tr>
<td>DL.2</td>
<td>Check the SYSREF capture.</td>
<td>Check that FPGA and ADC capture SYSREF correctly and restart the LMF counter. Both FPGA and ADC are also repetitively reset. Read the value of rbd_count (bit[10:3]) identifier in rx_status0 register at address 0x80.</td>
<td>If the SYSREF is captured correctly and the LMF counter restarts, for every reset, the rbd_count value should only drift a little due to word alignment.</td>
</tr>
<tr>
<td>DL.3</td>
<td>Measure the total latency.</td>
<td>Measure the time difference between the rising edge of pulses in Signal Tap Logic Analyzer.</td>
<td>The latency should be consistent.</td>
</tr>
<tr>
<td>DL.4</td>
<td>Re-measure the total latency after setup power cycle and FPGA reconfiguration.</td>
<td>Measure the time difference between the rising edge of pulses in Signal Tap Logic Analyzer.</td>
<td>The latency should be consistent.</td>
</tr>
</tbody>
</table>

### Related Links

Test Results on page 22
Test Results

The following table contains the possible results and their definition.

<table>
<thead>
<tr>
<th>Table 12.</th>
<th>Results Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Result</td>
<td>Definition</td>
</tr>
<tr>
<td>PASS</td>
<td>The Device Under Test (DUT) was observed to exhibit conformant behavior.</td>
</tr>
<tr>
<td>PASS with comments</td>
<td>The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.</td>
</tr>
<tr>
<td>FAIL</td>
<td>The DUT was observed to exhibit non-conformant behavior.</td>
</tr>
<tr>
<td>Warning</td>
<td>The DUT was observed to exhibit behavior that is not recommended.</td>
</tr>
<tr>
<td>Refer to comments</td>
<td>From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.</td>
</tr>
</tbody>
</table>

The following table shows the results for test cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, and SCR.1 with different values of L, M, F, K, subclass, data rate, sampling clock, link clock, and SYSREF frequencies.

<table>
<thead>
<tr>
<th>Table 13.</th>
<th>Results Definition for DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>2</td>
</tr>
<tr>
<td>10</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>4</td>
</tr>
<tr>
<td>12</td>
<td>4</td>
</tr>
</tbody>
</table>
**Table 14. Results Definition for Main ADC**

Mode with LMF=421 cannot be implemented in JESD204B IP core in Intel Arria 10 devices. The lane rate supported by Arria 10 devices are 2 Gbps-15 Gbps. But because of limited ADC IQ rate, the mode LMF=421 can only reach 1.536 Gbps in the converter side.

<table>
<thead>
<tr>
<th>Test</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>SCR</th>
<th>K</th>
<th>Lane rate (Gbps)</th>
<th>ADC IQ rate (MSPS)</th>
<th>Link Clock (MHz)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>0</td>
<td>32</td>
<td>6.144</td>
<td>153.6</td>
<td>153.6</td>
<td>Pass</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>32</td>
<td>6.144</td>
<td>153.6</td>
<td>153.6</td>
<td>Pass</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>0</td>
<td>32</td>
<td>3.072</td>
<td>153.6</td>
<td>76.8</td>
<td>Pass</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>3.072</td>
<td>153.6</td>
<td>76.8</td>
<td>Pass</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>4</td>
<td>8</td>
<td>0</td>
<td>32</td>
<td>6.144</td>
<td>76.8</td>
<td>153.6</td>
<td>Pass</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>4</td>
<td>8</td>
<td>1</td>
<td>32</td>
<td>6.144</td>
<td>76.8</td>
<td>153.6</td>
<td>Pass</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>0</td>
<td>32</td>
<td>6.144</td>
<td>153.6</td>
<td>76.8</td>
<td>Pass</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>1</td>
<td>32</td>
<td>6.144</td>
<td>153.6</td>
<td>76.8</td>
<td>Pass</td>
</tr>
<tr>
<td>9</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>0</td>
<td>32</td>
<td>3.072</td>
<td>153.6</td>
<td>7.68</td>
<td>Pass</td>
</tr>
<tr>
<td>10</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>3.072</td>
<td>153.6</td>
<td>7.68</td>
<td>Pass</td>
</tr>
</tbody>
</table>

The following table shows the results for test cases DL.1 and DL.2 with different values of L, M, F, K, subclass, data rate, sampling clock, link clock and SYSREF frequencies.

**Table 15. Results Definition for Deterministic Latency Test**

<table>
<thead>
<tr>
<th>Test</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>Sub-class</th>
<th>SCR</th>
<th>Transmitter Lane rate (Gbps)</th>
<th>Receiver Lane rate (Gbps)</th>
<th>SYSREF pulse frequency (MHz)</th>
<th>Total Latency Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>6.144</td>
<td>6.144</td>
<td>0.48</td>
<td>Pass (1.146 us)</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>6.144</td>
<td>3.072</td>
<td>0.48</td>
<td>Pass (1.328-1.341 us)</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>3.072</td>
<td>0.48</td>
<td>Pass (16) (0.651-0.657 us)</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>4</td>
<td>8</td>
<td>1</td>
<td>1</td>
<td>6.144</td>
<td>6.144</td>
<td>0.48</td>
<td>Pass (2.331 us)</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>6.144</td>
<td>6.144</td>
<td>0.48</td>
<td>Pass (1.133-1.146 us)</td>
</tr>
<tr>
<td>6</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>6.144</td>
<td>3.072</td>
<td>0.48</td>
<td>Pass</td>
</tr>
</tbody>
</table>

(15) The sysref frequency is taken as integer multiple of LMFC period. The value of 0.48MHz is derived as a common integer multiple for all JESD204B modes.

(16) The link latency is measured as the loopback delay of transmitter and receiver datapaths. For more information on how DL validation is performed on mode with LMF=421, refer to the section on deterministic latency.
<table>
<thead>
<tr>
<th>Test</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>Subclass</th>
<th>SCR</th>
<th>K</th>
<th>Transmitter Lane rate (Gbps)</th>
<th>Receiver Lane rate (Gbps)</th>
<th>SYSREF pulse frequency (MHz)</th>
<th>Total Latency Result</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(1.328-1.354 us)</td>
</tr>
</tbody>
</table>

**Figure 10. Oscilloscope plot observed at DAC output.**

The LO frequency is set to 400MHz in AD9371 RF transmitter in this example and a monotone of 7.68MHz is being transmitted from FPGA.

![Oscilloscope plot](image1)

**Figure 11. Spectrum Analyzer plot observed at DAC output.**

The LO frequency is set to 400MHz in AD9371 RF transmitter in this example and a monotone of 7.68MHz is being transmitted from FPGA. The peak is observed at 392.32 MHz (i.e., 400-7.68 MHz).

![Spectrum Analyzer plot](image2)

*The sysref frequency is taken as integer multiple of LMFC period. The value of 0.48MHz is derived as a common integer multiple for all JESD204B modes.*
Figure 12. Transmitted sine wave at input of transmitter transport layer and Received sine wave at output of receiver transport layer observed in Signal Tap II Logic Analyzer for mode LMF=148.

Figure 13. Latency measured between rising edge of transmitted single pulse and rising edge of received single pulse for mode LMF=148.
Latency is observed to be 179 rxframe_clk cycles or 2.331 us.

Figure 14. Latency measured between centre of transmitted sinc pattern and centre of received sinc pattern for mode LMF=148.
Two pulses are sent with 100 rxframe_clk cycles delay. Same delay of 100 clock cycles is observed in received signal.
Test Result Comments

In each test case, both the JESD204B transmitter and JESD204B receiver IP core successfully initialize from CGS phase, ILAS phase, and until user data phase.

The test results for JESD204B transmitter are marked with Pass with comments because the deframer of AD9371 raises IRQ due to ILAS configuration mismatch. The conflicting ILAS parameters are N value and CS value. The AD9371 deframer register contains the following JESD204B parameter values N=14 and CS=2 while FPGA transmits ILAS with following JESD204B parameter N=16 and CS=0. The FPGA is configured with JESD204B parameters as per values defined in AD9371-User-Guide-UG-992 document available at the time of testing (refer Figure 15 on page 26). Otherwise the behavior of the JESD204B transmitter IP core meets the passing criteria.

Figure 15. Snapshot of datasheet describing JESD204B parameters of DAC datapath.

The monotone sine wave from FPGA is transmitted into RF domain successfully at desired frequency and when loopbacked into ADC, the original monotone sine wave is received back.

In the deterministic latency measurement, consistent total latency is observed across the JESD204B transmitter link and JESD204B receiver link.
## Document Revision History for AN 792: Intel FPGA JESD204B IP Core and ADI AD9371 Hardware Checkout Report

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| December 2017 | 2017.12.18 | • Renamed the document as *AN 792: Intel FPGA JESD204B IP Core and ADI AD9371 Hardware Checkout Report*.  
• Added a note to clarify that the IOPLL input reference clock is sourcing from device clock through global clock network in the *Hardware Setup* topic.  
• Updated for latest branding standards.  
• Made editorial updates throughout the document. |
| May 2017    | 2017.05.08 | Initial release. |