With any switch mode power supply, proper layout of the printed circuit board is essential to prevent switching noise generated by the converter from contaminating the rest of the circuit. Switching noise in the form of $\text{di/dt}$, $\text{dv/dt}$, and magnetic coupling can disturb sensitive analog or digital circuitry, especially circuits operating at RF frequencies. A poor layout can even cause the power supply itself to be inoperable.

Since the switching noise is generated primarily by the power stage of the supply, careful layout of the power components should take place before the small signal components are placed and routed. The basic strategy is to minimize the area of the loops created by the power components and their associated traces. In the synchronous buck converter shown below the input (source) loop #1 ideally consists of a DC current with a negligible AC ripple. Loop numbers 2 and 3 are the power switch loops. The current in these loops is composed of trapezoidal pulses with large peaks and fast edges ($\text{di/dt}$ and $\text{dv/dt}$). The area of these loops will be determined primarily by how close together the power components, the inductor, and the capacitors $\text{Cin}$ and $\text{Cout}$ can be placed. The closer the components, the shorter the PCB traces connecting them, and therefore the smaller loop area.

![Figure 1: Synchronous buck converter.](image)

The Enpirion family of modules greatly simplifies the board layout because of the self-contained power switches and inductor. This means that the only external power components that need to be placed are the input and output filter capacitors, and the pinout of the part ensures that the area of the critical current loops is kept to a minimum.

Due to the high frequency of operation of the Enpirion power converters, circuit board layout is important to minimize input/output ripple and noise and radiated EMI. Proper layout requires attention primarily to two areas: (1) maintaining tight, well disciplined ac current loops on the input and output through the respective filter capacitors, and (2) creation of a “quiet” ground for referencing the dc input and output voltages, and properly bypassing of the I/O terminals to the quiet ground.

The first area of consideration requires that the input and output filter capacitors, which conduct sizable ac currents, be situated as close to the converter package as possible. Ideally, the input filter capacitors should connect between the $\text{+Input}$ and the Input Ground leads immediately adjacent to the package. Similarly, output
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Filter capacitors should connect between the +Output and the Output Ground leads where these leads exit the package. These “loops” should lie entirely on the same layer of metal on the PCB as the power converter.

The second area of consideration, a “quiet” ground, is best implemented by creating a ground layer in a multi-layer board. To minimize ac ripple voltage, noise and EMI on the input and output, bypass capacitors may also be placed between the respective input and output terminals and the “quiet” ground using vias as necessary to the GND plane. These vias should be placed as close to the capacitor terminals as possible.

One of the most important performance parameters of a switching regulator is the output voltage ripple. The output voltage ripple has two main components: one at the fundamental switching frequency of the converter, and another caused by the fast switching edges resulting in voltage spikes at hundreds of megahertz. The large output filter capacitors right next to the output pins of the package keep the switching frequency component under control while providing energy storage for reasonable transient response. The larger the number of capacitors, the lower will be the fundamental ripple component. To control the high frequency spikes, additional smaller capacitors are also sometimes needed in parallel to the output filter capacitors. If the load is some distance away from the converter, additional capacitors will be needed at the load to bring down the fundamental and the switching spike components of the ripple. Usually these capacitors are the output terminal bypass capacitors to the quiet ground discussed above. The value and size of the capacitors needed at the load will depend a lot on the board layout and parasitic elements.

Capacitor choice for ripple and noise bypassing between the I/O terminals and the quiet ground should seek to minimize the overall capacitor impedance at the frequencies of interest. Many times different values of bypass capacitors are needed in parallel to bypass multiple ranges of noise frequencies. We recommend only ceramic multi-layer chip capacitors with the C0G (NP0), X7R, or X5R dielectric to be used with the Enpirion regulators. Do not use the Y5V dielectric ceramics. This dielectric can lose a lot of its capacitance with temperature and with applied dc voltage.

*Turn off the Auto-router and Do It Manually*

Ideally, the power supply section of any circuit should be physically isolated from the rest of the circuit. Imagine if you will a small “island” of power supply circuitry that connects to the rest of the circuit through a single “land bridge”. Schematically, the power and ground nets are typically distributed throughout an entire design, including the power section. It is often difficult to prevent layout problems with the power section because the electrical rules check performed by the PCB design software cannot differentiate between the power/ground nets used by the power supply and those used by the rest of the circuitry because they are the same net.

The input and output filter capacitors should be placed on the same side of the PCB as the power IC and right next to the input and output pins of the package. This will ensure that the high frequency current loops are minimized.

Since the power IC has fast switching signals, it is advisable to keep all sensitive signals as far away as possible from the device. The quiet GND plane should be the second layer directly underneath the top layer where the converter and its critical current loops are routed. There should not be any breaks in the GND plane underneath the switching converter. In addition, try not to route any traces on the top layer underneath the device other than ground copper. The copper on the top layer should be as densely filled with thermal vias as possible, and it should have a soldermask opening which matches the thermal pad under the Enpirion device.
Analog vs. Power Ground

The Enpirion POL devices have two grounds: a single quiet AGND pin for the control section, and several PGND connections for the power section. The PGND connections consist of pins on the input side, on the output side, and a thermal pad underneath the package. All these PGND points are connected to each other inside the Enpirion package, and they need to be connected to AGND on the PCB. AGND should go to the quiet ground plane of the PCB, using vias right next to the AGND pin. These vias can also serve as test points in case any signals need to be measured with respect to AGND. Any small-signal component that needs to be connected to AGND pin of the regulator needs only to be connected to the quiet ground plane of the PCB in the vicinity of the Enpirion package.

The input PGND set of pins is very noisy due to high-frequency, trapezoidal AC currents with very fast rise and fall times, and these currents should be kept away from the quiet ground plane of the PCB as much as possible. For this reason, these pins should only go to the input filter capacitors, and no other point. From the input capacitor GND pins there should be a row of vias to the quiet GND plane. These vias will help minimize input voltage ripple spikes. See the figures in the Layout Recommendations section.

The output PGND pins are also quite noisy due to the high-frequency triangular inductor ripple current going through them. There should be a direct connection from these pins to the output capacitors. Similarly to the input capacitors, there should be a row of vias from the output cap ground leads to the quiet GND plane, which will help minimize output voltage ripple. See the figures in the Layout Recommendations section.

The input PGND pins should not be connected to the output PGND pins on the PCB. None of the PGND pins should also be connected to the thermal PGND pad on the PCB. These connections are all made inside the Enpirion module and through the GND plane. The thermal PGND is to be connected to the quiet ground plane through the thermal vias underneath it.

Remote Sensing Capability

Remote sensing gives the system designer the ability to achieve the best possible regulation at the load. In order to avoid any stability problems, the inductance between the last output capacitor and the load should be minimized. This can be achieved by making the positive and ground connections between the converter and the load with very wide copper pours. The connection from the load to the VSENSE pins should also be made as thick as possible. It should also be kept away from any noisy circuits that could contaminate it.

Loop Compensation

The Enpirion devices are all internally compensated to achieve stable operation through all operating conditions. Since the control loop includes the output capacitors and any connections up to and including the load, some applications may require adjustments to the compensation circuit depending on the board layout. For this reason, three pins (COMP, EAIN, and EAOUT) are made available. Most applications will not require adjustments to the compensation. We do, however, recommend adding through-hole test points next to each of these pins. The test points can be used to observe the control loop behavior and perform any optimization of the loop if needed. The signals on these test points should be measured relative to the AGND test points.
Radiated EMI Requirements

One of the most prevalent radiated EMI requirements is the EN55022. Most electronic systems need to pass the level B specification of this requirement. The test is done using a calibrated antenna at 3 or 10 meters away from the equipment. The frequency range of the test is from 30MHz to 1GHz. Following the guidelines mentioned in this app note will help an electronic system consisting of a POL switching regulator meet the radiated EMI specifications. For the Enpirion POL converters, small 0603 or 0805 ceramic capacitors may have to be used in parallel with the larger input filter capacitors between the PVIN and PGND pins of the package. The value of these smaller capacitors in any given application will depend on the board layout in. In order to add further suppression of the switching signals causing the radiated EMI, the smaller capacitors may also be needed as bypass caps at the input terminal of any PCB that has the Enpirion POL converters assembled on it.

Some Notes on the Use of Vias

As the switching frequency of power converters increases, it is necessary to consider skin effect when laying out the power path. High frequency AC currents do not flow through a conductor evenly as does DC current. The depth of penetration of the conductor is a function of the frequency and conductor material. The use of through-hole vias to carry high frequency currents may not give the perceived benefit, and can also cause noise contamination of power planes even though the component placement and layout appear optimized from a DC standpoint. That is why the input and output filter caps should be placed right next to their respective pins on the same side of the PCB. The vias next to the capacitor ground leads should be placed under the capacitors at the edge of the conductor. See the figures in the Layout Recommendations section. Vias can be used for DC currents, but it is important to use enough vias, both to carry the high currents and to provide redundancy to the power connection.

![Skin Depth Diagram]

Figure 2: AC current can only penetrate the conductor to the skin depth, forcing high frequency currents to flow around the edge of the trace instead of through a filled via. This effect causes a longer than expected current path.

In order to determine the skin depth in a PCB trace, use the following calculation:

\[ \Delta = \frac{k}{\sqrt{f}} \]

Where:

- \( k = 6.58 \frac{cm}{\sqrt{Hz}} \) Copper at 20°C
- \( \Delta = \text{skindepth(cm)} \)
- \( f = \text{frequency(Hz)} \)

In a flat copper conductor, the skin depth at 5MHz is 0.029mm at 20°C. A PCB trace made of 1-ounce copper is 0.034mm thick.

Vias are also necessary to carry heat out of the package to other PCB layers where it can be dissipated. As
shown in the next section, an array of vias under the part connects to the quiet ground plane. The size of the vias should be ≤ 0.3mm.

Layout Recommendations

The recommendations shown in this section are for the Enpirion DFN, laminate package, POL converters. These products consist of the EN5310, EN5330, and EN5360. Since all these packages are very similar to each other, the layout guidelines below can be applied to all of them. The recommendations only show the critical input and output filter capacitors. The table below shows the values of these capacitors for the three POL products:

<table>
<thead>
<tr>
<th>Product</th>
<th>Input Capacitor</th>
<th>Output Capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Total Capacitance</td>
<td>Minimum Footprint</td>
</tr>
<tr>
<td>EN5310</td>
<td>10µF, 10V</td>
<td>1x10µF, 1206</td>
</tr>
<tr>
<td>EN5330</td>
<td>22µF, 10V</td>
<td>1x22µF, 1210</td>
</tr>
<tr>
<td>EN5360</td>
<td>~44µF, 10V</td>
<td>1x47µF, 1210</td>
</tr>
</tbody>
</table>

Table 1: Input and output capacitor configuration for the Enpirion DFN POL switching regulators

In the layout recommendations below, the Vin and Vout connections go to the respective power planes and the input and output ground connections go to the system ground plane. The system components then pick up their inputs from the output power plane and the ground plane. The drawings are not to scale; the recommendations therefore present a relative comparison among different options.

Use of Thermal Vias

The center ground pad of the device is used as a thermal connection to remove heat from the die into system ground plane. The number of vias under the package should be maximized, and each should be ≤ 0.3mm. The soldermask opening needs to be the same size as the exposed pad, and additional vias can then be used around the pad to decrease the thermal resistance of the connection. For best thermal performance, in addition to the GND plane, the maximum amount of copper should be connected to the thermal vias on any other layer with available space. There should be no thermal relief or thermal spokes when connecting the thermal vias to the copper on any layer.
Minimum Footprint Layout

Figure 3: This layout contains the minimum number of input and output capacitors required for basic operation, and it is recommended when space is at a premium. Vout ripple will be higher with this layout. Some smaller filter capacitors should be used at the load to further reduce the ripple.

Optimum Performance Layout

Figure 4: This layout results in the lowest output ripple; however, it takes up the most footprint on the PCB. For the EN5310, assume only one input capacitor and two output capacitors.
**Vertical Output Capacitor Placement**

Through hole test points are recommended for pins 1, 4, 5 and AGND for troubleshooting purposes.

Connect to system ground plane using the center thermal pad, using as many vias as possible for optimum heatsinking.

- Vias from output cap to GND
- Vias from input power plane
- Vias to the output power plane
- Vias from input cap to GND

Figure 5: This layout still employs 5 output capacitors, but arranged to use the PCB footprint in a different way. The parasitic inductance in the output is slightly higher than the previous layout with 5 output capacitors.

Next page shows a specific example of a minimum footprint layout for the EN5310 & EN5330, and one for the EN5360. These examples show only the input and output caps and critical traces. Soft-start, VSENSE, ENABLE, Vout-programming, and other small-signal traces would need to be added to these layouts.
Figure 6: EN5310 and EN5330 power path layout (minimum footprint)

- Extend copper to the right & above thermal pad beyond the soldermask opening to get as many thermal vias to the GND plane as possible.
- Vias from AGND to GND plane. Can also serve as test points for AGND.
- Fill area under the thermal pad with as many small (<0.3mm) vias to the GND plane as possible.

- Note vias to the GND plane.

Figure 7: EN5360 power path layout (minimum footprint)

- Extend copper to the right & above thermal pad beyond the soldermask opening to get as many thermal vias to the GND plane as possible.
- Vias from AGND to GND plane. Can also serve as test points for AGND.
- Fill the area under the thermal pad with as many small (<0.3mm) vias to the GND plane as possible.

- Note vias to the GND plane.
Notes on Laying Out Multiple Converters

When laying out multiple converters in close proximity to each other, care must be taken to avoid crosstalk between the converters. Crosstalk between multiple converters operating at slightly different switching frequencies will result in low frequency noise appearing on the output, effectively increasing the output voltage ripple amplitude.

In order to isolate the converters from each other, it is necessary to separate the input voltage connections going to each converter. If possible, connect them together in a star configuration right at the point where the input comes into the circuit. It is also helpful to bypass to ground the high frequency noise generated by the switching converters using one or more high quality ceramic capacitors from Vin to AGND at the star connection point. A 1µF, 0603, X7R capacitor has a resonant frequency close to the 5MHz switching frequency of the EN53X0 series converters, and thus provides optimum bypassing. The ground connection at the star point is considered a quiet GND point because it is removed from the switching grounds of the converters’ input filter capacitors. All the high-frequency AC current is ideally in the input PGND copper of each converter, and only the dc current flows through to the quiet GND.

In applications where the board layout constraints do not allow the star connection of the input traces to the multiple converters, small chip input LC filters may be used at the input circuit of each converter.

Another point to consider when using multiple devices on a board is to minimize the crosstalk between the input circuit of one converter and the output circuit of another one. The best way to accomplish this task is to keep the input circuit of any device away from the output circuit of any other converter.
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