The EN5365 and the EN5366 are both 6 A voltage mode synchronous buck converters operating at a fixed frequency of 5 MHz with an internal inductor. The EN5365 offers 3-pin VID codes to set the output voltage to any of the 7 pre-programmed voltages, while the EN5366 offers an adjustable output voltage to be set by an external resistor divider. Both devices have a built-in paralleling feature that allows 2 to 4 converters to be paralleled together to increase load current capability to 12 to 24 A. This application note details the circuit operation, component selection, performance characteristics and layout considerations to facilitate the design process.

Figure 1. EN5365 Paralleling Circuit

**Circuit Operation**

Two typical application circuits are shown in Figures 1 and 2 for paralleling two EN5365 and EN5366 devices to deliver 12 A current. The M/S pin of each device declares which device is Master and which is Slave. Master is the converter with the M/S pin pulled low. Master provides the gate driver output to Slave and synchronizes the turn-on and turn-off of the internal P-channel and N-channel MOSFETs in both devices. Master also sets the output voltage through its VID codes (with the EN5365) or its external resistor divider (with the EN5366), the soft-start ramp through its soft-start capacitor and provides the POK signal output. Slave provides the power stage and follows Master. Many internal control functions in Slave are disabled. As a result, it is recommended to ground the VS0, VS1, VS2 and VSENSE pins and to leave the SS and POK pins open in the EN5365 Slave. Likewise, it is recommended that the XFB be grounded and the XOV, SS and POK pins be left open.

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in the EN5366 Slave. A 1 Ω resistor is added between PVIN and AVIN to provide additional filtering on chip supply for stable operation. Please refer to the EN5365 and EN5366 datasheets for details on each converter and device operation.

![EN5366 Paralleling Circuit Diagram](image)

Figure 2. EN5366 Paralleling Circuit

**Component Selection**

**Input and Output Capacitors**

The power stage for both Master and Slave needs to be identical. Two 22 µF, 10 V, X5R or X7R ceramic capacitors in 1206 or 1210 packages are recommended on each converter’s input in order to provide sufficient ripple current capability and capacitance on the input. Each converter’s output can have five 10 µF, 10 V, X5R or X7R ceramic capacitors in a 1206 package for excellent ripple performance or a single 47 µF, 10 V, X5R or X7R ceramic capacitor for minimal footprint.

**Soft-Start Capacitor**

Only one soft-start capacitor on Master is needed to control the soft-start ramp. This capacitor begins to charge when ENAB LE and AVIN cross their turn-on thresholds. The typical soft-start time for the output to reach regulation voltage from when CSS begins to charge is given by:

\[ t_{SS} = C_{SS} \times 0.075 \]
Where the soft-start time $t_{SS}$ is in ms and the soft-start capacitance $C_{SS}$ is in nF. Typically, a capacitor around 15 nF is recommended.

**VID code setting for EN5365 Paralleling Circuit**

3 VID codes VS2, VS1 and VS0 allows the user to obtain one of the 7 pre-programmed output voltages. A logic low can be obtained by pulling the pin low such as to ground. A logic high can be obtained by simply leaving the pin open, as there is an internal pull-up on these three pins. The following table shows a matrix of these pre-programmed voltages.

<table>
<thead>
<tr>
<th>VS2</th>
<th>VS1</th>
<th>VS0</th>
<th>Output Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>3.3V</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>2.5V</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>1.8V</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>1.5V</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>1.25V</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>1.2V</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>0.8V</td>
</tr>
</tbody>
</table>

**Resistor Dividers for EN5366 Paralleling Circuit**

Resistor dividers are only needed on Master, as stated earlier. If the over-voltage threshold desired is 120% of the regulation output voltage, then the XOV pin of Master can be simply connected to the XFB pin of Master. Therefore only one resistor divider will be needed. Use a 2 kΩ resistor for the bottom of the divider. Then the top resistor $R_{XFB,M}$ in kΩ can be calculated by:

$$R_{XFB-M} = \frac{V_{OUT} - 0.75}{0.375}$$

Where $V_{OUT}$ is the output voltage in V. If the over-voltage threshold $V_{OVTH}$ in V needs to be different from 120% of the regulation output voltage, then the top resistor $R_{XOV,M}$ in kΩ can be calculated by:

$$R_{XOV-M} = \frac{V_{OVTH} - 0.9}{0.45}$$

1% or better resistors are typically recommended for these resistor dividers.

**Typical Performance Characteristics**

Circuit of Figure 1, $V_{IN} = 5$ V, $V_{OUT} = 1.2$ V and $T_A = 25$ °C, unless otherwise noted.

Note: Master/Slave current mismatch ratio is defined as \(\frac{|I_{MASTER} - I_{SLAVE}|}{0.5 \times I_{LOAD}} \times 100\%\). $X_{XX-M}$ and $X_{XX-S}$ represent the respective Master and Slave voltage or current.
Paralleling Circuit Design

Efficiency vs. Load Current (Vin = 5 V)

From Top: V_{OUT} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2V, 0.8V

Efficiency vs. Load Current (Vin = 3.3 V)

From Top: V_{OUT} = 2.5 V, 1.8 V, 1.5 V, 1.2V, 0.8V

Master/Slave Current Sharing over Load

Top: Slave, Bottom: Master

Master/Slave Current Sharing over Line at 6 A Load

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Steady-State Operation at No Load
CH1: V_{DRAIN-M}, CH2: V_{DRAIN-S}, CH3: V_{OUT-M}

Steady-State Operation at 12 A Load
CH1: V_{DRAIN-M}, CH2: V_{DRAIN-S}, CH3: V_{OUT-M}

Transient Response at \( V_{IN} = 5 \) V (0-12 A Load Step)
CH1: V_{OUT-M}, CH3: I_{LOAD}, CH4: I_{OUT-M}

Transient Response at \( V_{IN} = 3.3 \) V (0-12 A Load Step)
CH1: V_{OUT-M}, CH3: I_{LOAD}, CH4: I_{OUT-M}

Power-Up/Down at No Load
CH1: ENABLE, CH2: V_{OUT}, CH3: POK, CH4: I_{INDUCTOR-M}

Power-Up/Down at 0.1 \( \Omega \) Load
CH1: ENABLE, CH2: V_{OUT}, CH3: POK, CH4: I_{INDUCTOR-M}
### Layout Considerations

For best current sharing and EMI performance, special attention needs to be paid in laying out two or more converters:

1. All Master and Slave should have identical placement with the same values and numbers of input and output capacitors. The input, input GND, output, and output GND of Master and Slave should be connected together via PCB traces of identical width and length before connected to the system input and output. The output and output GND connection is especially critical and will affect current sharing to a great extent. The maximum resistance difference in PCB traces between the outputs should be less than 10 mΩ. The maximum difference of the input voltage between any 2 devices should be less than 50 mV.
2. All Master and Slave devices should have their ENABLE pins tied together and should be operated simultaneously with a fast rising edge of 10 \( \mu \text{s} \) or less, to ensure that devices start up at the same time. Startup imbalance could lead to OCP condition on the first device to start up.

3. The PWM pin from the Master device is connected to all Slave device PWM pins. Use short and wide traces to make connections and avoid routing these traces around noisy nodes in the circuit.

4. Each individual converter layout should follow the layout guidelines stated in the EN5365 and EN5366 datasheets.

Conclusions

Both the EN5365 and EN5366 work well in paralleling circuits to deliver greater load current. Current sharing is excellent, typically within 2 %. Stable operation with internal compensation and minimal component count offers most compact solutions for higher current applications.

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