Creating an FPGA Power Tree

An FPGA power tree is a graphical representation of your system’s power management architecture. The power tree illustrates the main supply power flow through a tree of power converters that convert the main supply power to the voltage and current required to drive various loads. Every FPGA design has unique power consumption requirements requiring a unique power tree. This application note outlines the creation of an FPGA power tree optimized for your FPGA design.

Your FPGA has several inputs requiring power for the FPGA to operate. These inputs supply power to various resource blocks within the FPGA, including logic, RAM, digital signal processing (DSP), phase-locked loops (PLLs), clocks, I/Os, and transceivers. These resource blocks have static and dynamic power requirements that vary by your selected FPGA and utilization. Your selected FPGA does not have a fixed power requirement; your total power consumption, and your FPGA power tree, depends on your design.

Related Information
Power Management Resource Center
Powering FPGAs Resource Center

Obtaining Power Requirements with the PowerPlay Early Power Estimator

Your FPGA’s power consumption is determined by the implementation of your FPGA design; design components such as logic requirements, the quantity and type of I/Os, the quantity and speed of transceivers, and the use of other FPGA features contribute to your FPGA’s power consumption. You must understand your FPGA power requirements to create an FPGA power tree.

You can calculate your FPGA power requirements with the Microsoft Excel-based PowerPlay Early Power Estimator (EPE) spreadsheet. You can use the PowerPlay EPE spreadsheet to estimate power consumption at any point in your design cycle, including before you have begun your design, or before your design is complete. The PowerPlay EPE spreadsheet allows you to submit estimates of how you will utilize the various resource blocks in your FPGA; once you enter your estimates, the PowerPlay EPE spreadsheet automatically estimates the required power consumption. For detailed information on using the PowerPlay EPE spreadsheet, please see the PowerPlay Early Power Estimator User Guide.

Altera® recommends switching from the PowerPlay EPE spreadsheet to the PowerPlay Power Analyzer in the Quartus® II software once your design is available. The PowerPlay Power Analyzer can access the implemented design details to produce more accurate results. For detailed information on using the PowerPlay Power Analyzer, please see PowerPlay Power Analysis in the Quartus II Handbook.

Related Information
• Altera’s Power Tree Grouping and Converter Selection Tools on page 8
Determining the Power Tree Input Supply Voltage

You must determine the input supply voltage prior to creating your FPGA power tree. Systems typically favor one of two implementations: a 12V input source, or a low voltage (5V or 3.3V) input source.

Most FPGA inputs require a voltage of ≤3.3V. Building an FPGA power tree from a low voltage input source often allows for a smaller, more efficient system. If you use an input source of 12V or higher, or if the PowerPlay Early Power Estimator (EPE) spreadsheet estimates the total FPGA current consumption is very high, Altera recommends that you use a two-stage voltage solution, where:

- A first-stage power converter converts a high voltage to a lower intermediate voltage, and
- A second-stage power converter converts the intermediate voltage to the final FPGA input voltages

**Figure 1: Two-Stage FPGA Power Tree**

This two-stage FPGA power tree voltage solution allows you to power the FPGA inputs with efficient, low-voltage converters. The figure illustrates a 12V power converter converting the input supply to a lower 5V or 3.3V intermediate voltage. The point of load (POL) low-voltage converter then converts the intermediate voltage to the final FPGA input voltages, usually between 0.85V and 3.3V.

The input supply voltage and voltage architecture must be determined before you select power converters.

**Related Information**

[Selecting Power Converters](#) on page 7

**Extracting Power Rails**

The next step in creating an FPGA power tree is extracting what power rails are required for your design; your power tree only needs to supply power to the utilized power rails. It is unlikely that all of your FPGA resource blocks are in use, even in a heavily loaded design.
The **Report** tab in the PowerPlay Early Power Estimator (EPE) spreadsheet details the expected voltage and current requirements for each FPGA power rail based on your design. The PowerPlay EPE spreadsheet indicates which FPGA power rails require a power supply in two ways:

1. The FPGA input line has a non-zero value in the “Total Current (A)” column.
2. For PowerPlay EPE spreadsheet versions 13.1 and later, the FPGA input line has an assigned (not grey) entry in the “Power Regulator Settings Regulator Group” column adjacent to the “Total Current (A)” column.

**Figure 2: I\textsubscript{CCIO} Section Call Out from the PowerPlay EPE Spreadsheet Report Tab**

This figure illustrates the **Report** tab of the PowerPlay EPE spreadsheet highlighting utilized inputs. Some inputs, such as FPGA I/O (I\textsubscript{CCIO}), are generic inputs that may have a total current value that is the sum of the currents required for various I/O inputs at different voltage levels. In this case, the sum of the total current is physically implemented as multiple inputs at their respective I/O voltage levels. As illustrated, the main I\textsubscript{CCIO} line is a summary of the total current needed for I/O inputs, while the individual I\textsubscript{CCxx} rows indicate the various I/O input currents at each voltage level. In this example, you must use different power rail groupings for the I\textsubscript{CCIO} (1.8V) and I\textsubscript{CCIO} (2.5V) power rails.

<table>
<thead>
<tr>
<th>Power Supply Voltage</th>
<th>Min Current Requirement (A)</th>
<th>Static Current (A)</th>
<th>Dynamic Current (A)</th>
<th>Total Current (A)</th>
<th>Power Supply Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>I\textsubscript{CCIO} (0.85V)</td>
<td>0.222</td>
<td>0.004</td>
<td>0.023</td>
<td>0.027</td>
<td>1</td>
</tr>
<tr>
<td>I\textsubscript{CCIO} (0.85V)</td>
<td>0.201</td>
<td>0.003</td>
<td>0.019</td>
<td>0.022</td>
<td>1</td>
</tr>
<tr>
<td>I\textsubscript{CCIO} (1.5V)</td>
<td>0.193</td>
<td>0.003</td>
<td>0.017</td>
<td>0.020</td>
<td>1</td>
</tr>
<tr>
<td>I\textsubscript{CCIO} (1.8V)</td>
<td>0.186</td>
<td>0.003</td>
<td>0.016</td>
<td>0.019</td>
<td>1</td>
</tr>
<tr>
<td>I\textsubscript{CCIO} (2.5V)</td>
<td>0.179</td>
<td>0.002</td>
<td>0.014</td>
<td>0.016</td>
<td>1</td>
</tr>
<tr>
<td>I\textsubscript{CCIO} (3.3V)</td>
<td>0.172</td>
<td>0.002</td>
<td>0.012</td>
<td>0.014</td>
<td>1</td>
</tr>
</tbody>
</table>

You must identify the power rails requiring power in your design prior to grouping the power rails together.

**Related Information**

- [Grouping Power Rail Inputs](#) on page 4
Grouping Power Rail Inputs

Altera FPGAs have several inputs requiring power, but each input does not necessarily require a dedicated power converter. Multiple inputs can be grouped together with a single regulator supplying the sum total of the power; grouping these inputs can reduce the utilized space on your PCB and reduce your system costs. When creating your FPGA power tree, you should group all relevant extracted FPGA power rails for use with a single regulator.

Refer to the Pin Connection Guidelines for your selected Altera FPGA to determine what inputs can be grouped together; the Pin Connection Guidelines recommend a power supply block architecture for each FPGA configuration and provide details about each input pin required during hardware design.

Figure 3: Example Power Supply Block Diagram for Stratix V Transceivers with Data Rates Between 6.5Gbps and 12.5Gbps

This figure illustrates a recommended Stratix V GX power tree, as shown in the Stratix® V E, GS, and GX Device Family Pin Connection Guidelines.

![Power Supply Block Diagram](image)

Notes:
1. When using a switcher to supply these voltages, the switcher must be a low-noise switcher as defined in Note 7.
2. For -1 or -2 speed grade devices, set this power supply to 0.9 V. Refer to the Stratix V data sheet for other speed grade options.
3. Although VCCR_GXB and VCCT_GXB may share a regulator, for better performance these power supplies should be isolated from each other with at least 60 dB of isolation for 1 MHz to 100 MHz bandwidth.

Altera suggests power rail groupings in the Pin Connection Guidelines for each Altera FPGA, but there are two other factors to consider when grouping your power rails. First, each of the FPGA power rail inputs in a group must have the same supply voltage requirement. This limitation is important for FPGA resource blocks such as I/O inputs that might require different voltages depending on the specific interface protocols utilized in your design. For example, a PCI Express® (PCIe®) I/O interface might require a 3V input supply and an LVDS I/O interface might require a 2.5V input supply; while both are I/O inputs, and the Pin Connection Guidelines simplified the I/O inputs as a single VCCIO rail, these two I/O inputs must be powered by different converters.

The second power rail grouping factor to consider is power-up sequencing. Not every FPGA or system requires power-up sequencing, but many advanced FPGAs require that power is supplied to various inputs in a specific order during system power-up. You can locate the power-up sequence guidelines for
your selected Altera FPGA in the device’s Pin Connection Guidelines or Handbook. If your design requires power-up sequencing, you must ensure that grouped power rail inputs meet the sequence requirements for your Altera FPGA. A power rail cannot be powered if it depends upon another rail in the same group or a rail in a later group.

Any inputs in your design can be powered individually, or can be powered in combination with another group of FPGA inputs that share their voltage and sequencing requirements.

**Figure 4: Power-Up Sequence Requirement for Stratix V Devices**

This figure illustrates power-up sequence requirements for the Stratix V device as described in Power Management in Stratix V Devices from the Stratix V Device Handbook.

Once you have determined your power rail input groupings, you can use the PowerPlay Early Power Estimator (EPE) spreadsheet to determine the total power required for the input group. The PowerPlay EPE spreadsheet combines the current requirements for each load by summing each FPGA input’s...
current requirement, as shown in the “Total Current (A)” column in the PowerPlay EPE spreadsheet **Report** tab. The PowerPlay EPE spreadsheet automatically sums the current requirements of the input power rail group and displays a summary on the **Main** spreadsheet tab. The shared input voltage and summed current of the power rail group determines the total power required for the group.

**Figure 5: Power Rail Groupings in the PowerPlay EPE**

You can use the PowerPlay EPE spreadsheet to group inputs at any point in your design cycle, including before you have begun your design, or before your design is complete.

To create a power tree block diagram, use the online, cloud-based PowerPlay Power Tree Designer.

**Related Information**

- Extracting Power Rails on page 2
- FPGA Pin Connection Guidelines
- PowerPlay Early Power Estimators (EPE) and Power Analyzer Download Web Page
- PowerPlay Early Power Estimator User Guide
- PowerPlay Power Tree Designer
Selecting Power Converters

After determining your FPGA power tree architecture and power requirements, you must select your power converters; every FPGA power rail input group requires a power converter. The converters must meet the minimum electrical requirements for input voltage, output voltage, and output load current.

Once you determine what converters meet the minimum electrical requirements, you must prioritize your system requirements, including size, efficiency, switching frequency, power supply noise, and cost. Optimizing some parameters or resources may degrade the performance of others. For example, increasing the switching frequency allows for a smaller system size with lower switching noise in critical frequency bands, but higher switching frequency requires more DC-DC switching and reduces efficiency by generating more switching loss. The Altera Enpirion® power solutions use special design techniques and laterally diffused metal oxide semiconductor technology to reduce loss at high switching frequencies to minimize this trade-off.

Figure 6: Equations Relating Switching Frequency, Inductance, Capacitance, and Switch Loss

These four equations can help you prioritize your system requirements. Equation a describes how inductance gets smaller with higher switching frequencies. Lower inductance enables the use of smaller, more efficient inductors. Equations b and c illustrate that input and output capacitance are smaller with higher switching frequency. Lower capacitance generally enables the use of smaller, cheaper capacitors. Equation d represents power loss, or a combination of conduction losses and switching losses. Power loss, even at high switching frequencies, can be minimized by Altera Enpirion devices designed to minimize $C_{ISS}$ and $C_{OSS}$.

\[
\begin{align*}
\text{a. } L &= \frac{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta I_{OUT} F_{SWITCH}} \\
\text{b. } C_{IN} &= \frac{D(1-D)}{\Delta V_{IN} F_{SWITCH}} \\
\text{c. } C_{OUT} &= \frac{\Delta I_{OUT}}{\Delta V_{OUT} F_{SWITCH}} \\
\text{d. } P_{LOSS} &= \frac{F_{SWITCH}}{R_{ON}} + C_{ISS} V_{GS} F_{SW} + C_{OSS} V_{DS} F_{SW} \\
& \text{Conduction Losses} \\
& \text{Switching Losses}
\end{align*}
\]

Where:
- $F_{SWITCH}$ is the switching converter switching frequency
- $\Delta I_{OUT}$ is the change in current (ripple)
- D is the switching converter duty cycle
- $R_{ON}$ is the MOSFET on resistance
- $C_{ISS}$ is the MOSFET equivalent input capacitance
- $C_{OSS}$ is the MOSFET equivalent input capacitance

System priorities also vary depending upon the load. For example, the FPGA core power rail input ($V_{CC}$) requires high power supply accuracy and low ripple to meet tight tolerance specifications, while power supply noise is a key parameter for sensitive power rails (such as transceiver voltage rails) to minimize both jitter and the bit error rate (BER).

Some power management decisions impact designs at the system level and must be considered early in the design process for successful implementation in the final system design. Some components support more advanced system power management and FPGA power reduction techniques; these components typically require special interfaces and feature sets that you should specify early in the FPGA design process. For
example, you can include Enpirion power solutions that support SmartVID in Arria® 10 device designs, or use Enpirion digital controllers and PowerSoCs with a PMBus interface to implement system telemetry.

Related Information
- Altera's Power Tree Grouping and Converter Selection Tools on page 8
- Powering FPGA Resource Center

Altera's Power Tree Grouping and Converter Selection Tools

Altera offers two tools to simplify the FPGA power tree generation process: the PowerPlay Early Power Estimator (EPE) and the PowerPlay Power Tree Designer.

PowerPlay Early Power Estimator

Power converter groupings and recommendations have been added to PowerPlay Early Power Estimator (EPE) versions 13.1 and later. The PowerPlay EPE tool automatically and seamlessly groups relevant FPGA power rails according to the recommendations in your selected Altera FPGA’s Pin Connection Guidelines. Based on the resulting current requirements, the PowerPlay EPE recommends Enpirion power solutions that best meet your requirements. You can find you recommended power solution in the Enpirion tab of the PowerPlay EPE spreadsheet.

You can use the Report tab of the PowerPlay EPE spreadsheet to manually adjust groupings based on your design. Modifications can include: using I/O protocols at different voltages; separating sensitive rails; and implementing sequencing.

You can use the Enpirion tab to adjust the power solution recommendations based on your design priorities. Modifications can include: selecting rails to choose a low-dropout (LDO) regulator for lower noise or lower cost; and selecting devices with a “Power Good” (POK) flag for sequencing or other fault monitoring.
Figure 7: The Enpirion Tab in the PowerPlay EPE Spreadsheet

The online cloud-based PowerPlay Power Tree Designer provides advanced power tree and system power tree block diagram design. You can upload your PowerPlay EPE spreadsheet to the PowerPlay Power Tree Designer to generate a power tree architecture based on your design features and power requirements, and you can customize each power converter based on your design priorities and parameters. The PowerPlay Power Tree Designer allows you to add more system components to your design, such as additional FPGAs and generic loads. This allows you to specify additional power converters needed to supply other system components and generate a single system power tree.

You can use the PowerPlay Power Tree Designer to save and share designs online, download your design’s bill of materials and netlist, check stock availability, and order components from distributors.

Related Information

- FPGA Pin Connection Guidelines
- PowerPlay Early Power Estimator User Guide
- PowerPlay Early Power Estimators (EPE) and Power Analyzer Download Web Page

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## Document Revision History

### Table 1: Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
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</thead>
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<tr>
<td>October 2014</td>
<td>Initial release.</td>
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Altera Corporation