1. Introduction

This document provides design guidelines specific to Intel® Stratix® 10 I/O Limited (IOL) FPGAs designated by ordering part numbers (OPN) ending with -NL. I/O Limited FPGAs limit transceiver utilization such that the one-way aggregate bandwidth is ≤499 Gbps and GPIO utilization to ≤700 I/O pins.

Customers may find these devices useful where export restrictions constrain the usage of FPGAs with transceiver and I/O utilization above those limits. Unless otherwise specified, Intel Stratix 10 I/O Limited FPGAs behave identically to standard Intel Stratix 10 FPGAs.

This document is based on Intel Quartus® Prime software version 21.1.
2. Overview

Intel Stratix 10 I/O Limited (IOL) FPGAs are designated with ordering part numbers (OPN) that end with an -NL suffix.

The Intel Quartus Prime software has restrictions on Intel Stratix 10 IOL FPGAs to limit GPIO, LVDS, and transceiver utilization.

The following table shows feature support for Intel Stratix 10 IOL FPGAs and Intel Stratix 10 standard OPN FPGAs.

### Table 1. Intel Stratix 10 I/O Limited Device and Intel Stratix 10 Standard Device Feature Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>Parameter</th>
<th>Standard Device</th>
<th>I/O Limited Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration</td>
<td>Scheme</td>
<td>Support all schemes with no functionality or performance difference.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Programming file compatibility</td>
<td>(1)</td>
<td>(1)</td>
</tr>
<tr>
<td>GPIO and LVDS</td>
<td>Maximum I/O pin count utilization (2) (3)</td>
<td>&gt;700 pins (4)</td>
<td>≤700 pins</td>
</tr>
<tr>
<td>Transceiver</td>
<td>Maximum bandwidth utilization (5)</td>
<td>&gt;499 Gbps</td>
<td>≤499 Gbps</td>
</tr>
<tr>
<td>Dynamic reconfiguration</td>
<td></td>
<td>Yes</td>
<td>Yes (6)</td>
</tr>
</tbody>
</table>

**Note:**
1. Refer to the Device Configuration Guidelines topic for details.
2. GPIO and LVDS pin counts are limited to 700 pins by the Intel Quartus Prime software IOL restriction. LVDS pin count is 2 pins per pair.
3. The I/O pin count includes general purpose I/O, LVDS I/O, and high voltage I/O.
4. Maximum I/O pin count availability depends on device package selection.
5. For details of the Intel Quartus Prime software bandwidth calculation, refer to the Transceiver Bandwidth Calculation topic.
6. Enabling Dynamic Reconfiguration reduces transceiver maximum bandwidth per Intel Quartus Prime software IOL restrictions. Refer to the Dynamic Reconfiguration Status section in the Transceiver Bandwidth Calculation topic for more information.

2.1. Available Device Options and Ordering Part Numbers

This topic illustrates the mapping between available device options and their corresponding ordering codes, and shows the comparison between I/O Limited (IOL) and standard ordering codes.
2. Overview
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Figure 1. Sample Ordering Code and Available Options for Intel Stratix 10 FPGAs with Optional NL Suffix

Packet Code
- T: FineLine BGA (FBGA), 1.0 mm pitch
- H: 24
- J: 32
- N: 48

Transceiver Count
- F: H-Tile
- E: E-Tile + H-Tile
- P: P-Tile + E-Tile

Sip Code
- L: L-Tile
- H: H-Tile
- N: 48

Family Signature
- 1S: Stratix 10
- 1G: GX variant
  - 26.6 Gbps transceivers (NRZ)
  - 28.3 Gbps transceivers (NRZ)
  - 58.3 Gbps transceivers (PAM4)
- 1D: DX variant
  - 16 Gbps transceivers (NRZ - PCIe only)
  - 28.3 Gbps transceivers (NRZ)
  - 56 Gbps transceivers (PAM4)

Logic Density
- 040: 400K logic elements
- 065: 650K logic elements
- 110: 1,100K logic elements
- 166: 1,660K logic elements
- 280: 2,800K logic elements

Transceiver Speed Grade
- 2: L-Tile: 26.6 Gbps NRZ
- H-Tile: 26.6 Gbps NRZ
- E-Tile: 28.3 Gbps NRZ & 56 Gbps PAM4
- P-Tile: 16 Gbps NRZ

Operating Temperature
- I: Industrial (Tj = -40°C to 100°C)
- E: Extended (Tj = 0°C to 100°C)

Power Option
- V: SmartVID standard power
- L: Low Power (Fixed Voltage)

Optional Suffix
- G: RoHS
- NL: IOL FPGA

Package Code
- 35: 1,152 pins, 35 mm x 25 mm
- 43: 1,760 pins, 42.5 mm x 42.5 mm

Note:
1. Lead-free RoHS6 devices use SAC405 solder balls, 95.5% Tin, 4.0% Silver, and 0.5% Copper.
The following table shows the Intel Stratix 10 IOL FPGA ordering part numbers (OPN) and the equivalent Intel Stratix 10 standard device OPN. For information on ordering devices not listed in this table, contact your Intel representative.

<table>
<thead>
<tr>
<th>Variant</th>
<th>Standard FPGA OPN</th>
<th>I/O Limited FPGA OPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>GX</td>
<td>1SG040HH2F35I2VG</td>
<td>1SG040HH2F35I2VGNL</td>
</tr>
<tr>
<td></td>
<td>1SG065HH2F35I2LG</td>
<td>1SG065HH2F35I2LGNL</td>
</tr>
<tr>
<td></td>
<td>1SG110HN2F43E2VG</td>
<td>1SG110HN2F43E2VGNL</td>
</tr>
<tr>
<td></td>
<td>1SG110HN2F43I2VG</td>
<td>1SG110HN2F43I2VGNL</td>
</tr>
<tr>
<td></td>
<td>1SG166HN2F43I2VG</td>
<td>1SG166HN2F43I2VGNL</td>
</tr>
<tr>
<td></td>
<td>1SG280LN2F43I2LG</td>
<td>1SG280LN2F43I2LGNL</td>
</tr>
<tr>
<td></td>
<td>1SG280HN2F43I2VG</td>
<td>1SG280HN2F43I2VGNL</td>
</tr>
<tr>
<td></td>
<td>1SG280HN2F43I2LG</td>
<td>1SG280HN2F43I2LGNL</td>
</tr>
<tr>
<td>TX</td>
<td>1ST040EH2F35I2LG</td>
<td>1ST040EH2F35I2LGNL</td>
</tr>
<tr>
<td></td>
<td>1ST110EN2F43I2VG</td>
<td>1ST110EN2F43I2VGNL</td>
</tr>
<tr>
<td></td>
<td>1ST110EN2F43I2LG</td>
<td>1ST110EN2F43I2LGNL</td>
</tr>
<tr>
<td>DX</td>
<td>1SD110P2F43E2VG</td>
<td>1SD110P2F43E2VGNL</td>
</tr>
</tbody>
</table>
3. Intel Quartus Prime Software Guidelines

You must use the Intel Quartus Prime Pro Edition software version 21.1 or later to compile designs targeting Intel Stratix 10 I/O Limited (IOL) FPGAs.

The following topics provide guidance for migrating Intel Quartus Prime designs between Intel Stratix 10 standard OPN FPGAs and Intel Stratix 10 IOL FPGAs, and for Intel Quartus Prime software patch compatibility.

3.1. Design Migration

There are two methods for migrating a design between a standard Intel Stratix 10 FPGA and an Intel Stratix 10 I/O Limited (IOL) FPGA.

**Design Migration Method 1: Change the Device OPN**

1. In the Intel Quartus Prime software, click Assignments ➤ Device and select your targeted device.
2. You have the flexibility to change location and pin assignments, if desired. Click **Yes** when prompted, to have the Intel Quartus Prime software remove location and I/O assignments, or click **No** to keep your existing assignments.

*Figure 2. Dialog Box to Remove Location and I/O Assignments*

**Design Migration Method 2: Use the Migration User Interface**

The Migration User Interface helps in checking device compatibility and provides a comparison table—accessible from the Pin Migration View in the Pin Planner—showing migration results between the devices chosen for migration.

1. In the Intel Quartus Prime software, click Assignments ➤ Device.
2. Click the Migration Devices button at the bottom-right of the Device window.
3. In the **Migration Devices** dialog box, choose the compatible migration device that you want to target.
4. The **Pin Migration View** is available in the Pin Planner, and facilitates comparison between migration devices; it provides the following information:

- Pin number
- Migration devices
- Pin finder
- Migration result
- Show only highlighted pins
- Show migration differences
- Export
- Show column

Open the **Pin Migration View** in the Pin Planner, by clicking **View ➤ Pin Migration Window**. You can access detailed information by right-clicking your selection in the **Pin Migration View**.
3.2. Intel Quartus Prime Software Patch Compatibility

The Intel Quartus Prime software patch for Intel Stratix 10 FPGAs with standard OPN is not compatible with Intel Stratix 10 I/O Limited (IOL) FPGAs, unless the patch specifies support.

To request an Intel Quartus Prime software patch for Intel Stratix 10 IOL FPGAs, contact My Intel Support.

3.3. Related Intel Quartus Prime Software Error Messages

When compiling designs targeting Intel Stratix 10 I/O Limited FPGAs, you might encounter compilation error messages as shown below.
### Table 3. Related Intel Quartus Prime Software Error Messages

<table>
<thead>
<tr>
<th>Intel Quartus Prime Software Error Message</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>This design uses a device that is restricted to a maximum of 700 user-IOs. Currently, &lt;I/O pin count&gt; are being used!</td>
<td>Error Message for &gt; 700 Pins Utilization</td>
</tr>
<tr>
<td>The current device &lt;device OPN&gt;’s data-rate cannot exceed 499Gbps. The design’s TX data-rate is &lt;TX cumulative data-rate&gt;, and RX data-rate is &lt;RX cumulative data-rate&gt;.</td>
<td>Error Message for Design Exceeding Maximum Transceiver Bandwidth</td>
</tr>
</tbody>
</table>
4. Device Guidelines

Intel Stratix 10 I/O Limited (IOL) FPGAs support the same device configuration schemes as Intel Stratix 10 standard OPN FPGAs.

The following topics provide guidelines for configuring GPIO, LVDS, and transceiver features to ensure successful design compilation on the Intel Stratix 10 IOL FPGA.

4.1. Device Configuration Guidelines

Intel Stratix 10 I/O Limited (IOL) FPGAs have unique device IDs that control device firmware to prevent loading of unauthorized programming files.

Programming File Compatibility

The following table shows programming file compatibility between standard OPN devices and equivalent IOL OPN devices. If you target the same design to both a standard OPN device and a compatible IOL OPN device, you can choose to compile the design using IOL OPN only.

<table>
<thead>
<tr>
<th>Programming file generated with I/O Limited OPN</th>
<th>Intel Stratix 10 Standard Device</th>
<th>Intel Stratix 10 I/O Limited Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Programming file generated with standard OPN</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Method to Identify a Device OPN from the .SOF Programming File

The following steps allow you to determine whether a given .SOF file targets an Intel Stratix 10 FPGA with Standard OPN or an Intel Stratix 10 FPGA with IOL OPN.

1. Go to the Intel Quartus Prime software command-line interface.
2. Change the working directory to locate the .SOF file:
   ```
   $ cd <sof_file_directory>
   ```
3. Type and run the quartus_pfg command:
   ```
   $ quartus_pfg -i <filename>.sof
   ```
4. In the displayed message, search for Device: `<device_OPN>`.

The following figure illustrates an example of the displayed Intel Quartus Prime software message. The part number of the targeted Intel Stratix 10 I/O Limited FPGA ends with `<NL>`.
4.2. GPIO and LVDS Guidelines

The following topics provide input/output (I/O) resource comparisons and design migration guidelines.

4.2.1. I/O Resource Comparison Between Standard OPN and IOL OPN Devices

The following table compares Intel Stratix 10 standard OPN and Intel Stratix 10 I/O Limited (IOL) OPN FPGAs.
Table 5. Similarities and Difference Between Intel Stratix 10 Standard OPN and I/O Limited OPN FPGAs

<table>
<thead>
<tr>
<th>Item</th>
<th>Similarities</th>
<th>Differences</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O Feature</td>
<td>I/O features are identical. (1)</td>
<td>None</td>
</tr>
<tr>
<td>Pin Function</td>
<td>All pin functions including power and configuration pins that are described in the Intel Stratix 10 device pin-out files are identical. (2)</td>
<td>None</td>
</tr>
<tr>
<td>I/O Utilization Limit</td>
<td>For F35 &amp; F43 packages, the total I/O count utilization limits are identical between standard OPN and IOL OPN devices, because both have &lt;700 I/O pins only.</td>
<td>For F50, F55 &amp; F74 packages (3) the total I/O utilization is limited to a maximum of 700 pins for IOL OPNs. The 700 I/O pins can be any pin combination listed within the pin-out file. For designs that utilize more than 700 pins in standard OPN devices, the total I/O count must be reduced to ≤700 to fit in the IOL device.</td>
</tr>
</tbody>
</table>

Note: 1. Refer to Intel Stratix 10 General Purpose I/O User Guide for information on Intel Stratix 10 I/O features.
2. Refer to Intel® Stratix® 10 Device Pin-Out Files.
3. Intel Stratix 10 IOL FPGAs with F50, F55 & F74 package options are not available currently. For information, contact your Intel representative.

4.2.2. Design Migration

When migrating a design from a larger I/O utilization count to a lesser I/O utilization count, you should evaluate the total device power and pin connections change.

Total Device Power Consumption

The device power consumption depends on the I/O utilization in the design. When I/O utilization changes after migrating a design from standard OPN to I/O Limited (IOL) OPN devices, you should evaluate power consumption using the Intel Quartus Prime Power Analyzer or Intel FPGA Power and Thermal Calculator, to achieve accurate power estimation.

For related information, refer to:
- Intel® FPGA Power and Thermal Calculator User Guide

Pin Connection for Unused Pins

If there are unused I/O pins after migrating a design from standard OPN to IOL OPN devices, you must connect the unused pins as defined in the Intel Quartus Prime software. The following steps illustrate this process:

1. In the Project Navigator in the Intel Quartus Prime software, right-click the OPN, and then click Device.
2. In the Device dialog box, click the Device and Pin Options button.

3. Navigate to the Unused Pins tab in the Category tree at the left side of the Device and Pin Options dialog box. Select your preferred setting from the dropdown list in the Reserve all unused pins section.
4.2.3. Error Message for > 700 Pins Utilization

When a design has I/O utilization exceeding 700 pins for a package that has more than 700 I/O pins, the Intel Quartus Prime software issues an error message during compilation.

Error message: This design uses a device that is restricted to a maximum of 700 user-I/Os. Currently, \textless I/O pin count\textgreater  are being used!"

4.3. Transceiver Guidelines

Intel Stratix 10 I/O Limited (IOL) FPGAs have additional Intel Quartus Prime Fitter placement restrictions that set the maximum transceiver bandwidth at 499 Gbps for respective TX accumulative data rate and RX accumulative data rate across all used transceiver channels in a design.

Placement guidelines in the respective L/H/E/P-Tile Transceiver User Guide and in AN 778 apply for both standard Intel Stratix 10 and IOL Intel Stratix 10 FPGAs.

For related information, refer to:

- L- and H-Tile Transceiver PHY User Guide
- E-Tile Transceiver PHY User Guide
- Intel FPGA P-Tile Avalon Streaming IP for PCI Express Design Example User Guide
- P-Tile Avalon® Memory-mapped Intel® FPGA IP for PCI Express* User Guide
- AN 778: Intel® Stratix® 10 L-Tile/H-Tile Transceiver Usage

4.3.1. Transceiver Bandwidth Calculation

The transceiver data rate for each channel that is applied to the design's TX cumulative data rate and RX cumulative data rate is subject to two native PHY IP configurations: signal modulation mode, and dynamic reconfiguration status.

Signal Modulation Mode

By default, the native PHY IP applies non-return-to-zero (NRZ) modulation for electrical signaling unless you select Pulse-Amplitude Modulation 4-Level (PAM4) in E-Tile. L-Tile and H-Tile have NRZ modulation for electrical signaling only.

When a channel uses NRZ, the data rate value counts as a single channel; however, when a link uses PAM4, the data rate value counts as two channels when it uses two physical channels.

Example of the calculation for a use model with one channel of 10 Gbps using NRZ and one link 56 Gbps using PAM4 signaling:

\[
\text{Bandwidth} = (10 \text{ Gbps} \times 1 \text{ channel}) + (56 \text{ Gbps} \times 2 \text{ channels}) = 122 \text{ Gbps}
\]
Dynamic Reconfiguration Status

For L-Tile, H-Tile, and E-Tile devices, the data rate used by the Intel Quartus Prime software for TX and RX data rate is subject to the status of the transceiver dynamic reconfiguration feature.

When you have not enabled dynamic reconfiguration, the data rate is defined by the data rate attribute set in the native PHY IP. When you have enabled dynamic reconfiguration, the data rate is defined by the maximum data rate of the channel per the fastest transceiver specification of the L-Tile, H-Tile, or E-Tile.

Transceiver bandwidth is further reduced according to the following definitions:

- For L-Tile devices, the Intel Quartus Prime software applies the maximum data rate of the channel at transceiver speed grade 2, because L-Tile does not have transceiver speed grade 1.
- For H-Tile and E-Tile devices, the Intel Quartus Prime software applies the maximum data rate of the channel at transceiver speed grade 1, even though the I/O Limited (IOL) OPN transceiver speed grade is 2.

The following table illustrates an example that uses 10 Gbps across all channels, within an L-Tile, H-Tile, or E-Tile device.

Table 6. Effective Data Rate per Channel for Intel Quartus Prime Software Transceiver Bandwidth Calculation with Example of 10Gbps Native PHY IP

<table>
<thead>
<tr>
<th>Channel Location</th>
<th>Applied Data Rate per Channel (Gbps)</th>
<th>Channel Location</th>
<th>Applied Data Rate per Channel (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L-Tile</td>
<td>H-Tile</td>
<td>E-Tile (NRZ/PAM4)</td>
<td>L-Tile</td>
</tr>
<tr>
<td>23</td>
<td>10</td>
<td>10 / 20</td>
<td>23</td>
</tr>
<tr>
<td>22</td>
<td>10</td>
<td>10 / 20</td>
<td>22</td>
</tr>
<tr>
<td>21</td>
<td>10</td>
<td>10 / 20</td>
<td>21</td>
</tr>
<tr>
<td>20</td>
<td>10</td>
<td>10 / 20</td>
<td>20</td>
</tr>
<tr>
<td>19</td>
<td>10</td>
<td>10 / 20</td>
<td>19</td>
</tr>
<tr>
<td>18</td>
<td>10</td>
<td>10 / 20</td>
<td>18</td>
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<tr>
<td>17</td>
<td>10</td>
<td>10 / 20</td>
<td>17</td>
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<td>16</td>
<td>10</td>
<td>10 / 20</td>
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<td>15</td>
<td>10</td>
<td>10 / 20</td>
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<td>10 / 20</td>
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<td>10 / 20</td>
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<td>10</td>
<td>10 / 20</td>
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</tr>
<tr>
<td>8</td>
<td>10</td>
<td>10 / 20</td>
<td>8</td>
</tr>
</tbody>
</table>

continued...
### 4.4. Error Message for Design Exceeding Maximum Transceiver Bandwidth

When a design exceeds the maximum transceiver bandwidth of ≤499Gbps, the Intel Quartus Prime Fitter issues error messages during compilation. The system displays information relating to the error, immediately before the error message.

Information messages part 1 lists all the RX and TX channels and the data rate applied by the Fitter in transceiver bandwidth calculations, with one message line for each TX and RX channel. The message identifies whether the channel enables the transceiver dynamic reconfiguration feature. The following examples illustrate these information messages:

RX Channel at PIN_<pin_number> is connected to the core and <reconfigurable/not reconfigurable>. The data-rate used is <data-rate> Gbps.

TX Channel at PIN_<pin_number> is connected to the core and <reconfigurable/not reconfigurable>. The data-rate used is <data-rate> Gbps.

Information messages part 2 lists the TX cumulative data rate and RX cumulative data rate that is applied by the Intel Quartus Prime software to determine whether transceiver bandwidth limit is exceeded. The following examples illustrate these information messages:

TX cumulative data-rate of the current design is <data-rate Gbps>.

RX cumulative data-rate of the current design is <data-rate Gbps>.

An error message appears if the TX or RX cumulative data rate of the current design exceeds 499 Gbps.

The current device <device OPN>’s data-rate cannot exceed 499Gbps. The design’s TX data-rate is <TX cumulative data-rate>, and RX data-rate is <RX cumulative data-rate>.
The following figures show examples of Intel Quartus Prime software information messages and error messages for the following data rates, respectively:

- TX and RX cumulative data rate of 498.998400 Gbps
- TX and RX cumulative data rate of 499.200000 Gbps
- TX and RX cumulative data rate of 1184.000000 Gbps

**Figure 10.** Example of Intel Quartus Prime Software Information Messages with TX and RX Cumulative Data Rate of 498.998400 Gbps, with Transceiver Dynamic Reconfiguration Disabled

**Figure 11.** Example of Intel Quartus Prime Software Information and Error Messages with TX and RX Cumulative Data Rate of 499.200000 Gbps, with Transceiver Dynamic Reconfiguration Disabled
Figure 12. Example of Intel Quartus Prime Software Information and Error Messages With TX and RX Cumulative Data Rate of 1184.00000 Gbps, with Transceiver Dynamic Reconfiguration Enabled

<table>
<thead>
<tr>
<th>Message</th>
<th>Message ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX Channel at PEN_000H is connected to the core and reconfigurable. The data-rate used is 28.398000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_030H is connected to the core and reconfigurable. The data-rate used is 17.409000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_070H is connected to the core and reconfigurable. The data-rate used is 28.398000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_100H is connected to the core and reconfigurable. The data-rate used is 17.409000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_130H is connected to the core and reconfigurable. The data-rate used is 28.398000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_170H is connected to the core and reconfigurable. The data-rate used is 17.409000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_210H is connected to the core and reconfigurable. The data-rate used is 28.398000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_250H is connected to the core and reconfigurable. The data-rate used is 17.409000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_300H is connected to the core and reconfigurable. The data-rate used is 28.398000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_330H is connected to the core and reconfigurable. The data-rate used is 17.409000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_380H is connected to the core and reconfigurable. The data-rate used is 28.398000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_420H is connected to the core and reconfigurable. The data-rate used is 17.409000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_460H is connected to the core and reconfigurable. The data-rate used is 28.398000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX Channel at PEN_500H is connected to the core and reconfigurable. The data-rate used is 17.409000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>TX cumulative data-rate of the current design is 1184.000000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>RX cumulative data-rate of the current design is 1184.000000 Gbps</td>
<td>22328</td>
</tr>
<tr>
<td>The current device 1G1110H12412V0AL’s data-rate cannot exceed 495Gbps. The design’s TX data-rate is 1G1110H12412V0AL’s data-rate cannot exceed 495Gbps. The design’s TX data-rate is</td>
<td>23046</td>
</tr>
<tr>
<td>Automatically applied size constraint on clock trees for periphery interfaces</td>
<td>19750</td>
</tr>
<tr>
<td>1.3K input pins were inserted to turn-off unconnected output partition boundary pins in the design.</td>
<td>26890</td>
</tr>
</tbody>
</table>
# 5. Document Revision History for AN 951: Intel Stratix 10 I/O Limited FPGA Design Guidelines

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2021.05.06</td>
<td>21.1</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>