AN 944: Thermal Modeling for Intel® Agilex™ FPGAs with the Intel® FPGA Power and Thermal Calculator

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1. List of Abbreviations

Table 1. Definition of terms

Abbreviation	Description
CFD	Computational Fluid Dynamic, a numerical analysis method for solving the conjugated heat transfer problems.
CTM	Compact Thermal Model, a geometric model that is used as an input to CFD tool.
DTS	Digital thermal sensor.
FAE	Field application engineer.
FPGA	Field Programmable Gate Array.
HBM	High Bandwidth Memory.
IHS	Integrated Heat Spreader - case of an FPGA.
MCM	Multi-Chip Module - an integrated circuit (IC) with more than one die.
PTC	Intel® FPGA Power and Thermal Calculator.
RTL	Register-transfer level.
SCM	Single Chip Module.
T_{CASE}	Integrated Heat Spreader or Case Temperature. The case temperature of a component is measured with an attached heat sink. This temperature is measured at the top geometric center of the package case/die.
TTP	The total power dissipation of the device. This includes static power, with static power savings subtracted. The PTC reports this value in the Power Summary window.
TDP	Thermal Design Power, the power dissipated in a die that is used for thermal analysis purposes.
T_A	Ambient Temperature, measured locally surrounding the FPGA. The ambient temperature should be measured just upstream of a passive heat sink or at the fan inlet for an active heat sink.
T_{CORE}	Core Fabric Die Temperature.
T_J	Junction Temperature.
$T_{J\text{-}MAX}$	Maximum Junction Temperature, a maximum allowable absolute temperature rating of the device or a targeted value.
TIM	Thermal Interface Material.
TSD	Temperature Sensor Diode.
VID	Voltage identification code.

2. Introduction

The Intel Agilex™ FPGA is a multi-chip device, whose thermal engineering requires specific design-related steps to determine power and other thermal design parameters.

The Intel FPGA Power and Thermal Calculator (PTC) provides thermal design parameters for Intel Agilex devices. The PTC is available as a standalone tool for use with early-stage designs, and as an integrated tool within the Intel Quartus® Prime software, for thermal calculations with later-stage FPGA designs, for higher accuracy.

This application note explains the necessary steps for thermal design for an Intel Agilex FPGA using the PTC, and highlights differences in procedure between design targeting Intel Agilex and Intel Stratix® 10 devices.

The following topics introduce the necessary terminology, tools, and collateral necessary for the thermal analysis:

- Intel Agilex FPGA Package Physical Design
- Intel Agilex Thermal Design Parameters
- Intel Agilex Thermal Design Process
- Intel FPGA Power and Thermal Calculator (PTC) for Intel Agilex Devices

3. Intel Agilex FPGA Package Mechanical Design

An Intel Agilex FPGA comes in a ball grid array (BGA) package with a copper integrated heat spreader (IHS). The BGA package can be square or rectangle, and can contain up to three types of dies, as follows:

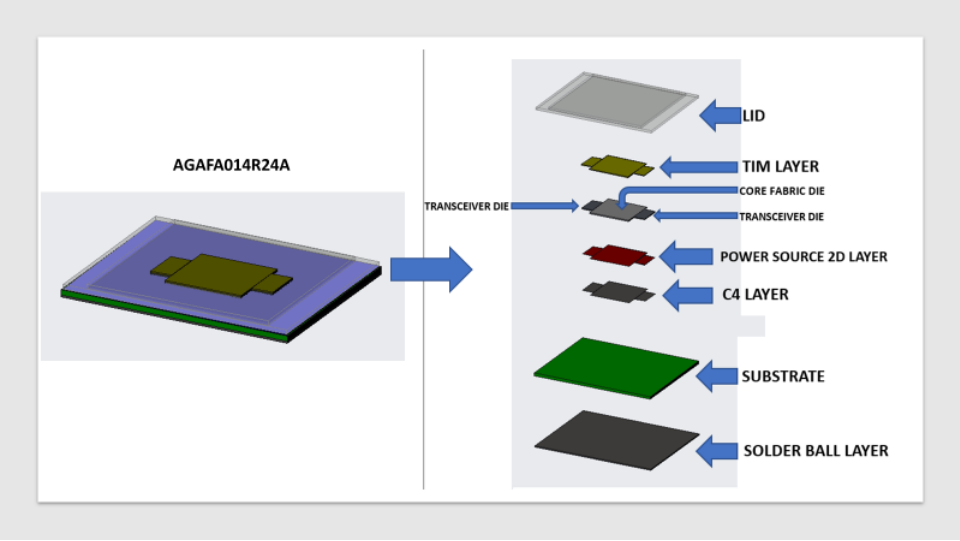
- **Core fabric die.** This is the main FPGA die, which contains the basic logic resources, and is available in various sizes and grades. All Intel Agilex devices have a single core fabric die.
- **Transceiver die.** Transceiver dies are offered in four types: H-Tile, E-Tile, F-Tile, and R-tile. Each transceiver tile type supports certain protocols and transceiver speeds. Depending on the package size, an Intel Agilex device can support up to 4 transceiver dies.
- **HBM die.** The HBM die is available in 4 high or 8 high configurations. Not all Intel Agilex packages have HBM, however those that do can have either one or two HBM dies.

All packages contain solder thermal interface material (TIM1) for enhanced thermal performance.

3.1. Intel Agilex Physical Package Structure

Figure 1. Physical Package Structure

This is a typical package structure relevant to thermal analysis and as laid out in the compact thermal models. This package only shows the core fabric die and two transceiver dies.



4. Intel Agilex FPGA Thermal Design Parameters

The Intel Agilex FPGA thermal parameters do not include the traditional junction-to-case thermal resistance (θ_{JC}) and junction-to-board thermal resistance (θ_{JB}) values, due to its multi-chip package construction. Instead of 2R resistor values, Intel provides a compact thermal model (CTM) of each package along with thermal parameters for each design through the Intel FPGA Power and Thermal Calculator (PTC). The PTC thermal parameters include T_J, Ψ_{CA}, $T_{AMBIENT}$, T_{CASE}, Ψ_{JC} and total thermal power (TTP). The table below lists the thermal design parameters used in this document.

Table 2. Thermal Design Parameters

Parameter	Description
T_A	Ambient temperature, measured locally surrounding the FPGA. Measure the ambient temperature just upstream of a passive heat sink or at the fan inlet for an active heat sink. This value affects the junction temperature of the main FPGA core fabric die and its power dissipation.
$T_{J\text{-}MAX}$	The maximum rated junction temperature of a die, or could be the design goal. For example, a particular die could have a manufacturer's specified $T_{J\text{-}MAX}$ of 100°C, but designers can specify a $T_{J\text{-}MAX}$ of less than 100°C as part of their design requirement. *Note:* The active junction temperature of the package T_J varies across the package and die, and varies with design. The junction temperatures across the package are used by the PTC only for more accurate power and temperature calculation.
Power	The PTC reports the power dissipation of each die individually.
Total Thermal Power (TTP)	The total power dissipation of the device. This includes static power, with static power savings subtracted. The PTC reports this value in the Power Summary window.
Ψ_{JC}	The thermal resistance between each of the dies in the package and the center of the package integrated heat spreader. (See Figure 2). A multi-chip module (MCM) such as the Intel Agilex device will have as many Ψ_{JC} values as the number of dies in the package. The PTC reports the maximum Ψ_{JC} value which corresponds to the die with the highest temperature on the device. The Ψ_{JC} value is calculated by this equation: $\Psi_{JC} = (T_{J\text{-}MAX} - T_{CASE}) / TTP$ *Note:* Ψ_{JC} values are not constant for a specific package and change as the FPGA resource usage changes.
Ψ_{CA}	The thermal resistance between the center of the package IHS and the ambient temperature. (See Figure 3.) Ψ_{CA} can be used as a figure of merit in assessing the required cooling solution for a design. For example, the lower the Ψ_{CA} value, the more aggressive cooling solution is needed. The value of Ψ_{CA} is calculated by this equation: $\Psi_{CA} = (T_{CASE} - T_A) / TTP$ *Note:* Ψ_{CA} values are not constant for a specific package and change as the FPGA resource usage changes. You must recalculate this value for each design.
T_{CASE}	The temperature at the top center of the IHS. For a design to not exceed its $T_{J\text{-}MAX}$, the cooling solution must be able to maintain the T_{CASE} temperature at or below the T_{CASE} temperature reported by the PTC.

continued...

Parameter	Description
	Note: T_{CASE} values are not constant for a specific package and change as the FPGA resource usage changes.
Temperature Margin	Temperature margin is calculated relative to a designated maximum junction temperature, T_J.
Power Margin	Power margin indicates the power buffer available before the maximum junction temperature, T_J is exceeded.

Figure 2. Individual Die Thermal Resistance to the Top of IHS

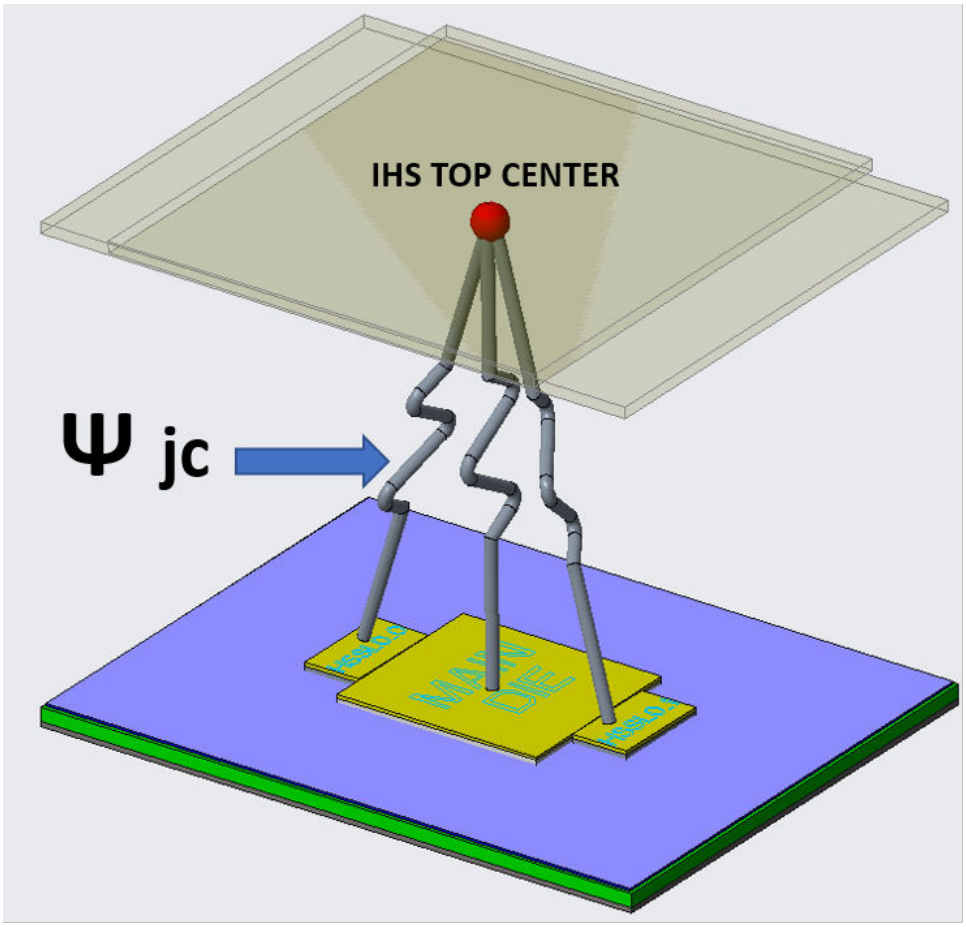
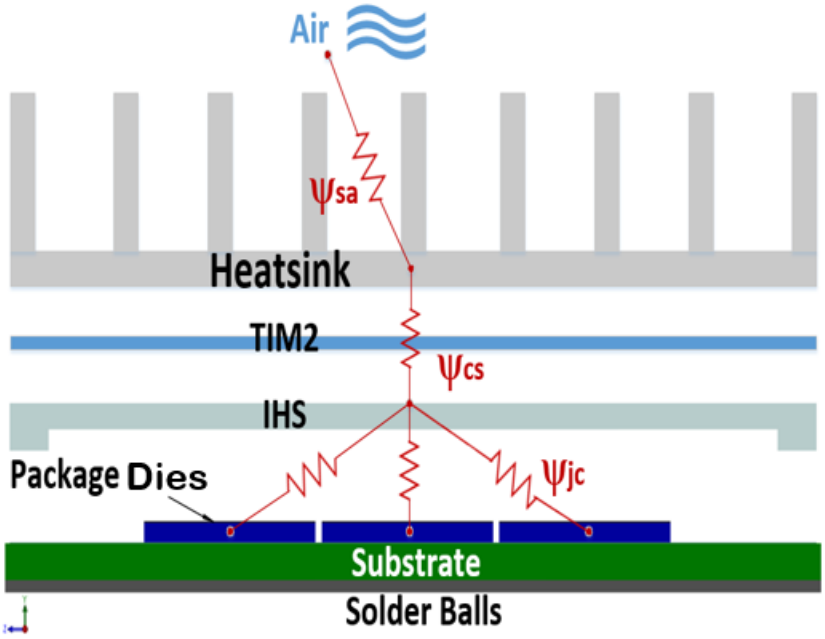


Figure 3. Thermal Resistance

The diagram shows the thermal resistance from each die to the IHS top surface and also to the air.



4.1. Intel Agilex Compact Thermal Model (CTM)

The system-level thermal analysis of the Intel Agilex FPGA requires the use of its compact thermal model (CTM) in a computational fluid dynamic (CFD) tool. The CTMs are simplified mechanical models of the packages with modified thermal properties so they can predict an accurate case temperature with uniform power distribution for each die. The results of the CFD analysis are valid only to evaluate the T_{CASE} of the package. Power values for input to the model come from the Intel FPGA Power and Thermal Calculator (PTC).

The IHS center temperature or $T_{CASE-CENTER}$ is useful to evaluate the cooling design. If the CFD-calculated $T_{CASE-CENTER}$ is less than or equal to the T_{CASE} reported by the PTC, then the maximum T_J specified in the PTC will not be exceeded.

The latest CTMs for use with Intel Agilex devices, are offered in ECXML format, which is compatible with the following CFD tools:

- Icepak* from ANSYS
- Flotherm* from Mentor Graphics*
- 6SigmaET* from Future Facilities

If your company does not use any of the above CFD tools, Intel can provide a step file of the CTM, by request. The step file model is compatible with other thermal tools, such as:

- Thermal Analysis* from SolidWorks
- Thermal Analysis by Autodesk

Step models do not have built in thermal material properties; that data is provided separately, and you must add it to the models.

4.2. Intel Agilex Temperature Sensing

Each die in an Intel Agilex FPGA contains at least one digital thermal sensor (DTS) and one temperature sensing diode (TSD). Each DTS has no physical connection to device pins and must be read using temperature sensing software.

The TSDs connect to pins on the FPGA, to which you must connect an external temperature-reading device, such as the Maxim Integrated Max6581, Max 31730, or Texas Instrument TMP468. Both the DTS and TSD report the temperature of their physical location on the die, which may or may not be the hottest location on the die. For this reason, the Intel FPGA Power and Thermal Calculator (PTC) reports the maximum temperature that each die should be reporting for the method used.

Note: Intel recommends using DTS. Thermal diode measurements are not validated by Intel, and must be validated by you if you choose to use them. Ensure that you read the latest application note on the diode measurement.

For example, given a device with two transceiver dies, the PTC would report temperatures like those in the table below. The reported temperatures are not the maximum temperatures for any of the dies; however, if the reported values exceed these values, it indicates that the cooling is not as expected, and the case temperature is likely to exceed the target (80°C, in this case). Temperatures exceeding these values also indicate that the operating power consumption is beyond what the PTC is showing—probably due to insufficient cooling.

Table 3. PTC Temperature Report Format

Monitor		Temperature Target (°C) (for example only)
Location	Sensor	
Case	dts01[1]	80
FPGA Core	dts11	85
FPGA Core	tds1[2]	83
FPGA Core	tds2	90
FPGA Core	dts1	88
HSS_0_0	tds1	92
HSS_0_0	dts1	90
HSS_0_1	tds1	88
HSS_0_1	dts1	90

- [1] Can be read only if a thermocouple is embedded in the case. Usually this method is used for verification during system design.
- [2] External pinned-out sensor read using an external device.

4.3. Thermal Sensor Accuracy

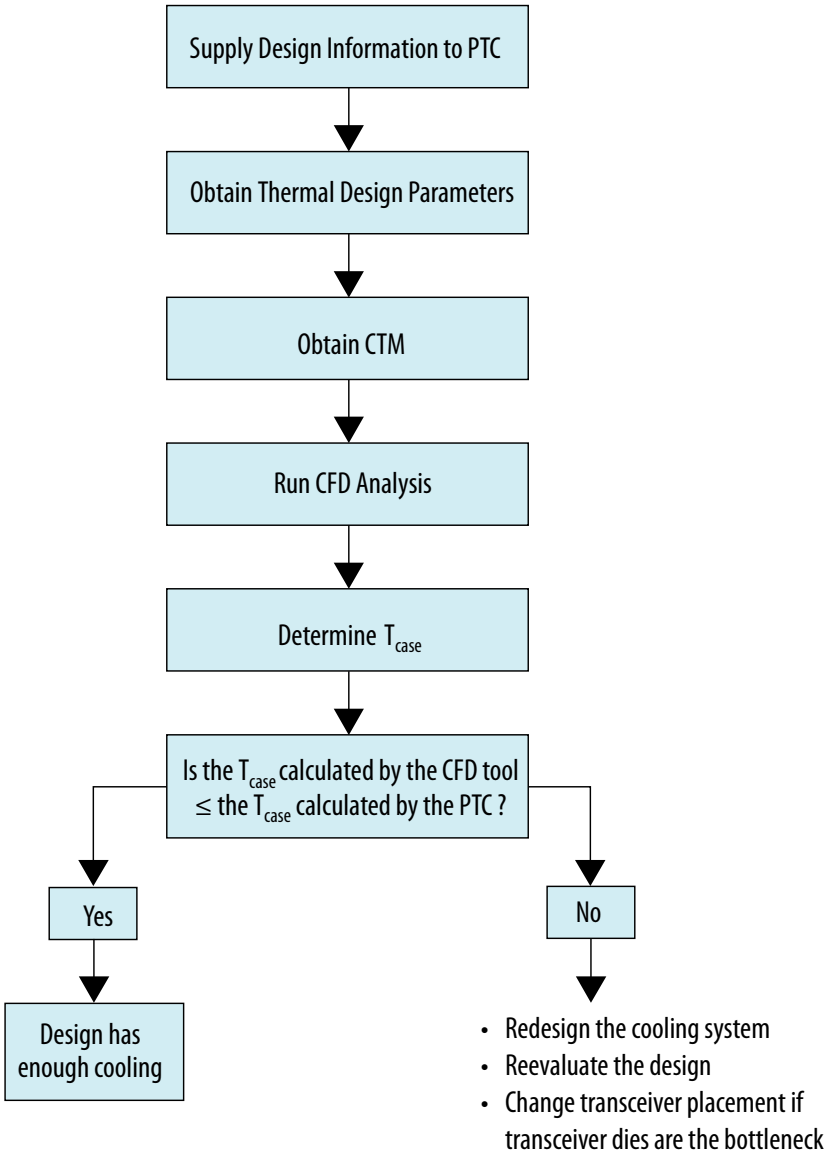
Both digital thermal sensors (DTSs) and thermal sensor diodes (TSDs) have a sensor accuracy of ±5°C. This margin of error means that a reported value of 100°C could actually be as high as 105°C, which might adversely affect the reliability and timing closure of the FPGA. Therefore, you should design for a cooling margin of at least 5°C, to ensure that the resulting cooling solution remains within the margin of error of the sensors, and does not exceed the desired maximum junction temperature.

When using TSDs you must calibrate the external device to your design circuitry. Reported temperatures from the external temperature sensors can be incorrect by 10°C or more, depending on which die temperature is measured. For further detail on the bonded sensors and how to read them, refer to AN 769: Intel FPGA Remote Temperature Sensing Diode Implementation Guide.

5. Thermal Design Process for Intel Agilex Devices

This topic describes the stages of the Intel Agilex FPGA thermal design process.

Figure 4. Thermal Design Flow



Thermal Design Stages

1. Supply design information to the Intel FPGA Power and Thermal Calculator (PTC). This step provides the necessary data to estimate the power dissipation of each die. The inputs include the FPGA design information as well as the thermal design requirements of T_A and $T_{J\text{-}MAX}$ and power margin selection. At this point the design is still in its early stages; be aware that power predictions at this point may have inaccuracies and should not be taken as indicative of the final values for a functional design.

   Note: It is important to ensure that your design information is entered as accurately as possible, to ensure the most accurate thermal calculations.
2. Obtain thermal design parameters from the PTC. The power dissipation of the transceiver die is provided as a constant value, but the main core die power dissipation is provided as a function of its junction temperature, and should be entered into the computational fluid dynamic (CFD) tool as a function of temperature for most accurate results.
3. Obtain the compact thermal model (CTM). Contact your Intel Field Application Engineer (FAE) to obtain the applicable CTM for the CFD analysis.
4. Run the CFD analysis. Model the system in the CFD tool and apply all the applicable power values to the corresponding dies. The CFD solution provides the T_{CASE}. The CFD cannot predict the transceiver and HBM die temperatures, therefore those must be calculated manually.
5. Compare the CFD results with the PTC results. If the CFD-predicted value for the T_{CASE} is equal to or less than the T_{CASE}calculated by the PTC, then the cooling solution is sufficient. If the T_{CASE} predicted by the CFD is higher than that calculated by the PTC, then additional cooling, or design changes such as transceiver placement optimization, may be needed. The PTC also allows for entering a cooling solution in the form of Ψ_{CA} , in which case it reports the resulting junction temperature; the PTC can also solve for needed ambient temperature to meet a required junction temperature.

5.1. Thermal Parameter Dependencies and Accuracy

The Intel Agilex FPGA thermal design parameters are unique for every project. Thermal design parameters are mainly determined by the power, local power density, and power ratio of dies. Any change to the design requires design information to be updated accordingly in the Intel FPGA Power and Thermal Calculator (PTC). That is, a set of thermal parameters calculated early in the project, may no longer be valid if the FPGA utilization is changed later.

At the beginning of the project, the only power and thermal parameter calculations possible are those performed in the standalone PTC without using an actual RTL design. However, when the RTL design becomes available, you should run the PTC integrated within the Intel Quartus Prime software, and recalculate the power and other thermal parameters with the actual RTL design. Calculations in the integrated version of the PTC are based on actual routings inside the core fabric, and are more accurate.

6. Power and Thermal Calculator (PTC) for Intel Agilex Devices

The Intel FPGA Power and Thermal Calculator (PTC) can estimate the power consumption of an Intel Agilex FPGA and generate the thermal parameters needed for a system thermal simulation or evaluation of an existing solution..

The PTC is available in two versions:

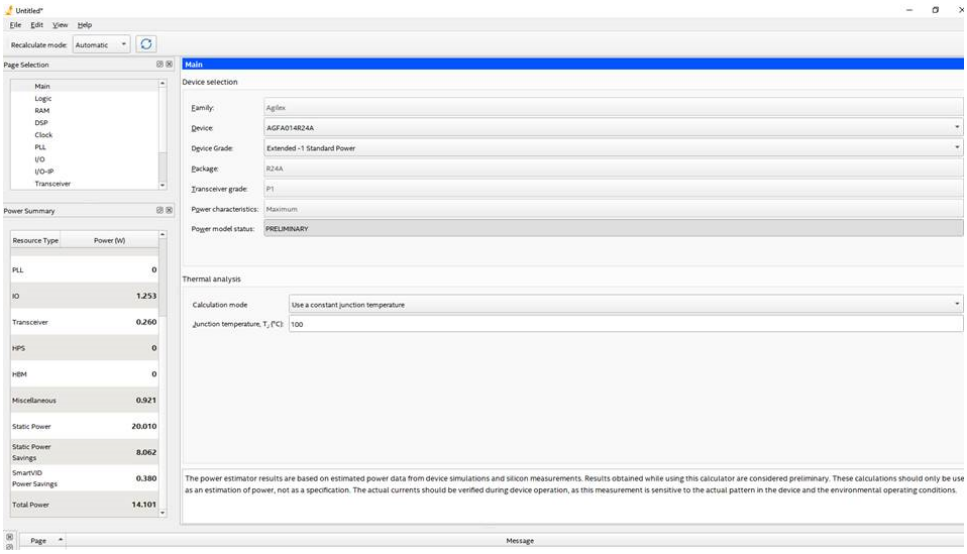
- A standalone version that you can use without having an actual RTL design. You provide all input to this version manually, or from an imported `.ptc` or `.csv` file. The standalone version is essential at the early stages of projects when power and cooling requirements must be determined and no RTL design is available.
- An embedded version that is part of the Intel Quartus Prime software. Input data for this version is generated when you compile an RTL design. This version can provide more accurate results, and should be used when possible.

The Intel Quartus Prime PTC can export a design file to the standalone PTC for ease of use and faster what-if analysis.

The PTC allows you to enter and select relevant information for your FPGA design and calculate relevant power and relevant thermal design information for that design. The data provided to the PTC includes device information, FPGA logic design information, and thermal information. The effects of the above inputs determine the overall power dissipation of each die and the thermal characteristics of the package to use for system thermal modeling.

The following figure depicts the PTC Main page, where you can select your FPGA device and enter a junction temperature while the thermal calculator is off. In this mode the calculated power is for all the dies at the same temperature and the PTC does not report the individual die thermal power for thermal analysis.

Figure 5. Intel FPGA Power and Thermal Calculator Main Page



You can download the standalone PTC from the *Additional Software* tab on the *Download Center for FPGAs* page, here: https://fpgasoftware.intel.com/21.1/?edition=pro

The *Intel FPGA Power and Thermal Calculator User Guide* is available here: https://www.intel.com/content/www/us/en/programmable/documentation/mdj1572270584041.html

6.1. Device Selection and Analysis Example

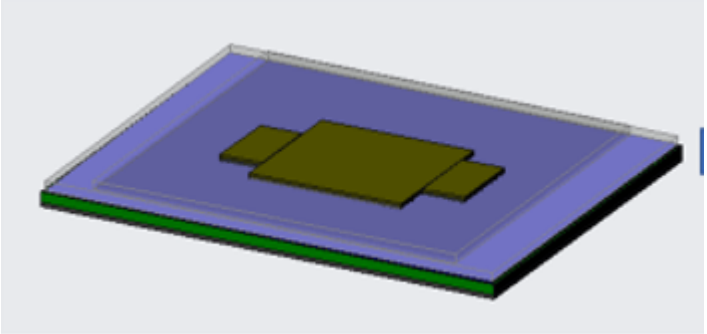
This section illustrates the setting of Intel FPGA Power and Thermal Calculator (PTC) parameters for an example thermal analysis of a PCIe board. The first step in the design process is to select an FPGA device.

For the purpose of this example, choose a AGFA014R24A Intel Agilex device, which has E and P transceiver tiles in addition to the core die.

Table 4. Intel Agilex FPGA AGFA014R24A Details

Feature	Value	Comment
Family	Intel Agilex	
Device	AGFA014R24A	Intel Agilex FPGA with P and E tiles.
Package	R24A	47x36mm BGA package
Device Grade	Extended -1 standard power	
Transceiver Grade	P1	

Figure 6. Top View of AGFA014R24A with Integrated Heat Spreader (IHS) Removed



6.2. Logic Design Information

The Intel FPGA Power and Thermal Calculator (PTC) has several pages for data entry.

The subject of this document is thermal analysis, therefore it focuses primarily on the thermal-related settings. For broader and more detailed information, refer to the *Intel FPGA Power and Thermal Calculator User Guide*.

Main Design Entry

The following table shows settings for our PCIe board example.

Table 5. Values for Example AGFA014R24A Intel Agilex Design

PTC Page	Values for this Design	Comment
Logic	• 900,000 Half ALM • 1,800,000 FF • Clock: 500 MHz • Toggle rate: 25%	
RAM	• M20K • 5000 blocks • Data width: 8 • RAM depth: 32 clock • Frequency: 500 • Clock: 50%	
DSP	• Configuration two 18×16 • # of instances: 4000 • Clock: 500 MHz • Toggle rate: 25%	
Clock	• Clock: 500 MHz • Total fan out: 40,000 • Global enable: 100% • Local enable: 100%	
PLL	• PLL Type: ATX PLL • PLL block: 3 • Output frequency: 6000 MHz	
I/O	• Application: GPIO	None

continued...

PTC Page	Values for this Design	Comment
I/O-IP	• DDR4 SDRAM • Data width: 32	None
Transceiver	• E-Tile, HSSI_0_1, channels 0-11 active at 28 MBPS, NRZ • P-Tile, HSSI_0_0, PCIe Gen4×16, 500 MHz	
HPS		None
HBM		None

At this point the power summary window shows a total power of 64 W for the FPGA when the maximum junction temperature ($T_{J\text{-}MAX}$) is set to 25°C. Changing the $T_{J\text{-}MAX}$ to 90°C increases the total power to 73 W. The power increase is due to rise in static or leakage power. The static power is mainly a function of temperature.

6.3. Thermal Page and Thermal Design Parameters

The maximum junction temperature rating of all Intel Agilex dies is 100°C unless stated otherwise in the documentation.

Inputs to the Intel FPGA Power and Thermal Calculator (PTC) Thermal Page

In the Intel FPGA Power and Thermal Calculator (PTC), you must select the type of analysis that you want to perform, and provide the system thermal parameters.

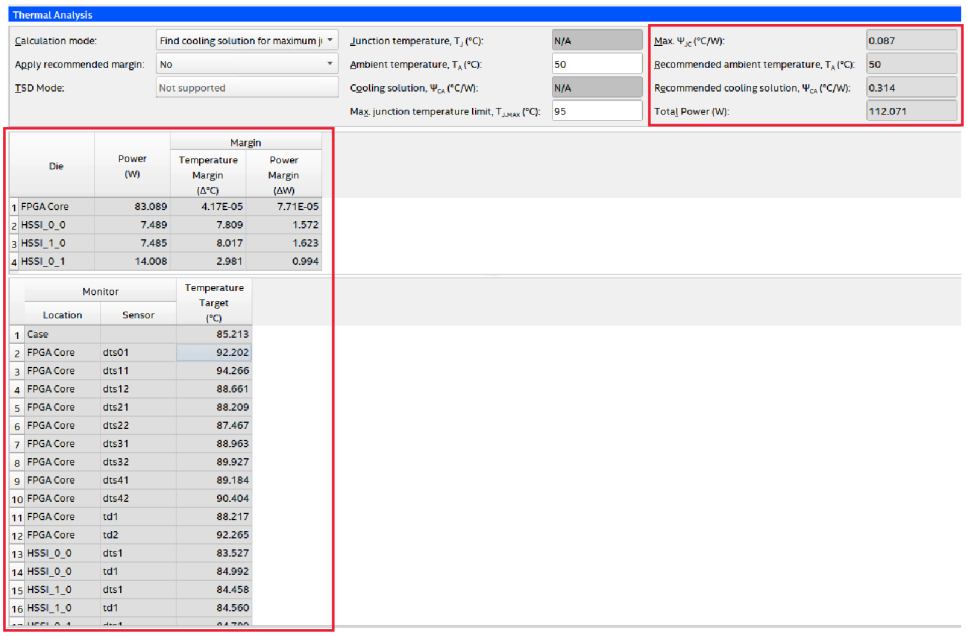
With the **Thermal** page active, you must choose appropriate settings for **Calculation Mode** and **Recommended margin**:

- **Calculation Mode**. Choose one of the following:
  - Use a constant junction temperature.
    - This mode assumes that all the dies are at the same fixed, constant temperature. The power calculated in the constant junction temperature mode is not representative of actual power during use. It is unlikely that all components of the die are at uniform temperature during normal operation. For more representative power, use the other calculation modes that utilize the thermal calculator.
    - Enter the junction temperature for this mode, on the **Main** page or the **Thermal** page.
  - Find a cooling solution for a maximum junction temperature.
    - In this mode the PTC finds the T_{CASE}, cooling solution, Ψ_{CA}, and power of all the dies, while no die can exceed the entered maximum T_J.
    - Enter the maximum T_J and ambient temperature suitable for the design. (For our example, assume a maximum T_J of 95°C, and an ambient temperature of 50°C.
  - Find a maximum junction temperature for a cooling solution.
    - In this mode the PTC finds the thermal parameters for a known cooling solution and ambient temperature.
    - Enter the Ψ_{CA} and ambient temperature.
  - Find an ambient temperature for a cooling solution.
    - In this mode the PTC finds the ambient temperature which can allow the specified cooling solution to meet the junction temperature target and maximum T_J.
    - Enter the maximum T_J suitable to the design and Ψ_{CA}.
- **Apply recommended margin**. Choose one of the following:
  - Set this field to *yes* if the power model status in the main page is not final. Added margins are set very conservatively at 25% extra power. Consult your Intel Field Application Engineer (FAE) before adding margin power to your design.
  - In general, it is good engineering practice to add some margin very early in the design cycle when the RTL design is not yet available, and only the PTC is used for evaluation. You can do this by applying, for example, 5% higher toggle rates or clock frequencies to various logic settings to increase the core power. Transceiver function, power, and placement are usually stable and should not change through the course of the project, therefore no additional margin need apply there.

Intel FPGA Power and Thermal Calculator (PTC) Thermal Page Outputs

The following figure shows the PTC Thermal page for the PCIe board example, with output fields circled in red.

Figure 8. Intel FPGA Power and Thermal Calculator (PTC) Thermal Page - Outputs Marked in Red



The thermal page outputs are as follows:

- **Die power** is the thermal power dissipated by each die, and is used for the thermal analysis.
- **Temperature margin** for each die. In the case of our example, this is calculated relative to a designated maximum T_J of 95°C. Often, one or more dies may have no margin, because the solution is calculated for the specified maximum T_J. In this example, the core fabric is operating at 95°C. The HSSI_0_0 transceiver is operating at 95-5.2= 89.8°C and HSSI_0 transceiver is operating at 93.3°C.
- **Power margin**, The PTC calculates the power margin for each die. That is the power for resources that can be added before the maximum T_J is exceeded under the same cooling condition. This is only an approximate indication, as the exact value varies depending on the specific subsystem to which the power is allocated. Any increase or decrease in total power causes a change in the cooling solution requirement.
- **Max Ψ_{jC}** is the thermal resistance of the die with the highest temperature. In this example, the maximum resistance belongs to the core fabric die, because it has the highest junction temperature. To check the results: $T_{J\text{-}MAX} = T_{CASE} + TTP \times \Psi_{jC}$ =88.3 +(58+7.8+7.9) × 0.091= 95° C.

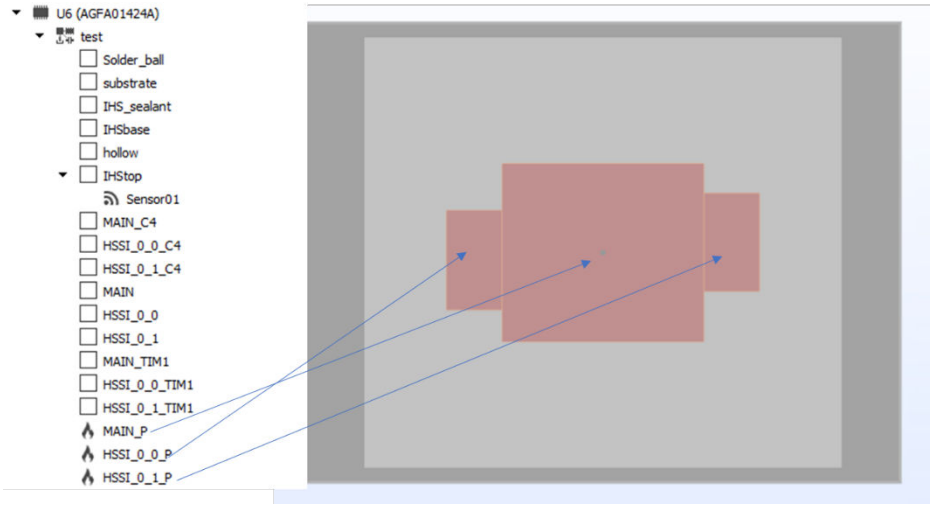
- **Ψ_{CA}** is the maximum thermal resistance of the cooling solution that satisfies the cooling requirement. In this case of our example, $T_J = T_{AMBIENT} + TTP \times (\Psi_{jC} + \Psi_{CA}) = 50 + 73.6 * (+0.091 + 0.519) = 95°C$.
- **T_{CASE}** is the temperature at the top center of the FPGA lid and may not necessarily be hottest temperature. In a computational fluid dynamic (CFD) analysis, this temperature is the best indication of whether the cooling solution meets the design requirements. Intel recommends putting a sensor in the center of the integrated heat spreader (IHS) if the compact thermal model (CTM) does not come with one.
- **Die monitor temperatures,** are the temperatures at the FPGA temperature sensors when the system is operating. These sensors may not necessarily be in the hottest locations, and therefore might report values less than the maximum value in the design. If these thresholds are exceeded, it indicates that extra cooling is required, otherwise the targeted design goal may be exceeded.

6.4. CTM Model

The compact thermal model (CTM) for the AGFA01424A Intel Agilex FPGA is shown below, with its mechanical parts listed.

The CTMs for Intel Agilex devices come with the thermal properties built-in for steady state analysis. However, there is no built-in power, therefore you must enter that from the PTC thermal page calculations.

Figure 10. CTM Model for the AGFA01424A Device



6.5. Heat Sink

FPGAs appear in a wide variety of products and layout configurations, consequently it can be difficult to find off-the-shelf heat sinks that meet all physical and performance requirements. Consequently, most applications will require custom heat sinks to maximize performance. For the purpose of our example, we have chosen an extruded aluminum heatsink generated by the CFD tool.

Attachment Force

The force with which the heat sink is attached depends on the number of pins in the package and the solder material. For more information about heat sink attachment force, refer to the article What is the maximum downward pressure that can be applied to the top of FPGA BGA packages?.

Thermal Interface Material (TIM)

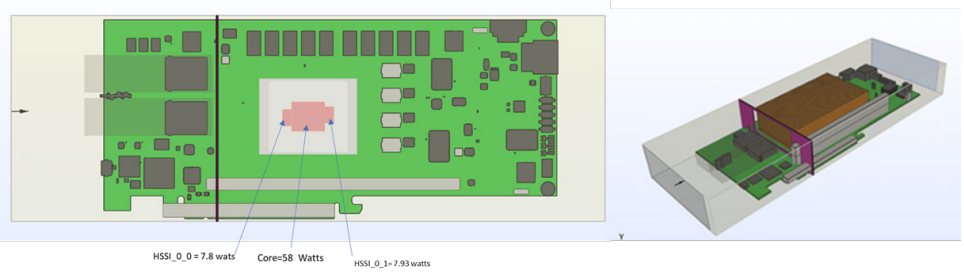
Intel does not recommend a specific thermal interface material (TIM). The choice of TIM depends on multiple factors, including TIM performance, performance over lifetime, cost, ease of application, and reworkability. Depending on the type of TIM used, the manufacturer may specify different application criteria. As a general rule, TIMs with high conductivity and low bond-line thickness perform the best. In our example we have chosen a generic TIM with 0.25 mm thickness and a thermal conductivity of 5 W(/mk).

6.6. CFD Model

After determining the necessary design parameters and obtaining the compact thermal model (CTM), the next step is to build the computational fluid dynamic (CFD) model.

The following figure shows the CFD model for this example, where the PCIe card occupies two slots, about 40 mm wide for the face bracket. Airflow to the slot is 15 CFM at 50°C.

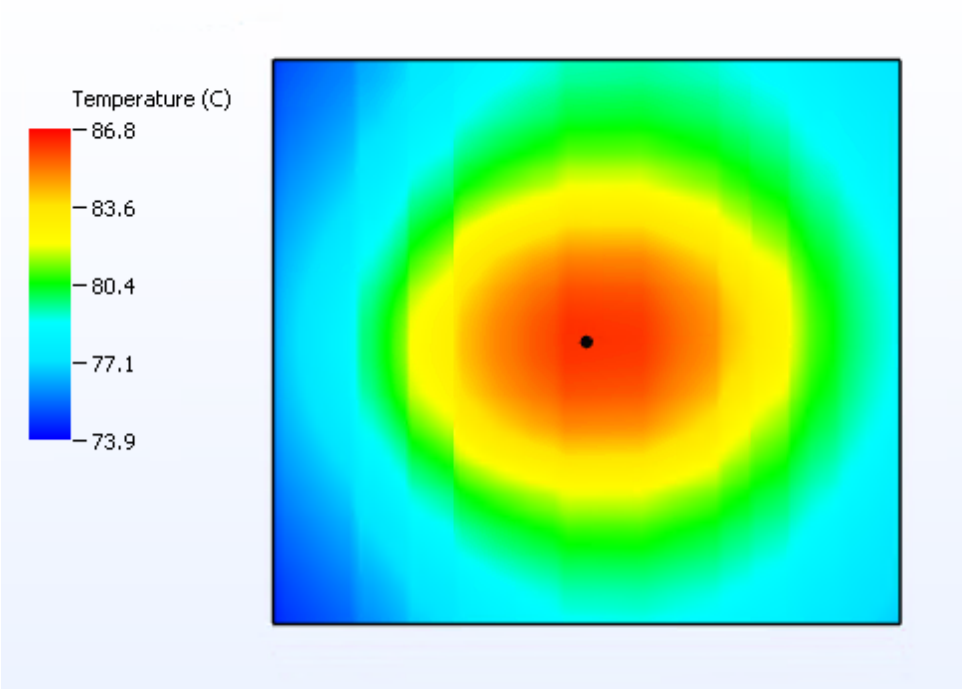
Figure 11. CFD Model Setup



CFD Results

This cooling solution would be viable if the T_{CASE} were equal to or less than 88.2°C; however, the CFD result for T_{CASE} is 86.8°C, as shown below.

Figure 12. CFD Results, Case Temperature Profile



Consequently, the T_J temperatures are less than the T_J limit entered in the Intel FPGA Power and Thermal Calculator (PTC), and the cooling solution is viable. When the temperatures are close, you can assume a linear relationship in estimating the maximum junction temperatures. So, in this case, the maximum T_J is ~88.2-86.8= 1.4°C less than the 95°C limit set in the PTC. However, the lower temperatures cause power consumption to go down, and temperatures to drop further.

CTM Case Temperature Sensor

Not all the CTMs provided have a built-in temperature sensor at the center of their integrated heat spreader (IHS). If the CTM for your project does not have a built-in temperature sensor at the center of the IHS, Intel recommends that you add one. You should place the temperature sensor at the top center of the IHS and ensure that it does not touch the heat sink.

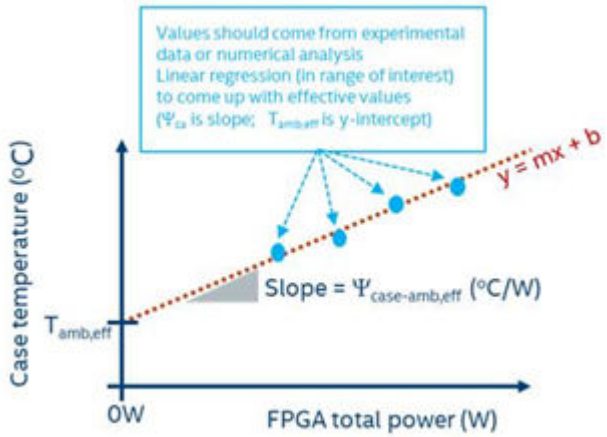
7. Example 2—Alternative Method of Analyzing Thermal Design

This example presents an alternative way of analyzing the thermal design. In this method you deduce the effective ambient temperature and Ψ_{CA} from prior knowledge, or determine them by the method described below. You then enter these two values into the Intel FPGA Power and Thermal Calculator (PTC), and have the PTC calculate the resulting junction temperatures and viability of the cooling solution.

The Thermal page of the Intel FPGA Power and Thermal Calculator (PTC) reports the required Ψ_{CA} for the FPGA; consequently, if you can determine the Ψ_{CA} for the FPGA in question, you can then readily determine whether the system has sufficient cooling. The method of entering effective Ψ_{CA} and effective ambient temperature is especially useful for large systems where you do not want to re-run your analysis or deployed systems in the field where the cooling design is fixed. For this method you can measure the effective ambient temperature and Ψ_{CA} experimentally, or determine it by CFD analysis. In either case, the result is valid only if other components of the system—especially upstream components—are powered up as they would be in the actual system, and are not subject to change. Otherwise, ensure that you perform the analysis for maximum power of the other parts and the least cooling available.

To perform the measurement or analysis keep all the transceiver powers constant but vary the core die powers by ±25% and determine the FPGA case temperature as a function of total package power. You can then use a simple linear regression to determine the $\Psi_{case\text{-}amb,eff}$ and $T_{amb,eff}$ for the FPGA.

Figure 13. Calculating Effective T_{AMB} and Ψ_{CA}

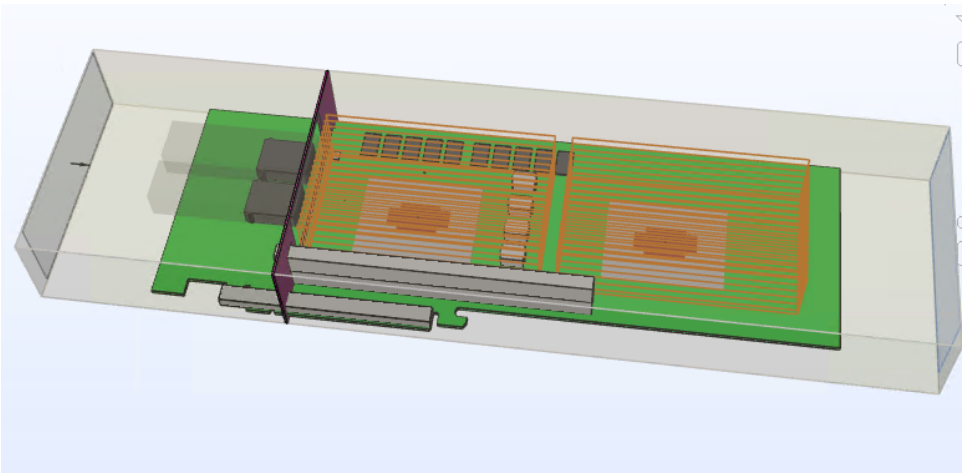


7.1. Example 2—Full Length 1 Slot PCIe with 2 FPGAs

Consider an example with a full length, half height PCIe card with two AGFA014R24A Intel Agilex FPGAs.

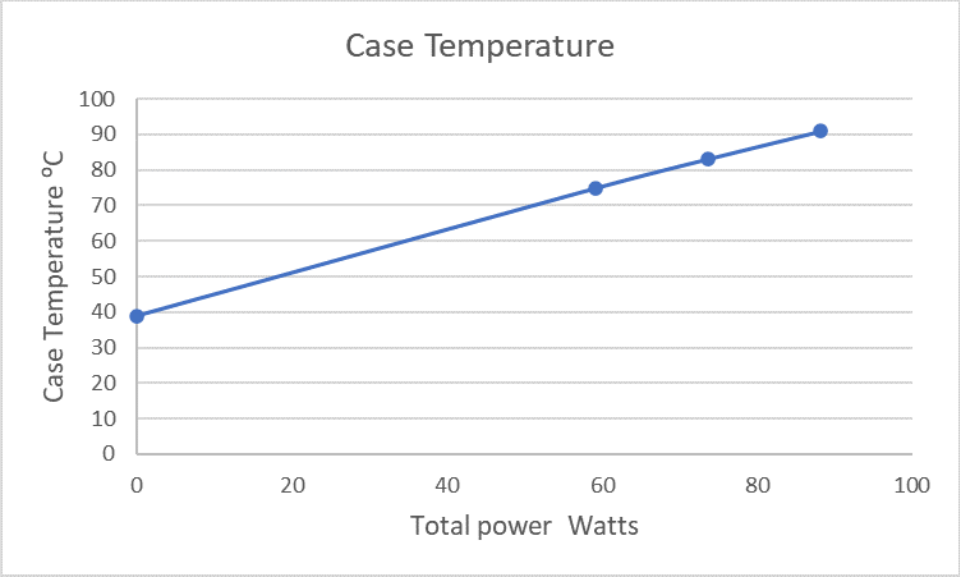
To begin with, assume the same resource selections as in the previous example; however, the second FPGA could be reprogrammed in the field, resulting in various levels of core resource usage. Our goal is to establish the effective ambient temperature and Ψ_{CA}, so that we can determine the thermal viability of future applications just by running the Intel FPGA Power and Thermal Calculator (PTC).

Figure 14. CFD Setup Example 2



For purposes of this example, let's assume that the design targets a 35°C data center environment, and airflow over the card is 20 CFM. Using the methodology described above, we perform three sets of CFD analysis, for FPGA core die powers of 43.5 W, 58 W and 72.5 W.

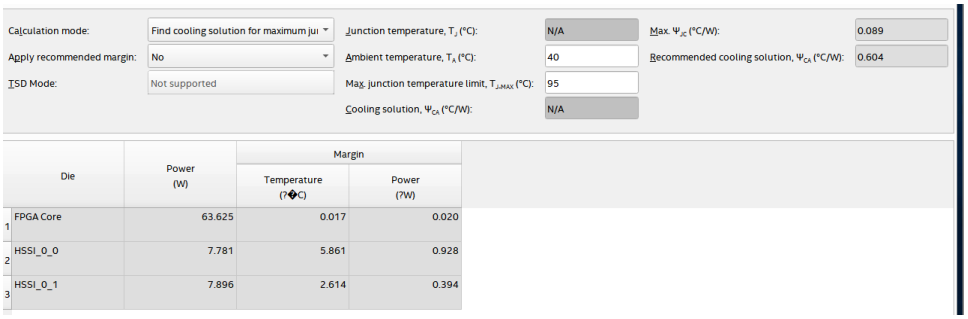
Figure 15. Example 2 Linear Regression



The above graph shows that the effective Ψ_{CA} is 0.6°C/W and the effective ambient temperature is 40ºC.

With the maximum T_J set to 95°C, if we were to change the ambient temperature to 40°C in the PTC, the Ψ_{CA} would become 0.66ºC/W , indicating that we could still add more power before reaching the FPGA's effective Ψ_{CA}. In this example the core power could be increased by almost 6 watts before Ψ_{CA} reaches its limit. Alternatively, if the solution mode is set to **Find a cooling solution for the Maximum junction temperature limit** and T_J set to 95°C and T_{AMB} to 40°C in the PTC, the Ψ_{CA} calculated is 0.66ºC/W , indicating that we could still add more power before reaching the FPGA's effective Ψ**CA**. In this example the core power could be increased by almost 6 watts before Ψ_{CA} reaches its limit.

Figure 16. Updated Thermal Parameters



7.2. Thermal Design Optimization

After you have captured your design in the Intel FPGA Power and Thermal Calculator (PTC), it is good practice to evaluate whether any thermal optimization is possible to make the cooling easier.Improved cooling can be achieved by reducing overall power consumption, or by reducing the design's maximum Ψ_{JC} value.

Power Reduction

There are two types of power consumed in an FPGA: static power and dynamic power.

- *Static power* is the power that the configured device consumes when powered up but with no user clocks operating. Static power is mainly a function of die temperature. For Intel Agilex devices, this excludes DC bias power of analog blocks, such as I/O and transceiver analog circuitry.

  Reducing junction temperatures can save power. For example, if a given design has a total static power of 14.6 watts when the maximum T_J is 95°C, and you decrease the maximum T_J, the static power also decreases, with no change to the operation of the device. However, reducing the maximum T_J requires additional cooling, such as a reduction to the ambient temperature, increased airflow, or the use of a larger heat sink. You should always consider methods of reducing static power consumption—especially when evaluating operating costs for large data centers or central offices.
- *Dynamic power* is the additional power consumed due to signal activity or toggling. For example, if you reduce the number of half ALMs or flip flops in the core die, or the clock frequency or toggle rate, the dynamic power goes down. Such action may not always be possible, but you should consider it, especially for dies that seem to be the limiting factor in the cooling system.

Transceiver Channel Spreading

Intel Agilex devices have transceiver dies with either 16 channels or 24 channels. If the channel selection can be done manually then it is possible to reduce the power dissipation by physically spreading the channels on the tile. Simply put, fewer contiguous channels use less power, have lower local power density (power/area), and are easier to cool.

For example. the table below shows an E-Tile with 14 channels but different placement. As shown, E-Tile 3 has the most widespread placement and therefore the lowest Ψ_{JC}, which translates to operating at almost 8°C lower temperature in a 100 watt device, under the same cooling condition as the other two.

Table 6. Transceiver Channel Placement Impact on Thermal Behavior

XCVR Die ID	Starting Channel Location	Number of Channels	Op Mode	Data Rate	Thermal Power	Ψ_{JC} °C/W	Temperature Difference for a 100 watt device
E-Tile 1	5	14	TX	28000	9.03	0.334	7.7
E-Tile 2	0	14	TX	28000	9	0.325	6.8
E-Tile 3	0	2	TX	28000	8.871	0.257	
	3	2	TX	28000			

continued...

XCVR Die ID	Starting Channel Location	Number of Channels	Op Mode	Data Rate	Thermal Power	Ψ_{JC} °C/W	Temperature Difference for a 100 watt device
	6	2	TX	28000			
	9	2	TX	28000			
	12	2	TX	28000			
	15	2	TX	28000			
	18	2	TX	28000			

It may not always be possible to optimize channel placement, due to design constraints and requirements; however, you should consider doing so whenever possible.

8. Document Revision History for AN 944: Thermal Modeling for Intel Agilex FPGAs with the Intel FPGA Power and Thermal Calculator

Document Version	Intel Quartus Prime Version	Changes
2021.03.29	21.1	Initial release.