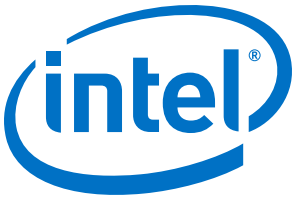

AN 932: Flash Access Migration Guidelines from Control Block-Based Devices to SDM-Based Devices

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Contents

1. Flash Access Migration Guidelines from Control Block-Based Devices to SDM-Based Devices

1.1. Introduction

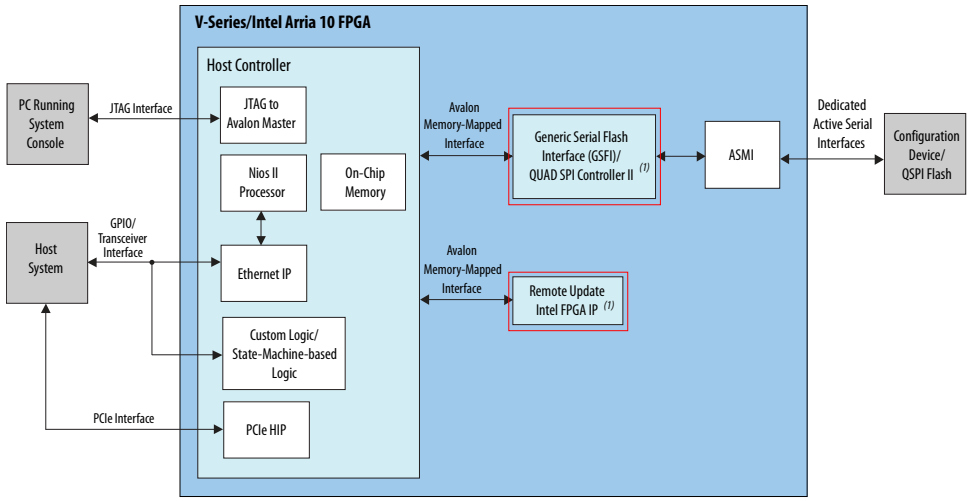
The flash access migration guidelines provide an idea on how you can implement a design with flash access and Remote System Update (RSU) operation on V-series devices, Intel® Arria® 10, Intel Stratix® 10, and Intel Agilex™ devices. These guidelines can also help you migrate from control block-based design to Secure Device Manager (SDM)-based design with flash access and RSU operation. Newer devices such as Intel Stratix 10 and Intel Agilex use SDM-based architecture with different flash access and remote system update when compared to the V-series and Intel Arria 10 devices.

1.2. Migration from Control Block-Based to SDM-Based Devices in Flash Access and RSU Operation

1.2.1. Control Block-Based Devices (Intel Arria 10 and V-Series Devices)

The following figure shows the IPs used in flash access and remote system update operation on V-series and Intel Arria 10 devices, as well as the interfaces of each IPs.

Figure 1. Block Diagram of Control Block-based Devices (Intel Arria 10 and V-Series Devices)



Note:
1. You can only use the appropriate IP blocks after you migrate from control block-based devices to SDM-based devices. Refer to Figures 2, 3, and 4 for more details.

You can use the Generic Serial Flash Interface Intel FPGA IP and QUAD Serial Peripheral Interface (SPI) Controller II to perform the flash access, similarly the Remote Update Intel FPGA IP is used to perform the RSU operation. Intel recommends that you use the Generic Serial Flash Interface Intel FPGA IP as this IP is newer and can be used with any quad serial peripheral Interface (QSPI) flash devices.

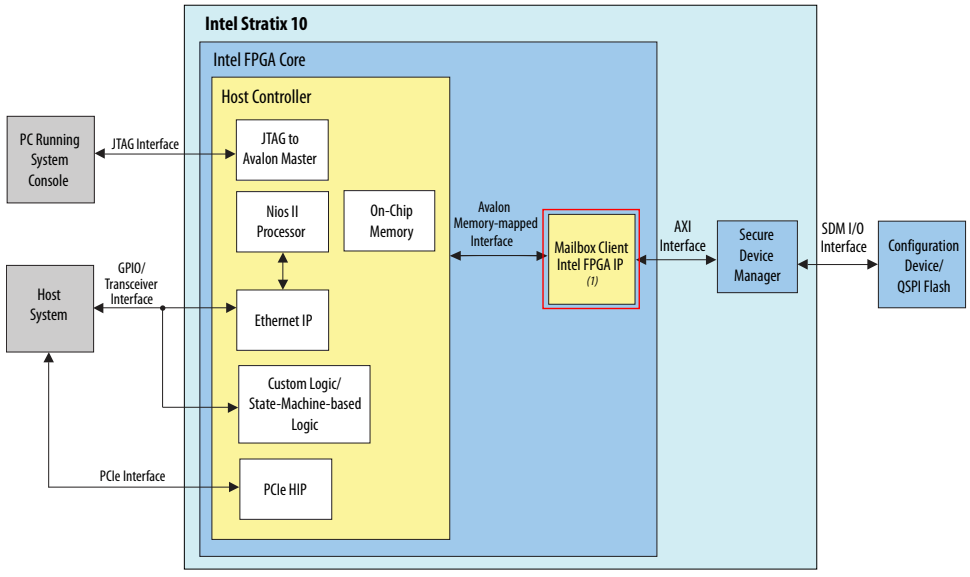
The flash devices can be connected to either a dedicated Active Serial (AS) pins or the general purpose I/O (GPIO) pins. If you want to use the QSPI flash devices for FPGA configuration and to store user data, the QSPI device must be connected to the dedicated active serial memory interface (ASMI) pin. In an active serial configuration, the MSEL pin setting is sampled when the FPGA is powered up. The control block receives QSPI flash data from the configuration devices and configures the FPGA.

1.2.2. SDM-Based Devices (Intel Stratix 10 and Intel Agilex Devices)

There are three ways to access the QSPI flash in SDM-based devices when you migrate from control block-based devices in flash access and remote system update. Intel recommends that you use the Mailbox Client Intel FPGA IP for both flash access and remote system update, as shown in the following figure.

When the configuration flash is connected to the SDM I/O pins, Intel also recommends that you use the Mailbox Client Intel FPGA IP.

Figure 2. Accessing QSPI Flash and Updating Flash Using Mailbox Client Intel FPGA IP (Recommended)



Note:
1. You can only use the appropriate IP blocks after you migrate from control block-based devices to SDM-based devices.

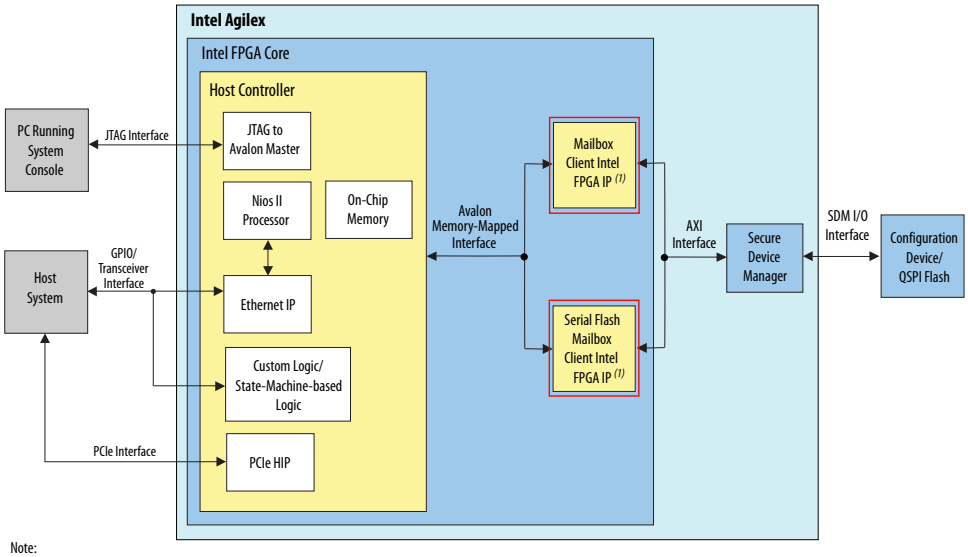
You can use the Mailbox Client Intel FPGA IP to access the QSPI flash which is connected to the SDM I/O and perform the remote system update in the Intel Stratix 10 and Intel Agilex devices. Commands and/or configuration images are sent to the host controller. The host controller then translates the command into Avalon® memory-mapped format and sends it to the Mailbox Client Intel FPGA IP. The Mailbox Client Intel FPGA IP drives the commands/data and receives the responses from the SDM. The SDM writes the configuration images to the QSPI flash device. The Mailbox

Client Intel FPGA IP is also an Avalon memory-mapped slave component. The host controller can be an Avalon master, such as JTAG master, a Nios® II processor, PCIe, a custom logic, or Ethernet IP.

You can use the Mailbox Client Intel FPGA IP to command the SDM to perform reconfiguration with the new/updated image in QSPI flash devices. Intel recommends that you use the Mailbox Client Intel FPGA IP in new designs because this IP can access QSPI flash and perform RSU operation. This IP is also supported in both Intel Stratix 10 and Intel Agilex devices, which eases design migration from Intel Stratix 10 to Intel Agilex devices.

Figure 3. Accessing QSPI Flash and Updating Flash Using Serial Flash Mailbox Client Intel FPGA IP and Mailbox Client Intel FPGA IP

Note: Only applicable for Intel Stratix 10 devices. Serial Flash Mailbox Intel FPGA IP is not supported in Intel Agilex devices.



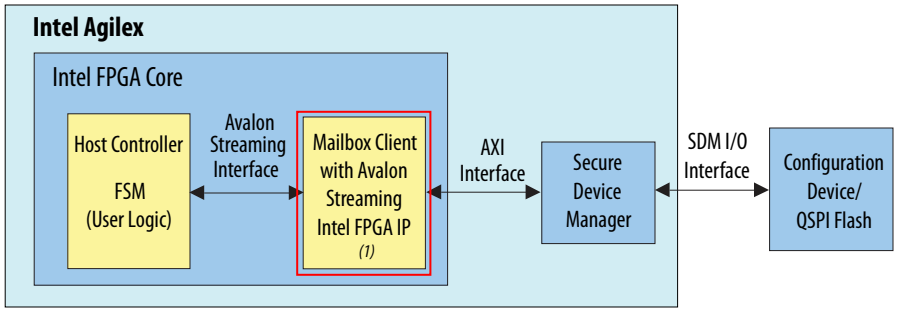
Note:
1. You can only use the appropriate IP blocks after you migrate from control block-based devices to SDM-based devices.

You can only use the Serial Flash Mailbox Client Intel FPGA IP to access QSPI flash connected to SDM I/O in the Intel Stratix 10 devices. Commands and/or configuration images are sent to the host controller. The host controller then translates the command into Avalon memory-mapped format and sends it to the Serial Flash Mailbox Client Intel FPGA IP. The Serial Flash Mailbox Client Intel FPGA IP then sends the commands/data and receives responses from the SDM. The SDM writes the configuration images to the QSPI flash device. The Serial Flash Mailbox Client Intel FPGA IP is an Avalon memory-mapped slave component. Hence, the host controller can be an Avalon master, such as a JTAG master, Nios II processor, PCI Express (PCIe), a custom logic, or Ethernet IP.

The Mailbox Client Intel FPGA IP is required to perform remote system update operation. Hence, Serial Flash Mailbox Client Intel FPGA IP is not recommended in newer designs as it only supports Intel Stratix 10 devices and can only be used to access QSPI flash devices.

Figure 4. Accessing QSPI Flash and Updating Flash Using Mailbox Client Intel FPGA IP with Avalon Streaming Interface

Note: Only applicable for Intel Agilex devices.



Note:
1. You can only use the appropriate IP blocks after you migrate from control block-based devices to SDM-based devices.

The Mailbox Client with Avalon Streaming Interface Intel FPGA IP provides a communication channel between your custom logic and the secure device manager (SDM) in Intel Agilex. You can use this IP to send command packets and receive response packets from the SDM peripheral modules, including QSPI. The SDM writes the new images to the QSPI flash device and then reconfigures the Intel Agilex device from the new or updated image.

The Mailbox Client with Avalon Streaming Interface Intel FPGA IP uses the Avalon streaming interface. You must use a host controller with Avalon streaming interface to control the IP. The Mailbox Client with Avalon Streaming Interface Intel FPGA IP has faster data streaming than the Mailbox Client Intel FPGA IP. However, this IP does not support Intel Stratix 10 devices, which means you cannot migrate your design directly from Intel Stratix 10 to Intel Agilex devices.

Related Information

- Mailbox Client Intel FPGA IP User Guide
- Serial Flash Mailbox Client Intel FPGA IP User Guide
- Mailbox Client with Avalon Streaming Interface Intel FPGA IP User Guide

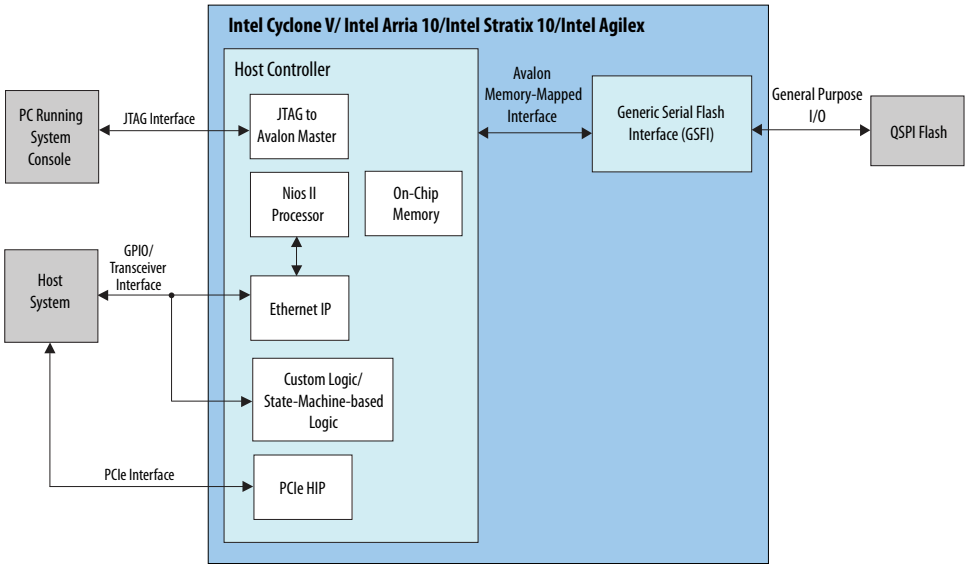
1.2.2.1. Comparison between Serial Flash Mailbox, Mailbox Client and Mailbox Client with Avalon Streaming Interface Intel FPGA IPs

The following table summarizes the comparison between each of the IPs.

	Mailbox Client with Avalon Streaming Interface Intel FPGA IP	Serial Flash Mailbox Client Intel FPGA IP	Mailbox Client Intel FPGA IP
Supported Devices	Intel Agilex	Intel Stratix 10 only	Intel Agilex and Intel Stratix 10
Interfaces	Avalon streaming interface	Avalon memory-mapped interface	Avalon memory-mapped interface
Recommendations	Host controller which uses Avalon streaming interface to stream data.	Host controller which uses Avalon memory-mapped interface to perform read and write.	• Host controller which uses Avalon memory-mapped interface to perform read and write. • Recommended to use this IP in Intel Stratix 10 devices. • Easy to migrate from Intel Stratix 10 to Intel Agilex devices.
Data Transfer Speed	Faster data streaming than Serial Flash Mailbox Client Intel FPGA IP and Mailbox Client Intel FPGA IP.	Slower data streaming than Mailbox Client with Avalon Streaming Interface Intel FPGA IP.	Slower data streaming than Mailbox Client with Avalon Streaming Interface Intel FPGA IP.

1.3. Using GPIO as Interface for Accessing Flash Devices

Figure 5. Accessing QSPI Flash



You can port over design in control block-based devices to SDM based devices directly if the design is using Generic Serial Flash Interface Intel FPGA IP with exported flash pin to GPIO.

In some rare cases, the QSPI flash device is connected to GPIO pin in FPGA. The QSPI flash device will only be used as a general purpose memory storage when it is connected to GPIO. The flash device can be accessed through the Generic Serial Flash Interface Intel FPGA IP (recommended) or Generic QUAD SPI Controller II Intel FPGA IP by selecting the option to export the SPI pin to GPIO.

In the Intel Stratix 10 and Intel Agilex devices, you can connect the flash devices to GPIO pin in the FPGA to use as general purpose memory storage as well. However, please take note that the parameter setting enable SPI pin interface must be enabled in the Generic Serial Flash Interface Intel FPGA IP when you are using Intel Stratix 10 and Intel Agilex devices to prevent error during compilation. This is because there is no dedicated Active Serial interface available in the Intel Stratix 10 and Intel Agilex devices. For configuration purpose in these devices, you must connect the flash devices to the SDM I/O as described in the *SDM-based Devices (Intel Stratix 10 and Intel Agilex Devices)* section.

Related Information

SDM-Based Devices (Intel Stratix 10 and Intel Agilex Devices) on page 4

1.4. Supported QSPI Devices Based on Controller Type

The following table summarizes the supported flash devices based on the Generic Serial Flash interface Intel FPGA IP and Generic QUAD SPI Controller II Intel FPGA IP.

Device	IP	QSPI Devices
Cyclone® V, Intel Arria 10, Intel Stratix 10[(1)], Intel Agilex[(1)]	Generic Serial Flash Interface Intel FPGA IP	All QSPI devices
Cyclone V, Intel Arria 10, Intel Stratix 10[(1)], Intel Agilex[(1)]	Generic QUAD SPI Controller II Intel FPGA IP	• EPCQ16 (Micron*-compatible) • EPCQ32 (Micron*-compatible) • EPCQ64 (Micron*-compatible) • EPCQ128 (Micron*-compatible) • EPCQ256 (Micron*-compatible) • EPCQ512 (Micron*-compatible) • EPCQL512 (Micron*-compatible) • EPCQL1024 (Micron*-compatible) • N25Q016A13ESF40 • N25Q032A13ESF40 • N25Q064A13ESF40 • N25Q128A13ESF40 • N25Q256A13ESF40 • N25Q256A11E1240 (low voltage) • MT25QL512ABA • N2Q512A11G1240 (low voltage) • N25Q00AA11G1240 (low voltage) • N25Q512A83GSF40F • MT25QL256 • MT25QL512 • MT25QU256 • MT25QU512 • MT25QU01G

For more information on the flash devices supported by the Serial Flash Mailbox and Mailbox Client Intel FPGA IPs, refer to the *Intel Supported Configuration Devices* section in the *Device Configuration - Support Center* page.

Related Information

Intel Supported Configuration Devices, Device Configuration - Support Center

(1) For Intel Stratix 10 and Intel Agilex devices, you must enable the SPI pin interface.

1.5. Document Revision History for AN 932: Flash Access Migration Guidelines from Control Block-Based Devices to SDM-Based Devices

Document Version	Changes
2020.12.21	Initial release.