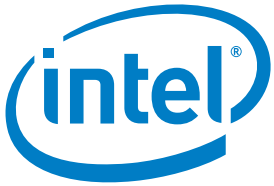


Application Note AN 920:
Input Decoupling of Power System

Contents

1. Introduction

Designing efficient power systems in modern electronics is dominated by the usage of DC/DC switching converters due to their high conversion efficiency. The high efficiency is achieved through high switching speeds across low resistance power transistors. DC/DC converters have been improving year after year with technology pushing the boundaries of physics. Often, pushing towards these boundaries can cause unwanted side effects and good system designers must pay attention to them in order to minimize the negative aspects. Switching noise caused by DC/DC buck convertors is a well-known side effect and has been documented for as long as DC/DC switching converters have been in usage. In modern electronics where systems require many power rails at various voltages and current levels, it is important to understand how switching noise can be compounded within a system and cause problems that are not normally seen on simpler systems with fewer rails and lower power consumption. When there are many rails, the printed circuit board (PCB) design of the power rails become more complex and routing traces can contribute to equivalent series resistance (ESR) and equivalent series inductance (ESL). These parasitic elements can increase switching noise and degrade performance. In attempt to mitigate the switching noise, decoupling capacitors are used, but often without consideration for their derating due to voltage bias, temperature change as well as aging over time. These real world, analog power issues can combine to create power system problems that can lead to initial power up failures as well as reliability failures over time. Given the issues at hand, it is important to understand how the problems occur and learn how to mitigate them in a good power system design.

2. General Discussion

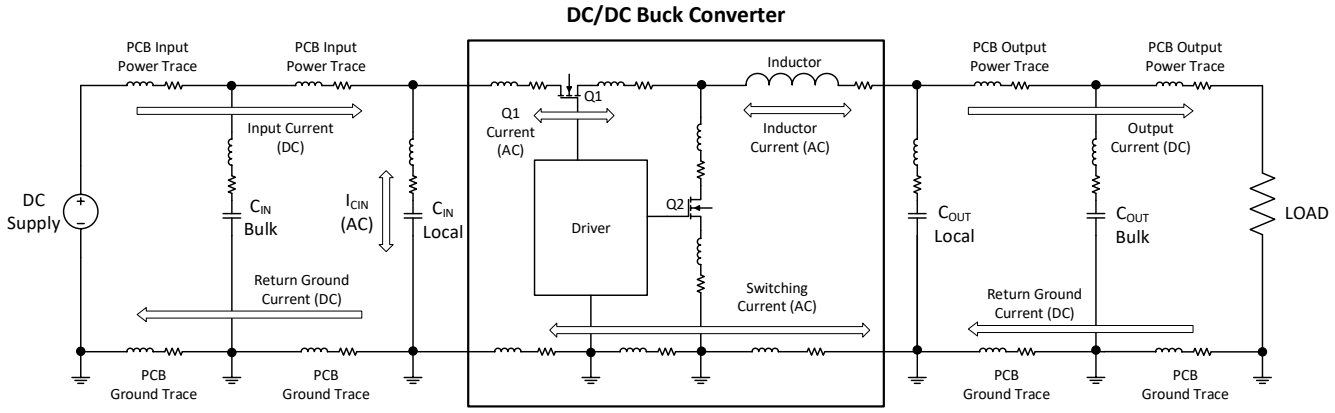


Figure 1. Buck Converter with Parasitic Resistance and Inductance

DC/DC Switching Converter Overview

As shown in Figure 1, the DC/DC switching converter is shown with the parasitic resistance and inductance that is not present on a typical design schematic, yet they exist on the system board. This certainly complicates things, but in order to address it, it is important to understand how they affect the circuitry. First, let's examine where the input switching ripple is coming from.

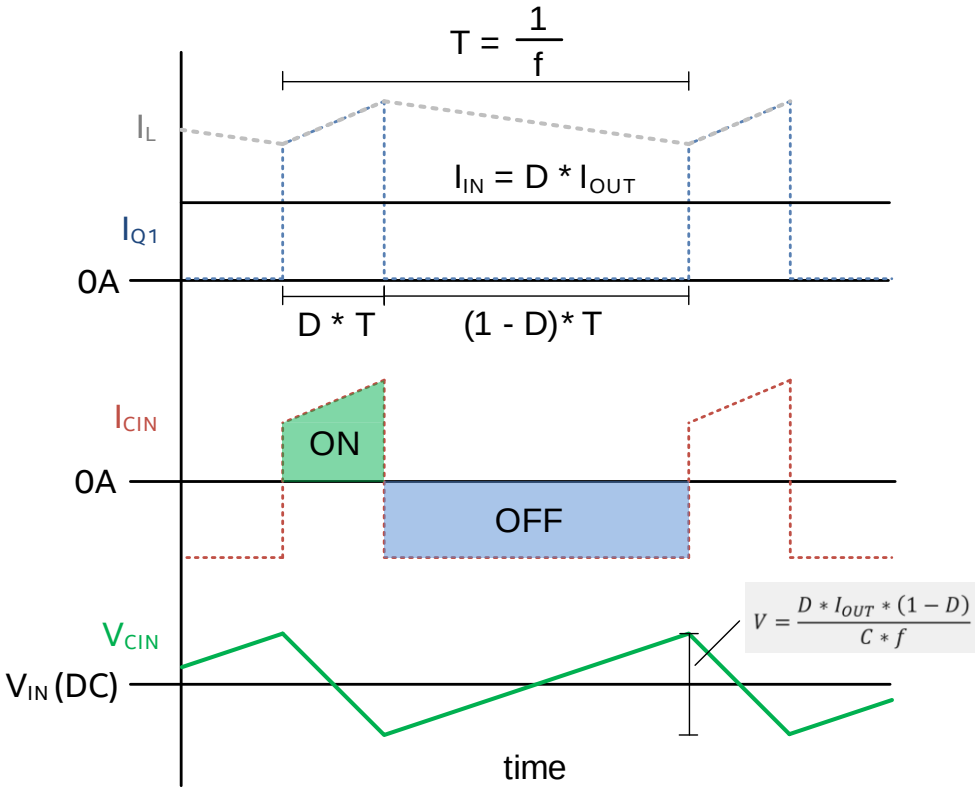


Figure 2. DC/DC Buck Converter Ideal Switching Waveforms

Figure 2 shows the current waveforms with respect to time of a typical DC/DC switching converter. Such waveforms are standard for the buck topology and are derived from the switching mechanism of Q1 and Q2 turning on and off. The input current for a switching buck regulator is discontinuous, meaning when the Q1 transistor turns on, current flows from input through the inductor into the output and when the Q1 transistor turns off, current stops flowing from input to output. The energy stored within the inductor keeps the output voltage up, while Q1 is turned off. This switching mechanism allows the buck regulator to conserve energy without burning power through resistive elements when converting from a high input voltage to a low output voltage. If Q1 turns on more often, then the input is connected more often to the output therefore raising the average output voltage. Conversely, if the Q1 turns off more often, then the average output voltage will be lower. This ideal scenario can be

expressed by the direct relationship that V_{OUT} is equal to V_{IN} times the ratio of how often the Q1 transistor turns on for a given period, called the duty cycle (D).

$$V_{OUT} = V_{IN} * D \quad (1)$$

In the real application, there will be some power loss; therefore, the duty cycle must be slightly higher to account for those losses, depending on the efficiency (η) of the converter. Since the efficiency of buck regulators are generally high, the duty cycle (D) can be considered V_{OUT}/V_{IN}.

$$V_{OUT} = V_{IN} * D * \eta \quad (2)$$

$$D = \frac{V_{OUT}}{V_{IN} * \eta} \quad (3)$$

Input Capacitor Voltage Ripple (Ideal)

The input ripple of the buck regulator comes from the charging and discharging of the input filter capacitor. The amount of charge (Q) a capacitor holds are directly related to its voltage (V) and capacitance (C), as shown in equation (4).

$$Q = V * C \quad (4)$$

When charging or discharging, the amount of charge moving in and out of a capacitor is equal to the current (I) times the time (t).

$$Q = I * t \quad (5)$$

As shown in Figure 2, when the Q1 transistor turns on, the current leaving the input capacitor is shown to increase instantaneously to the inductor current level. During this time, the input capacitor supplies the energy and is therefore discharging. When the Q1 transistor turns off, the input current supplied by the capacitor abruptly stops and the input capacitor gets recharged by the current from the DC power supply. This charging and discharging of the input capacitor create an input voltage change, which can be calculated. To do so, we first need to know the average input current (I_{IN}), which can obtain if we know the output voltage (V_{OUT}), output current (I_{OUT}) and the efficiency (η) of the buck converter.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} * I_{OUT}}{V_{IN} * I_{IN}} \quad (6)$$

$$I_{IN} = \frac{V_{OUT} * I_{OUT}}{V_{IN} * \eta} \quad (7)$$

$$I_{IN} = I_{OUT} * D \quad (8)$$

The efficiency is just the output power (P_{OUT}) divided by the input power (P_{IN}), shown in equation (6). With some algebra, we can deduce that the average input current (I_{IN}) is equal to I_{OUT} times D. Note that since the input current to the buck is discontinuous, we need to know the average input current so we can understand why the switching mechanism generates voltage ripple.

Since the average input current is known, we can deduce that during the on-time, shown by the green shaded area in Figure 2, the Q1 current is higher than the average current; therefore, more charge leaves the input capacitor. This will cause a drop in input voltage. Conversely, during the off-time, shown by the blue shaded area in Figure 2, the Q1 current is lower than the average current; therefore, more charge enters the input capacitor. This will cause a rise in input voltage. The amount of voltage rise and voltage fall caused by charge leaving and entering the input capacitor can be quantified by equating equations (4) and (5).

$$Q = V * C = I_{IN} * t \qquad (4), (5)$$

$$t = (1 - D) * T \quad \rightarrow \quad t = \frac{1 - D}{f} \qquad (9)$$

$$V = \frac{Q}{C} = \frac{I_{IN} * t}{C} \quad \rightarrow \quad I_{IN} = D * I_{OUT} \qquad (10), (8)$$

$$V = \frac{I_{IN} * (1 - D)}{C * f} \quad \rightarrow \quad V = \frac{D * I_{OUT} * (1 - D)}{C * f} \qquad (11)$$

Note that in steady state, the amount of charge entering and leaving the input capacitor during each switching cycle are equal; therefore, the total charge shown by the green shaded area is equal to the blue shaded area in Figure 2. The total charge (Q) is the blue shaded area, which is the average input current (I_{IN}) times time (t). The change in voltage (V) is equal to the total charge (Q) divided by the input capacitance (C), shown by equation (10). These formulas allow us to calculate the change in voltage due to charge transfer of a switching DC/DC buck regulator. We can make some assumptions and simplify the calculations significantly to make input voltage ripple estimations. For example, if we wanted to estimate the input ripple for a given application, we can do this quickly.

Conditions:

V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 3A, C_{IN} = 22µF, f = 1MHz, η = 100% (assume D = V_{OUT} / V_{IN}).

Solve for input voltage ripple by using Equation 11.

$$V = \frac{Q}{C} = \frac{I_{IN} * t}{C} = \frac{D * I_{OUT} * (1 - D) * T}{C} = \frac{D * I_{OUT} * (1 - D)}{C * f}$$

$$V = \frac{0.5454 * 3 * 0.4545}{22\ 10^{-6} * 1 * 10^{6}} = 0.0338V = 33.8mV$$

Given the conditions above, the switching input voltage ripple for the given capacitance is around 34mV. Note that this is an ideal calculation and does not account for the ripple caused by parasitic elements in a real application.

Parasitic Resistance and Inductance (with ESR and ESL)

The previous calculations estimate the input voltage ripple based on pure capacitance alone and does not account for the capacitor's ESR and ESL nor the resistance and inductance from layout traces in an actual application. The ripple caused by the ESR and ESL is usually much higher than the voltage change caused by charging and discharging of the input capacitance. This is especially true in modern electronics where switching speed is critical for high efficiency. Figure 3 shows the input switching waveforms with the breakdown of the voltage change caused by ESR and the ESL.

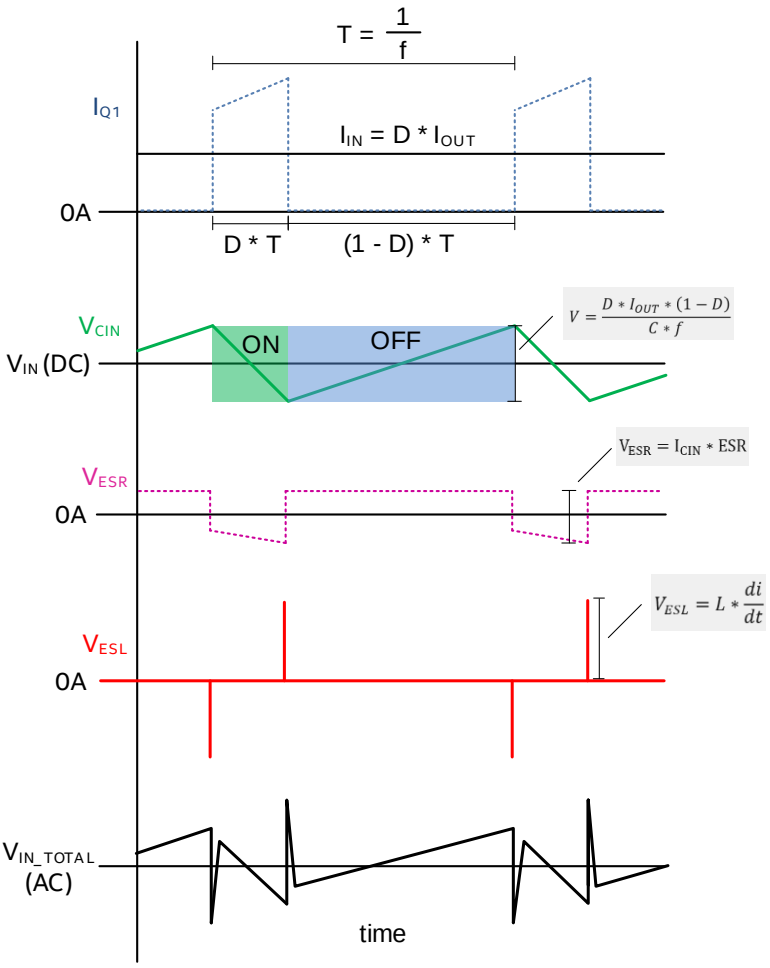


Figure 3. DC/DC Buck Converter Input Ripple Waveforms with ESR and ESL

As shown in Figure 3, when the ESR and ESL is considered, the actual input voltage ripple is much higher in amplitude. This is mainly due to the ESL. At very high frequencies, the capacitor's impedance

is high due to its own intrinsic ESL. When the Q1 transistor turns on, the instantaneous current demanded from the input is impeded by the capacitor's ESL as well as the parasitic inductance from the PCB traces. If these parasitic elements increase the impedance, then the capacitor is unable to source current to the Q1 transistor and for that brief moment in time, the voltage will drop dramatically. The ESR also influences the input voltage ripple, which is why lower ESR capacitors like ceramic capacitors are very useful for decoupling high frequencies. Figure 4 shows the impedance of various ceramic capacitors over frequency. The lowest impedance point for each ceramic capacitor is at its resonant frequency, which is usually a few milliohms. This chart shows that the lower value capacitors have higher resonant frequency and better suited to filter high frequency spikes. Unfortunately, lower value capacitors store less energy and cannot sustain high current for long, which is why using a combination of high, medium and low value ceramic capacitors will help reduce impedance across a wider frequency range.

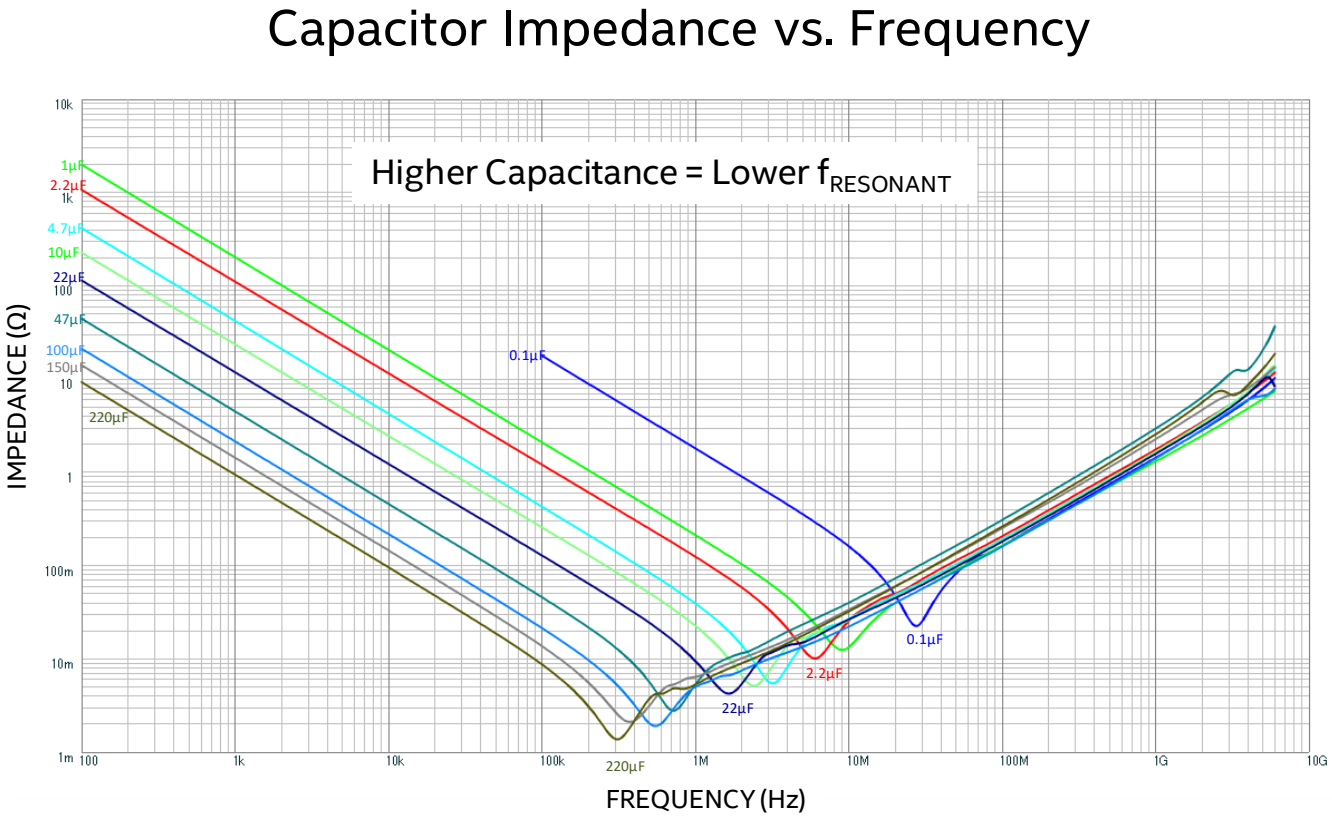


Figure 4. Capacitor Impedance vs. Frequency

The ESR and ESL changes the input ripple significantly and can cause issues in real systems. If the magnitude of the ripple is high enough to trigger a low or high voltage protection threshold (Under Voltage Lock-Out or Over Voltage Lock-Out), then the entire buck converter can shut down. This can cause a series of unfortunate events within a system. Most of the time, the ripple generated is

concerning switching noise or electromagnetic interference (EMI). Although undesirable, EMI is tolerated and managed in a good application. Figure 5 shows the actual input voltage ripple of a buck converter with the voltage deviation cause by the capacitance, the ESR and ESL illustrated. The theoretical total input voltage ripple (V_{TOTAL}), which includes the voltage change due to capacitance, ESR and ESL is also superimposed on this image for comparison.

Measured Input Capacitor Voltage Ripple

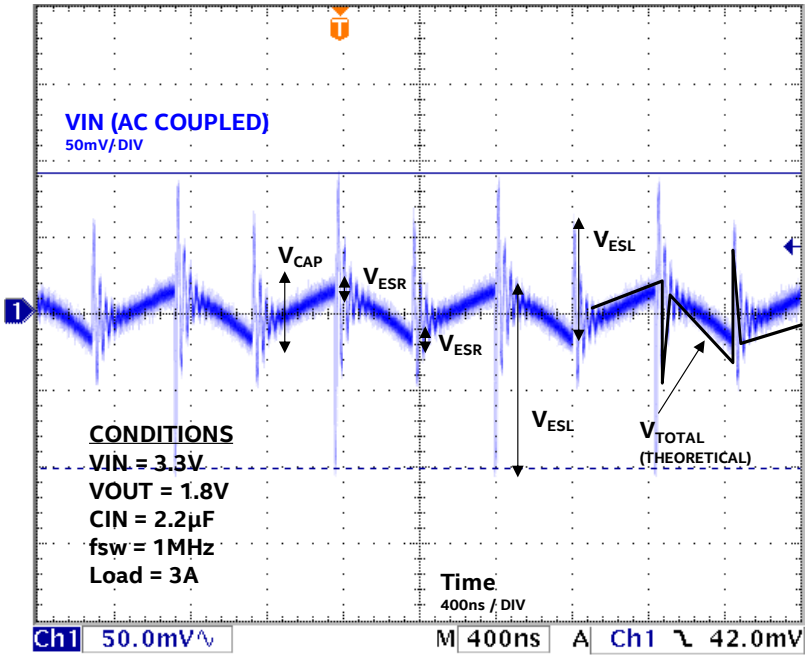


Figure 5. Measured Input Capacitor Voltage Ripple

Calculating the ripple caused by the total ESR and ESL is straight forward, but may not be accurate. This is because the parasitic elements are of very low value. It is not easy to measure the actual parasitic elements on a board. It is usually estimated. Mistakes within the estimation can cause the calculations to be way off.

The ripple caused by the ESR is simply the input capacitor current (I_{CIN}) times the ESR.

$$V_{ESR} = I_{CIN} * ESR \qquad (13)$$

The ripple caused by the ESL is equal to the change in capacitor current (di) over the change in time (dt), times the parasitic inductance. This inductance includes the intrinsic ESL of the capacitor itself as well as the parasitic inductance on the input trace connecting to the Q1 transistor.

$$V_{ESL} = ESL * \frac{di}{dt} \qquad (14)$$

As shown, the parasitic inductance is directly related to the voltage spike it causes. The higher the switching speed of the converter, the better the efficiency, but it will also cause the change in current (di) to be very high for a small change in time (dt). The trend of using highly efficient converters with high switching speeds is why good layout practice for buck converters should be followed. This starts with placing the right type of capacitors at the right place in order to minimize parasitic resistance and inductance.

Input Pi Filter

Sometimes, when EMI levels are over specifications, extra filtering may need to be implemented. One common filter configuration is the Pi filter, shown in Figure 6. The Pi filter is a commonly used filter configuration since it works in both directions by filtering voltage ripple from the supply to the input of the buck converter and vice versa. The ferrite bead has high impedance in its resistive region which is usually over a certain frequency band. This information is usually shown in the ferrite's datasheet. Below or above this region is where the ferrite bead will have low impedance and will not attenuate signals as desired. Note that since current will pass directly through the ferrite bead from the supply to the input of the buck converter, a slight DC voltage drop will be introduced due to the impedance of the ferrite bead. As a result of this voltage drop, power loss is also generated. The ferrite bead will have a current rating and should not be surpassed. For higher currents, the ferrite's physical size will increase, thus using this filter configuration will come at the cost of higher power lost, extra board space and more complexity.

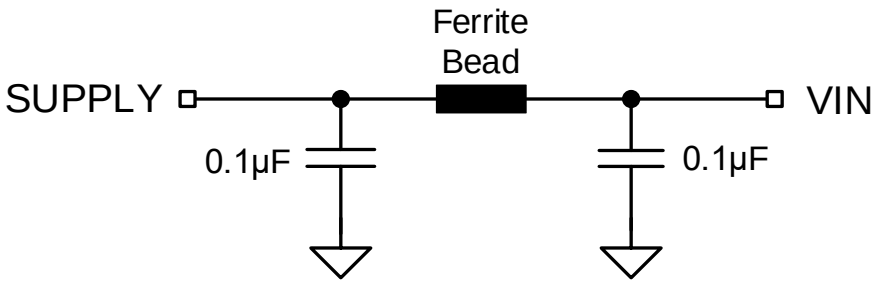


Figure 6. Input Pi Filter

Input Capacitance in PCB Layout Design

Placement of the input capacitor close to the input power pins of a buck converter is the most crucial step in buck converter PCB layout. Placing the capacitor(s) close to the input power pins will reduce parasitic resistance and inductance and minimize the input ripple. When possible, adding capacitors in parallel will not only increase capacitance but reduce the over-all impedance. Lower value capacitors have higher resonant frequency and will have lower impedance at higher frequencies. Since they are used solely to decouple higher frequencies, they must be placed close to the input pin. Placing them further away will add parasitic resistance and inductance and reduce their effectiveness. Higher value capacitance has lower resonant frequency and thus do not respond as quickly, but they have a higher

energy capacity. As a result, placing them in parallel with the lower capacitance capacitors will improve decoupling by lowering the impedance across their resonant frequency ranges. This technique of placing various capacitance values in parallel is how circuit designers combine their attributes and filter noise at various frequencies across the board.

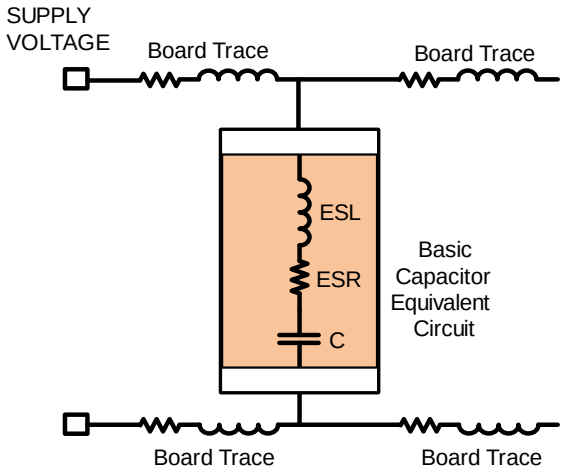


Figure 7. Input Capacitor with ESR/ESL and Parasitic Resistance/Inductance

Types of Decoupling Capacitors (Electrolytic, Tantalum and Ceramic)

There are various types of capacitors used in system level design and it is important to understand their advantage and disadvantages. The three type that will be discussed are electrolytic capacitors, tantalum capacitors and ceramic capacitors.

Electrolytic capacitors are physically bulky, but they have a high capacitance. They have much higher ESR and ESL due to their physical size and can be damaged by over-voltage or over temperature. Nonetheless, they are critical in a power system as an energy storage element. The high capacitance will help decouple for the line inductance coming from the source. Sometimes the power source is connected via long cables and they have very high inductance. It is good to have bulk electrolytic capacitors as the first filter on the system board. One thing to pay attention to is how they will be charged. Due to their high capacitance, it may be a good idea to charge these capacitors up slowly with a slew rate monitor in order to reduce high current spikes. When used properly, electrolytic capacitors offer on-board energy that can be used to source various nodes during load transients.

Tantalum capacitors are less bulky compared to electrolytic capacitors and are usually surface mounted onto the PCB. They have a lower ESR and ESL and are meant for local bulk decoupling. In applications where space constraint and high current is needed, some tantalum capacitors can fill the need for bulk capacitance. Like the electrolytic capacitors, they have a voltage tolerance rating and can be prone to damage if the voltage tolerance is breeched. Although lower and lower ESR tantalum capacitors are being manufactured, they are still not as low as modern ceramic capacitors.

Ceramic capacitors are widely used in electronics due to their size, low ESR and ESL. Ceramic capacitors come in various capacitance, size, voltage rating, dielectric and temperature rating. There are even specialized ceramic capacitors with emphasis on lower ESR and ESL by placing the terminals on the length of the package and other special surface mount construction. Despite many advantages, unlike electrolytic or tantalum capacitors, ceramic capacitors have a changing capacitance over DC Bias, temperature and time (aging). Figure 8, 9 and 10 show examples of these characteristics.

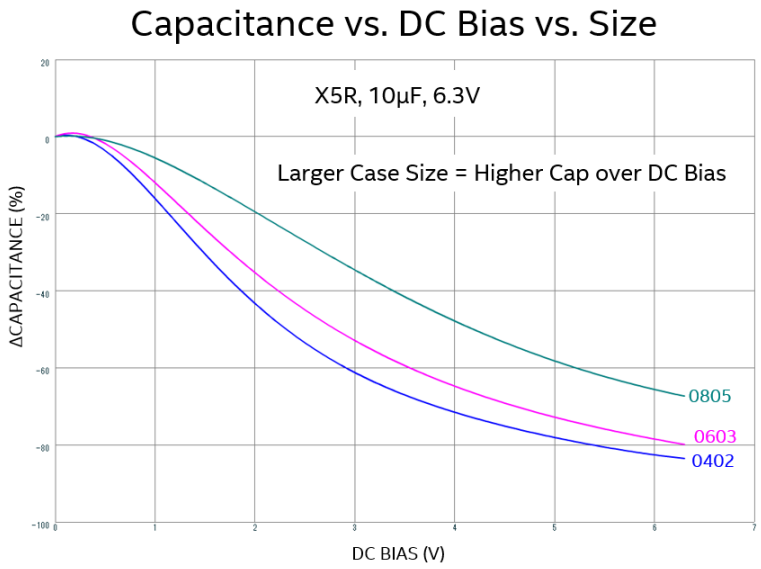


Figure 8. Change in Capacitance over DC Bias

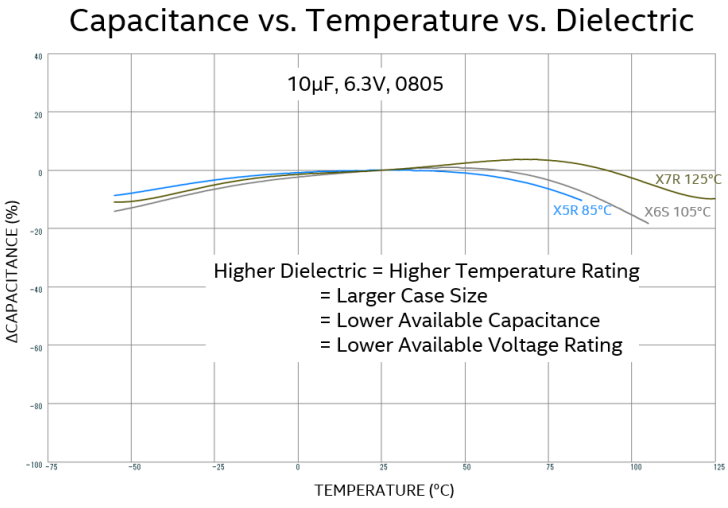


Figure 9. Change in Capacitance over Temperature

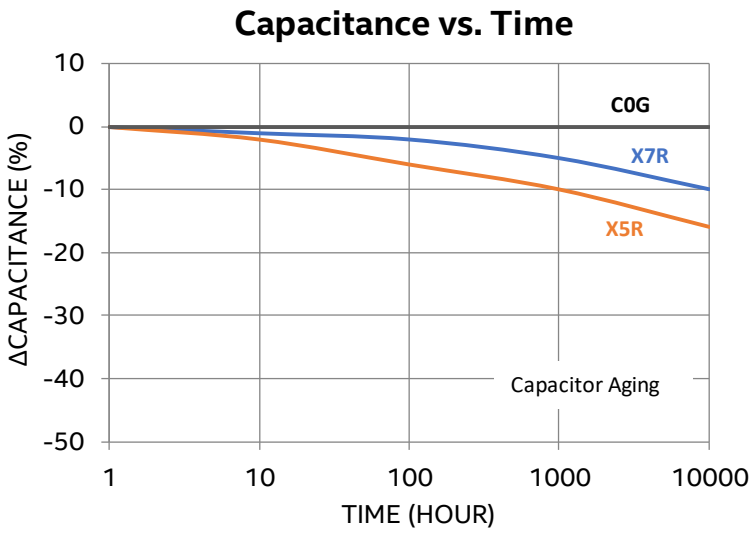


Figure 10. Change in Capacitance over Time

As shown, ceramic capacitors derate quite significantly, especially over DC Bias. That means power system designers cannot use the ceramic capacitors at face value and must always account for their derating when using them in a system. Figure 11 shows the typical power system decoupling scheme.

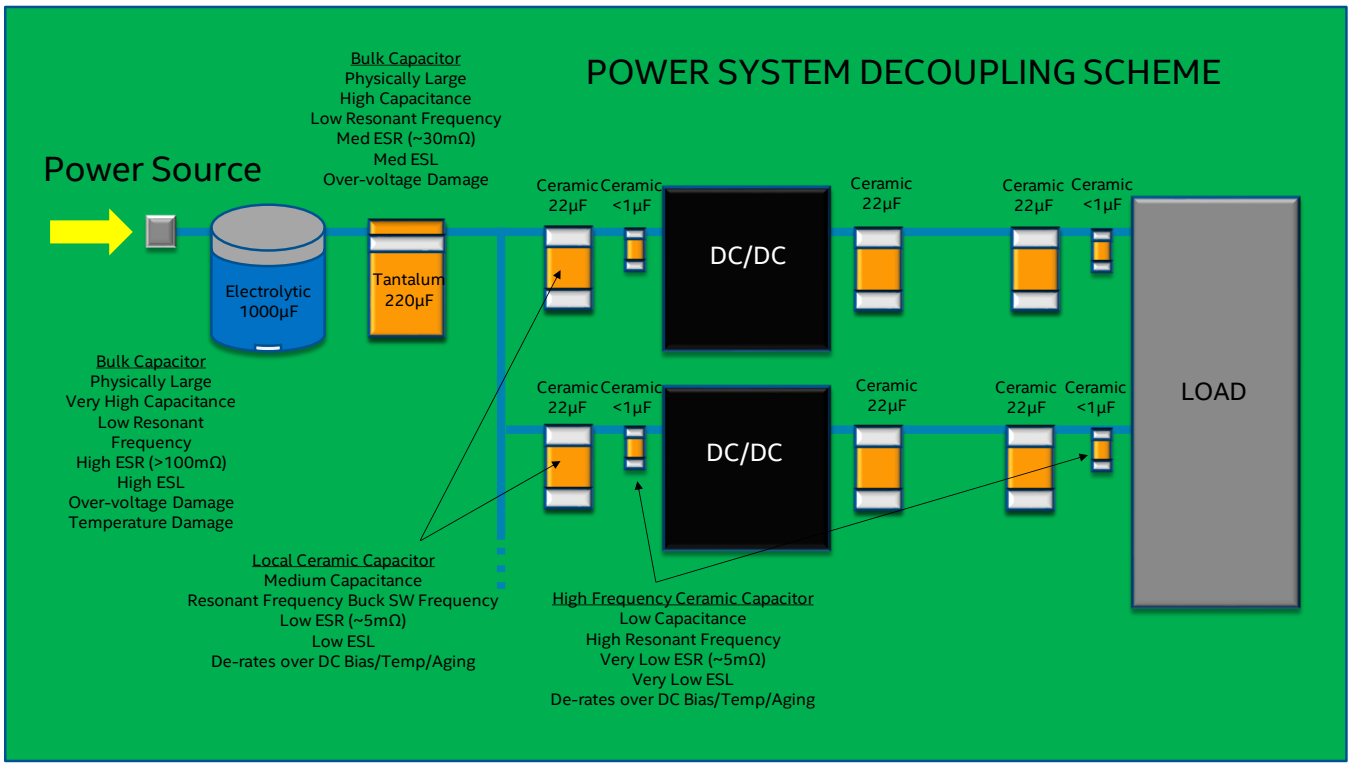


Figure 11. Typical Power System Decoupling Scheme

Due to the attributes of each of the electrolytic, tantalum or ceramic capacitors, their usage is common in the decoupling scheme shown in Figure 11. The electrolytic capacitors are used at the first stage to decouple the system board right where the power source comes in. As power is routed throughout the board, tantalums can fill the gap for bulk capacitance at various locations on the board. Finally, the ceramic capacitors are used local to the DC/DC converter. Low value ceramic capacitors are placed closer to the power input pins while high value ceramic capacitors are placed next in line. This configuration ensures that high frequency spikes are minimized and sufficient capacitance is on-board for dynamic events such as load transients. This is especially helpful when the system board has many power rails and undergoes temperature cycling with vigorous testing of the load on each power rail.

Multi-rail Power System and Load Transient

In the previous discussions, we have shown the effects of input filtering on the input voltage ripple. Minimizing ESR and ESL using good layout practice helps minimize input ripple. The discussions have so far been focused on steady-state operation, which is assuming no dynamic events are happening within the system. In the real world, that is rarely the case. This section is dedicated to the discussion regarding dynamic events such as during a load transient. Figure 12 shows an issue that happens when a system board is designed with only the minimal amount of ceramic capacitance with a typical layout that is not optimized, but not poor. The input voltage is 12V, and based on what we have covered, this causes the single 22µF ceramic capacitor to derate (can be over 50%). The system this converter is designed in may be subject to thermal cycling with some dynamic load tests on the output. In this typical scenario, the schematic will not reveal any issues, as most datasheet recommendations would have been followed, yet in real life when there is a simple 2A load step on the output, the input begins to oscillate. This type of oscillation can occur when the input line inductance is much larger than the input filter. The excess energy stored in the input line inductance is greater than the input filter can decouple for. This excess energy will easily cause the voltage to ring when the Q1 transistor of the buck converter turns on and suddenly off during each switching cycle. When the input oscillates as wildly as shown in red in Figure 12, the entire buck converter will begin to misbehave. Each cycle causes the next to be more and more inconsistent until either a protection feature is triggered, or a catastrophic event happens. In any case, the system faults and the board designer may be left without a clue.

Insufficient Input Filter with Load Transient

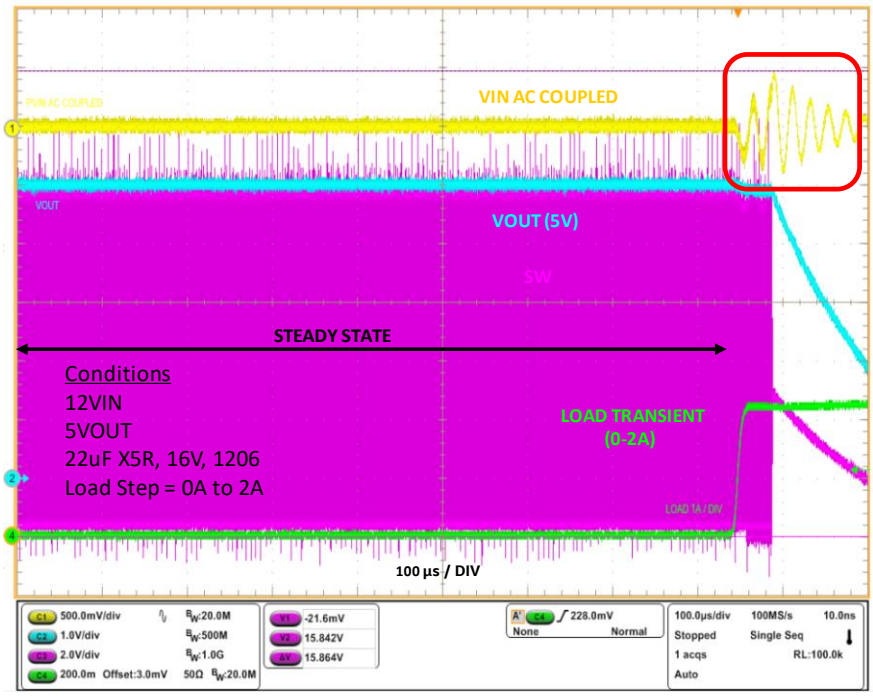


Figure 12. Insufficient Input Decoupling During Load Transient

In order to avoid such scenarios, it is important to understand what happened and to recognize the dangers of not using enough input decoupling on the system board. Minimum capacitance recommended in device datasheets are usually based on ideal conditions without extraneous elements added. Figure 13 shows the switching waveform during a dynamic event and what happens when it is compounded by multiple rails.

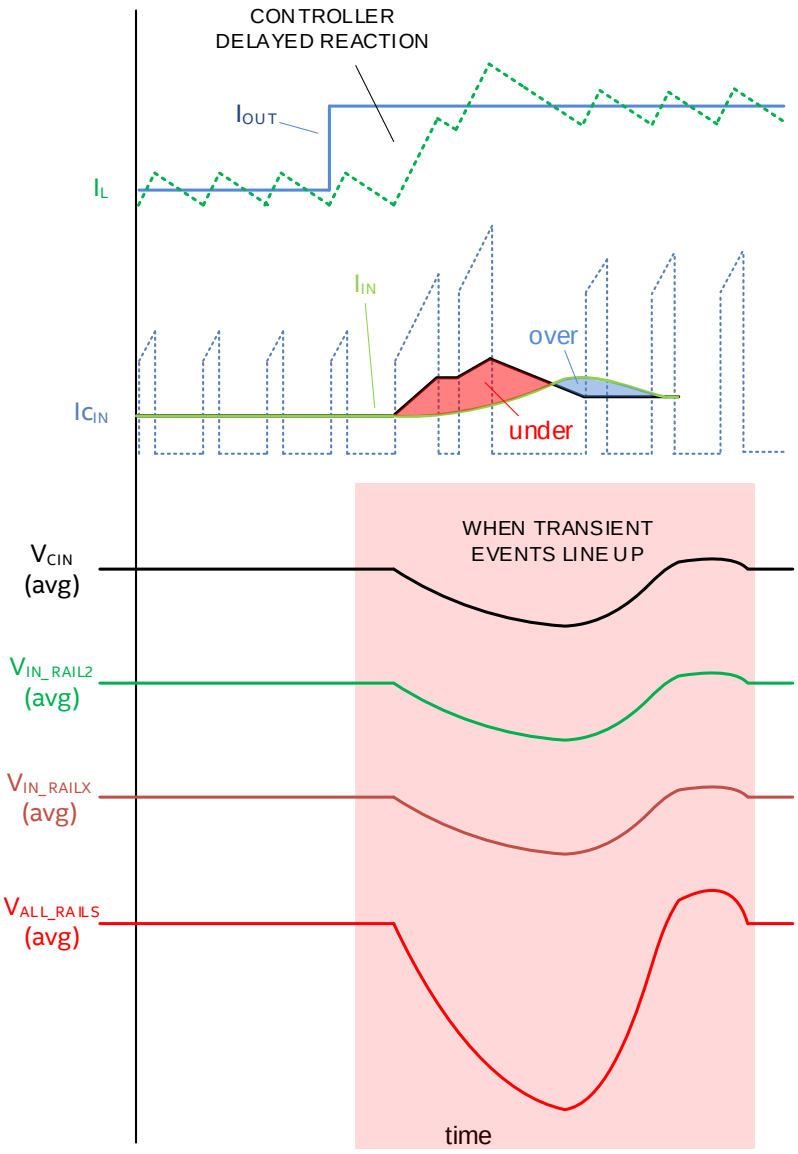


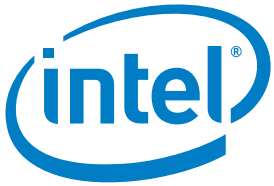
Figure 13. Line Transient on Multiple Rails

Figure 13 illustrates what might happen in a system with multiple rails under stress testing. In steady state, nothing unusual happens. When there is a load step (I_{OUT}) on the output of one rail, that rail's buck controller will not be able to react to it instantaneous. The reaction time depends on the buck controller's loop bandwidth, but assuming if it can react in a few cycles, there will still be a delay due to the slow ramping of the inductor current. This delay is why there are voltage droops on the output during load transients. This very same mechanism can also cause a voltage droop on the input. Note that the capacitor input current (I_{CIN}) rises as the duty cycle increases. However, the input current to recharge the capacitor from the supply (I_{IN}) does not follow exactly due to line inductance. This is a very important concept that should be understood. The same reason the output droops during a load

transient due to the output inductor slewing current can happen on the input due to line inductance slewing current. As shown in Figure 12, the charge discrepancy (shaded red) causes a voltage drop and the excessive charge (shaded blue) causes a voltage rise on the input capacitor. When there are multiple rails in a system undergoing stress test, the transient events of all rails can potentially line up and cause a huge spike on the input. Most of the time, stress tests are conducted in an oven and oscilloscope voltage measurements are not made throughout the process. When a fault happens, it is difficult to assess what happened. It may also be very late in the design stage to make significant changes. The line inductance prevents current from charging the input capacitors as quickly as needed. If local bulk capacitors are near, the input voltage will not drop as much and the line inductance will be negated. In order to avoid power related issues within a system, it is essential to understand the importance of input decoupling.

3. Conclusion

As modern electronics become more complex and more efficient, DC/DC converters will be there to fill the need. With all advances in technology, there are some side effects. In order to manage the EMI and build robust power systems, it is imperative that the input decoupling for each switching converter is sufficient and the power system is properly designed. The technologies used to power today's electronics are constantly improving, but the fundamentals stay the same. Knowing the inner details of power converters and how to mitigate their side effects will allow the power system designer to design robust power systems. When proper care is taken, the power system will be more reliable over time.



4. Revision History

Revision	Description	Revision Date
A	Initial release.	6/1/2020