Intel® Enpirion® Power Solutions

AN 913: Designing Multi-Phase Step Down Switching Regulators with ED8401 for Powering FPGAs and ASICs
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Introduction

Next generation FPGAs, ASICs and Memory devices demand high performance switching regulators to extract superior performance both in active state and in idle state. This requires switching power supplies powering next generation FPGAs, ASICs and Memory devices to have very low input output ripple, excellent transient performance and a small footprint while meeting the required efficiency specifications. So, designing a power supply which meets above requirements is extremely critical. This design guide highlights the methodologies to be used for designing high performance switching power supplies using Intel Enpirion multi-phase step-down controller ED8401 and 70A power stage ET6160LI.

The ED8401 is a true digital multi-phase step-down controller for non-isolated, high current DC/DC applications. A PMBus version 1.2 compliant interface provides setup, control, and telemetry. Differential remote sensing and ±0.5% set-point accuracy provides precise regulation over line, load and temperature variation to provide excellent static regulation for today’s FPGAs, ASICs, Processors, and DDR memory devices. The ED8401 offers a scalable solution by operating in 4, 3, or 2 phase modes to meet power delivery needs of various power SKUs (for example of an FPGA family).

The ET6160LI is a monolithic 70A Power Stage with integrated current and temperature monitors. The ET6160LI monolithic output stage offers high system efficiency while offering switching frequency operation of up to 1MHz. Monolithic construction provides excellent thermal impedance from junction to case top and bottom.

- Supports Wide Input Range of 4.5V to 16V
- Programmable Digital Control Loops
- Up to 70A Per Phase Current Capability
- Integrated Current Monitor (IMON)
- Actively Balanced Phase Currents
- Intel® Enpirion’s Proprietary LDMOS Technology for High Frequency Operation
- High Efficiency
- Tracking Pin to Support Complex Power Sequencing
- Input Voltage Feed-forward
- Separate TMON (Temperature Monitor) for Each Phase
- Optimized Customer configurations stored in NVM (Non Volatile Memory)
- Protection features
  - Short Circuit Protection
  - Over-Current Protection
  - Over Voltage protection (Input and Output)
  - Under Voltage protection (Input and Output)
  - Over Temperature Protection
- Small 5.0mmx5.0mmx0.9mm QFN Package (ED8401)
- Compact 5.0mm x 6.0mmx0.9mm LGA package (ET6160)
- RoHS compliance with no-EU exemptions
Figure 1. ED8401 Pin Out

Figure 2. ET6160 Pin Out
Default ED8401 Configurations

The ED8401 has six different flavors to support the power delivery needs of a wide variety of applications. Some applications may require a very small solution size with low Z height, in which case higher switching frequency is desired. Other applications may require higher efficiency to meet thermal limitations for which lower switching frequency operation is advised. Also, the load current requirement of a specific application may determine the number of phases. See the table below.

Table 1. ED8401 Flavors Available

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Configuration*</th>
<th>Package Markings</th>
<th>Package Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ED8401P01QI</td>
<td>4-Phase 500kHz</td>
<td>84011</td>
<td>5 mm x 5 mm x 0.9mm QFN40</td>
</tr>
<tr>
<td>ED8401P03QI</td>
<td>3-Phase 500kHz</td>
<td>84013</td>
<td>5 mm x 5 mm x 0.9mm QFN40</td>
</tr>
<tr>
<td>ED8401P05QI</td>
<td>2-Phase 500kHz</td>
<td>84015</td>
<td>5 mm x 5 mm x 0.9mm QFN40</td>
</tr>
</tbody>
</table>

* For alternative configurations contact Sales

The ED8401 is designed to work very closely with the power stage family from Intel Enpirion. The multi-phase controllers make use of the IMON (Current Monitor Signal) output from the power stage for current balancing and protection from over current events and shorts. This also avoids the use of complex and not very accurate DCR current sensing topology. Considering wide range of applications, NVM of the multi-phase controller ED8401 stores a default configuration which meets the requirements of most of the applications by modifying few signal components such as RTUNE (selects compensation scaling factor), RVSET (Selects output voltage) etc. Table 2 below highlights the defaults settings of ED8401.

Table 2. Warning/Fault Limit Settings – ED8401

<table>
<thead>
<tr>
<th>Specification</th>
<th>Default Setting</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Under Voltage Warning Limit</td>
<td>4.2</td>
<td>V</td>
</tr>
<tr>
<td>Input Under Voltage Fault Limit</td>
<td>3.96</td>
<td>V</td>
</tr>
<tr>
<td>Input Over Voltage Warning Limit</td>
<td>16.6</td>
<td>V</td>
</tr>
<tr>
<td>Input Over Voltage Fault Limit</td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>Input ON Level</td>
<td>4.4</td>
<td>V</td>
</tr>
</tbody>
</table>
### Default Fault Response - ED8401

<table>
<thead>
<tr>
<th>Signal</th>
<th>Fault Level</th>
<th>Default Response Type</th>
<th>Retries #</th>
<th>Default Delay to Fault</th>
<th>Delay Resolution for Setting for Delay to Fault*</th>
<th>Maximum Delay to Fault*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Over-Voltage</td>
<td>Warning</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fault</td>
<td>High Impedance</td>
<td>None</td>
<td>0</td>
<td>1.5µs or 15µs</td>
<td>0.327ms or 3.27ms</td>
</tr>
</tbody>
</table>

*** Considering the output voltage range (0.5V to 1.3V) and input voltage (4.5V to 16V) range supported, maximum duty cycle required during normal operation is understood to be less than 50%.

All the warning and fault limits can be changed as needed to suit customer requirements by using PMBus. For example, the input voltage range for an application is 10V (Min) to 14V (Max) but the default input voltage range supported by the ED8401 is 4.5V to 16V. By using PMBus, the input under voltage and over voltage warning/fault limits can be changed so the switching regulator does not operate outside the required input voltage range. Refer to [ED8401 PMBus user guide](#) for more information.
<table>
<thead>
<tr>
<th>Signal</th>
<th>Fault Level</th>
<th>Default Response Type</th>
<th>Retries *</th>
<th>Default Delay to Fault</th>
<th>Delay Resolution for Setting for Delay to Fault*</th>
<th>Maximum Delay to Fault*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Under-Voltage</td>
<td>Warning</td>
<td></td>
<td></td>
<td></td>
<td>1.5µs or 15µs</td>
<td>0.327ms or 3.27ms</td>
</tr>
<tr>
<td></td>
<td>Fault</td>
<td>High Impedance</td>
<td>None</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Over-Voltage</td>
<td>Warning</td>
<td></td>
<td></td>
<td></td>
<td>1.5µs or 15µs</td>
<td>0.327ms or 3.27ms</td>
</tr>
<tr>
<td></td>
<td>Fault</td>
<td>High Impedance</td>
<td>None</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Under-Voltage</td>
<td>Warning</td>
<td></td>
<td></td>
<td></td>
<td>1.5µs or 15µs</td>
<td>0.327ms or 3.27ms</td>
</tr>
<tr>
<td></td>
<td>Fault</td>
<td>High Impedance</td>
<td>Infinite</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over-Current</td>
<td>Warning</td>
<td></td>
<td></td>
<td></td>
<td>1.5µs or 15µs</td>
<td>0.327ms or 3.27ms</td>
</tr>
<tr>
<td></td>
<td>Fault</td>
<td>High Impedance</td>
<td>None</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over Temperature</td>
<td>Warning</td>
<td></td>
<td></td>
<td></td>
<td>5ms</td>
<td>900ms</td>
</tr>
<tr>
<td>(Controller)</td>
<td>Fault</td>
<td>Soft Off</td>
<td>Infinite</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over Temperature</td>
<td>Warning</td>
<td></td>
<td></td>
<td></td>
<td>5ms</td>
<td>900ms</td>
</tr>
<tr>
<td>(Power Train)</td>
<td>Fault</td>
<td>Soft Off</td>
<td>Infinite</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*For voltage and current signals, the resolution (step size) of 1.5µs applies up to a maximum delay of 327µs. For a delay time exceeding 327µs, the step size increases to 15µs and the maximum delay time increases to 3.27ms.

**For retries, the delay to retry time can be programmed also as per the delay to faults however the retry times are scaled to be 100 greater than Delay to Fault times.

The warning limits are used to alert (Flag) the host about a potential “Outside the Operating Zone” situation. The fault limits defined above are used to determine the response for a given fault. The ED8401 supports different response types depending on the fault detected. A “Soft-Off” response ramps the output voltage down using the falling-edge sequencer settings. The “low-impedance” response immediately turns off the top MOSFET and
enables the low-side MOSFET. The “high-impedance” response immediately turns off both the top MOSFET and low-side MOSFET. **Table 3** above summarizes the default fault responses configured in the ED8401.

**Phase Configuration Selection**

The ED8401 along with ET6160 does provide optimized power solutions for a wide range of applications based on FPGAs, ASICs, Processors and memory devices. Even though the power stage ET6160 supports a maximum continuous current of 70A, it is recommended to limit maximum continuous current per phase to 40A for optimizing power conversion efficiency and solution size. **Table 4** can be used as a guideline for selecting the number of phases required for a given application.

**Table 4. Output Current Specification and Required Number of Phases**

<table>
<thead>
<tr>
<th>Output Current Specification (Amps)</th>
<th>No. Of Phases Required</th>
<th>Recommended Part Number (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>160</td>
<td>4</td>
<td>ED8401P01QI (500kHz)</td>
</tr>
<tr>
<td>120</td>
<td>3</td>
<td>ED8401P03QI (500kHz)</td>
</tr>
<tr>
<td>80</td>
<td>2</td>
<td>ED8401P05QI (500kHz)</td>
</tr>
</tbody>
</table>

Although the table mentioned above can be used as a guideline, other system level constraints (Form Factor, Z Height, Thermal Dissipation etc.) may need to be considered. For example, a very thin system (with Z height requirement of less than 3mm for components) may need a three phase ED8401+ET6160 based switching regulator to support 80A output continuous current (Max Specification) contrary to the information provide in the table above. Detailed design guidelines provided below can be used for selecting various components (Inductor, Input Capacitor, Output Capacitor and other components) to meet customer’s needs.

**Detailed Design Guidelines**

The ED8401 + ET6160 solution requires additional components to generate a high performance power supply rail to power FPGAs/ASICs. The schematic of the ED8401 evaluation board with power stage ET6160 is shown below. The configuration shown is a 4 phase, 160A continuous current capable switching regulator with support for high transient load currents (80A with a slew rate of 50A/us).
Figure 4. Phase 1/4 Schematic for a 4 Phase 160A Application (Output from 0.5V to 1.3V)

Figure 5. Phase 2/4 Schematic for a 4 Phase 160A Application (Output from 0.5V to 1.3V)
Figure 6. Phase 3/4 Schematic for a 4 Phase 160A Application (Output from 0.5V to 1.3V)

Figure 7. Phase 4/4 Schematic for a 4 Phase 160A Application (Output from 0.5V to 1.3V)
Figure 8. Output Decoupling Capacitors for a 4 Phase 160A Application (Output from 0.5V to 1.3V)

16x 470μF Tantalum

8x 100μF/0805 Ceramic Local Bypass

Figure 9. Input Filter for a 4 Phase 160A Application (Output from 0.5V to 1.3V)
Switching Frequency Selection

Frequencies around 500 kHz can provide low switching loss and high efficiency at the price of slower transient response as larger inductors are needed and the control loop bandwidth must be set lower than it otherwise would be at higher frequencies. Similarly, higher switching frequencies around 1 MHz suffer from greater switching loss but offer faster transient response. To support wide variety of applications, the default switching frequency option available with ED8401 is 500 kHz. If the system level requirements demand a very small footprint (Lower Z height) power solution, higher switching frequency is recommended. Please contact sales for more information on high frequency options. If the need is to find a solution with focus on both efficiency and solution size then it is advised to select 500 kHz switching frequency.

Inductor Design and Selection

In a multi-phase step-down switching regulator, each phase consists of an inductor and a power stage. These phases are connected in parallel and share the same input and output capacitors. The power stage recommended is ET6160. While choosing an inductor, four critical parameters (Inductance, Saturation Current, RMS Current and DCR) are usually considered. In applications requiring a very thin form factor, Z height may need to be considered as well.

In a step-down switching regulator, the inductance can be calculated using the equation given below.

\[ L = \frac{V_{OUT} \times (1 - D)}{F_{SW} \times I_{RIPPLE}} \]

**VOUT** – Switching Regulator Output Voltage

**D** – Duty Cycle

**FSW** – Switching Frequency of Operation

**IRIPPLE** – Ripple Current Allowed (Desired). Higher IRIPPLE requires lower inductance but results in higher steady state output voltage ripple. 30% of per phase current is commonly used as a baseline.

Duty cycle (in ideal case and in actual scenario) can be calculated by the equations given below.

\[ D = \frac{V_{OUT}}{P_{VIN}} \]

In an ideal case, the voltage drops of the power MOSFETs (High Side and Low Side) and Inductor are zero.

**PVIN** – Input Voltage used for power conversion.
In actual applications, high side and low side power MOSFETs within the power stage have ON resistance and hence drop voltage across them when turned ON. Similarly, Inductor has DCR which results in voltage drop. So,

\[
D = \frac{V_{OUT} + V_{DROPLS} + V_{DROPIND}}{P_{VIN} - V_{DROPHS} + V_{DROPLS}}
\]

**V\text{DROPLS}** – Voltage drop across the low side MOSFET when ON and can approximately be calculated using the formula given below.

\[
V_{DROPLS} = \frac{I_{OUT}}{N} \times R_{DS\text{ON}LS}
\]

**V\text{DROPIND}** – Voltage drop across the DCR of Inductor and can be calculated using the formula given below.

\[
V_{DROPIND} = \frac{I_{OUT}}{N} \times DCR
\]

**V\text{DROPHS}** – Voltage drop across the high side MOSFET when ON and can approximately be calculated using the formula given below.

\[
V_{DROPHS} = \frac{I_{OUT}}{N} \times R_{DS\text{ON}HS}
\]

**N** – Number of phases

**I\text{OUT}** – Maximum output current specification

**R\text{DS\text{ON}HS}** – On resistance of high side MOSFET

**R\text{DS\text{ON}LS}** – On resistance of low side MOSFET

**DCR** – DC resistance of the inductor.

MOSFET ON drops and DCR voltage drop may not have significant impact on the duty cycle value. So, for simplifying the design procedure, duty cycle can be calculated using the equation given for ideal case.

Once the inductance value is calculated, select an inductor which is closer to the calculated value and commonly available. If the calculated value is 73nH and a commonly available inductor is 70nH, 70nH can be selected. Once the inductance value is finalized, inductor peak current (**I\text{PEAK}**), saturation current (**I\text{SAT}**) and RMS currents (**I\text{RMS}**) can be calculated as below.

\[
I_{PEAK} = \frac{I_{OUT}}{N} + \left[ \frac{(P_{VIN} - V_{OUT}) \times \frac{I_{OUT}}{LSEL \times FSW}}{0.5} \right]
\]
\[ I_{LSAT} = I_{LPEAK} \times 1.25 \]

\[ I_{L RMS} = \frac{I_{OUT}}{N} \times \sqrt{1 + \left( \frac{LIR \times \frac{1}{12}}{LSEL \times FSW} \right)} \]

**LIR** – Inductor ripple current ratio. This can be calculated by using the following equation.

\[ LIR = \frac{\left( \frac{P_{VIN} - V_{OUT}}{I_{OUT} \times \frac{LSEL \times FSW}{N}} \right)}{D} \]

ED8401 evaluation board specifications can be used for designing the critical components to form a high performing power supply.

*Table 5. ED8401 Evaluation Board Specifications*

<table>
<thead>
<tr>
<th>Specification</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>PVIN</td>
<td>4.5 - 16</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>VOUT</td>
<td>0.5 – 1.3</td>
<td>V</td>
</tr>
<tr>
<td>Max Output Current (Continuous)</td>
<td>IOUT</td>
<td>160</td>
<td>A</td>
</tr>
<tr>
<td>Load Step</td>
<td>ISTEP</td>
<td>80</td>
<td>A</td>
</tr>
<tr>
<td>Load Step Slew Rate</td>
<td>ISLEW</td>
<td>50</td>
<td>A/\text{us}</td>
</tr>
<tr>
<td>Steady State Output Ripple*</td>
<td>\Delta VOUTDC</td>
<td>\pm 10</td>
<td>mV</td>
</tr>
<tr>
<td>Transient Output Ripple*</td>
<td>\Delta VOUTAC</td>
<td>\pm 30</td>
<td>mV</td>
</tr>
<tr>
<td>Steady State Input Ripple</td>
<td>\Delta PVINDC</td>
<td>\pm 250</td>
<td>mV</td>
</tr>
<tr>
<td>Transient Input Ripple</td>
<td>\Delta PVINAC</td>
<td>\pm 400</td>
<td>mV</td>
</tr>
</tbody>
</table>

*The output capacitance used on the evaluation board is 16x470uF and 16x100uF capacitors to meet the output voltage ripple specifications (Steady state and transient). Load step considered is 80A.

For this design, a switching frequency of 500 kHz is used to provide a balanced tradeoff between transient response, solution size and efficiency. To deliver 160A of load current, four phases are required for optimized solution size and efficiency. For simplifying the design, an output voltage of 0.8V and input voltage of 12V are considered.

\[ D = \frac{V_{OUT}}{V_{PIN}} = \frac{0.8}{12} = 0.066667 \]
\[ \text{IRipple} = \frac{\text{IOUT}}{N} \times 0.3 \times \frac{160}{4} \times 0.3 = 12 \text{ Amps} \]

\[ L = \frac{\text{VOUT} \times (1 - D)}{\text{FSW} \times \text{IRipple}} = \frac{[0.8 \times (1 - 0.066667)]}{500000 \times 12} = 124.44 \text{ nH} \]

The value selected is 120nH which is commonly available. If the entire input range and output range given in the specification table are considered, inductance of 120nH limits the inductor current ripple to around 30%.

\[ \text{ILPEAK} = \frac{\text{IOUT}}{N} + \left( \frac{\text{PVIN} - \text{VOUT}}{\text{LSEL} \times \text{FSW}} \right) \times 0.5 = \frac{160}{4} \times (12 - 0.8) \times \frac{0.06667}{120n \times 500000} \times 0.5 \]

\[ = 46.222 \text{ Amps} \]

\[ \text{ILSAT} = \text{ILPEAK} \times 1.25 = 46.222 \times 1.25 = 57.7775 \text{ Amps} \]

\[ \text{LIR} = \frac{\left( \frac{\text{PVIN} - \text{VOUT}}{\text{LSEL} \times \text{FSW}} \right) \times D}{\text{IOUT} \times \frac{160}{4}} = \frac{[(12 - 0.8) \times 0.06667]}{120n \times 500000} = 0.311 \]

\[ \text{ILRMS} = \frac{\text{IOUT}}{N} \times \sqrt{1 + \left( \frac{\text{LIR} \times \text{LIR}}{\text{N}} \right)} \times \frac{160}{12} \times \sqrt{1 + (0.311 \times \frac{0.311}{4})} = 40.1608 \text{ Amps} \]

Based on the inductance value, saturation current rating and RMS current rating, the following table has inductor part numbers that are recommended to operate robustly within the entire operating range including the temperature range of -40°C to 85°C. 120nH is suitable for all 500 kHz designs (4 phase, 3 phase and 2 phase) and 70nH is for 1MHz designs. Other part numbers can always be used as long as the requirements (Inductance, Saturation Current and RMS Current) are met. Also, it is advised to use inductors with soft saturation characteristics. Inductors L6, L7, L8 and L9 in the ED8401 evaluation board are of 120nH inductors from ITG.
Output Capacitor Design and Selection

The output capacitance required depends on the switching ripple and AC transient specifications of an application. Next generation FPGAs, Processors, ASICs and Memory devices typically have AC transient requirements that are more demanding than the switching ripple specifications and dictate how much total output capacitance is needed. While choosing output capacitors, a mix of MLCCs and bulk caps are used. Ceramic capacitors keep the output impedance of the converter low before the control loop can respond during fast transients, minimizing overshoot and undershoot. Bulk capacitors provide enough of a charge reservoir for the output voltage to stay within the tolerance band as the controller ramps the inductor current to the new load current level.

Assuming minimal ESR and ESL in the capacitor network, the amount of output capacitance needed to handle the DC ripple can be calculated using the below equation.

\[ C_{OUTDC} = \frac{I_{RIPPLE}}{8 \times N \times F_{SW} \times V_{OUTDC}} \]

Output capacitance required in a single phase configuration can be calculated using the equation given below. There is no inductor current cancellation in single-phase operation making it the worst-case scenario.

\[ C_{OUTDC} = \frac{I_{RIPPLE}}{8 \times F_{SW} \times V_{OUTDC}} \]

Where

\[ I_{RIPPLE} = \frac{[(P_{VIN} - V_{OUT}) \times D]}{F_{SW} \times L_{SEL}} \]

The capacitance calculated based on steady state ripple may not be enough to support the pulsating currents demanded by FPGAs, ASICs and Memory devices. Calculating the output capacitance based on transient specifications is critical in order not to violate any specifications.
During load transients (Increase in load current), the switching regulator takes some amount of time to slew to the high current level required. In that time, an amount of charge is pulled from the output capacitors while VOUT dips below its set point (Undershoot). Similarly, upon load release, the switching regulator takes some amount of time to bring the inductor current down to its final value. In this period, excess charge in the inductors is dumped into the output capacitors, causing VOUT to swing above its regulation point (Overshoot).

The below equations are derived by simplifying the constraints involving the bandwidth of the switching regulator, voltage drops due to MOSFETs/DCR and slew rate of the load step. The output capacitance calculated using the equations below does meet the load transient specifications.

The approximate time taken by the switching regulator for settling during a load step can be calculated using below equation.

\[
T_{\text{settling}} = \frac{1}{K_{\text{set}} \cdot FBW}
\]

**KSET** – Scaling factor. This is usually in between 3 and 4. “3” can be used to keep input voltage ripple (transient) well below specification. “4” can be used to have input voltage ripple (transient) around the specification.

**FBW** – Bandwidth (Transient loop in case of ED8401) of the voltage regulator. The compensators are designed to have a bandwidth of 75 kHz for 500 kHz switching frequency operation and 115 kHz for 1MHz operation.

Now, the bulk capacitor needed can be calculated by using the following equation.

\[
C_{\text{OUTAC}} = \frac{[0.5 \cdot \text{STEP} \cdot T_{\text{settling}}]}{\Delta V_{\text{OUTAC}}}
\]

Output capacitance required/used on the ED8401 evaluation board can be calculated by using evaluation board specifications and above equations.

\[
I_{\text{ripple}} = \frac{[(P_{\text{in}} - V_{\text{out}}) \cdot D]}{F_{\text{sw}} \cdot L_{\text{sel}}} = \frac{[(12 - 0.8) \cdot 0.066667]}{500000 \cdot 120n} = 12.445 \text{ Amps}
\]

\[
C_{\text{OUTDC}} = \frac{I_{\text{ripple}}}{8 \cdot N \cdot F_{\text{sw}} \cdot \Delta V_{\text{OUTDC}}} = \frac{12.445}{8 \cdot 4 \cdot 500000 \cdot 10n} = 77.78 \text{ uF}
\]
The highest value of the capacitances calculated COUTDC and COUTAC is 7.11 mF. As can be seen, capacitance calculated based on the transient output voltage ripple specifications is much higher than that of steady state ripple specification.

Considering the wide output voltage range, input voltage range, switching regulator bandwidth and voltage/temperature derating of the capacitors, sixteen 470uFs (SP Cap) and sixteen 100uFs (MLCC) are selected. A mix of ceramic capacitors (MLCC) and bulk capacitors (SP Caps) help minimize the ESR and ESL when connected in parallel. The following capacitors are recommended to be used with default ED8401 configurations.

<table>
<thead>
<tr>
<th>Description</th>
<th>Manufacturer</th>
<th>P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>470µF, 2.5V, ESR 3mΩ SP-CAP</td>
<td>Panasonic</td>
<td>EEFGX0E471R</td>
</tr>
<tr>
<td>100µF, 6.3V, X5R, 1206 Ceramic</td>
<td>Kemet</td>
<td>C1206C107M9PACTU</td>
</tr>
</tbody>
</table>

**Input Capacitor Design and Selection**

Input capacitors are used to reduce the ripple voltage amplitude seen at the input of the switching regulator. A combination of MLCC and bulk capacitors are used to meet steady state voltage ripple and load transient deviation specifications. Ceramic capacitors placed right at the input of the power stages (ET6160 in this case) to reduce switching ripple voltage amplitude. Only ceramics have the extremely low ESR that is needed to reduce the ripple voltage amplitude. These capacitors must be placed close to the power stage input pins to be effective. Additional inductance in the capacitor current path raises the impedance at the switching frequency to levels that negate their effectiveness.

The amount of ceramic capacitance per phase needed to keep the input voltage switching ripple within its limits can be calculated by using the equation below.

\[
C_{INDC} = \frac{[I_{OUT} \times D \times (1 - D)]}{\eta \times N \times FSW \times \Delta P_{INDC}}
\]
η - Efficiency of the switching regulator at maximum load current. This can be approximately estimated by using the efficiency graphs provided in the power stage (ET6160) datasheet.

The amount of bulk capacitance needed depends on the load and line transients. The line transients are not significant considering the application space of FPGAs, ASICs and Memory devices because of the fact that the front end regulator maintains its output which is an input to the ED8401+ET6160 based core power supplies. So, for calculating input capacitance, load transients need to be considered.

For a given load step (ISTEP), the effective increase in input average current can approximately be calculated using the below equation.

\[ HINSTEP = \frac{ISTEP \times D}{\eta} \]

The input bulk capacitors eventually get affected by the load current step and need to provide additional current for a period which is dependent on the bandwidth of switching regulator and the inductance in the path from the front end regulator and input bulk capacitors. For input capacitance calculation, assume that the bulk capacitors are providing all the charge required during load current change. The approximate time taken by the switching regulator for settling during a load step can be calculated using below equation.

\[ TSETTLING = \frac{1}{KSET \times FBW} \]

**KSET** – Scaling factor. This is usually in between 3 and 4. “3” can be used to keep input voltage ripple (transient) well below specification. “4” can be used to have input voltage ripple (transient) around the specification.

**FBW** – Bandwidth (Transient loop in case of ED8401) of the voltage regulator. The compensators are designed to have a bandwidth of 75 kHz for 500 kHz switching frequency operation and 115 kHz for 1MHz operation.

Now, the bulk capacitor needed can be calculated by using the following equation.

\[ CINAC = \frac{[0.5 \times HINSTEP \times TSETTLING]}{\Delta VINAC} - CINDC \]

Input capacitance (close to power stages and bulk capacitors) needed can be calculated for the ED8401 evaluation board specifications.

\[ CINDC = \frac{[OUT \times D \times (1 - D)]}{\eta \times N \times FSW \times \Delta PVINDC} \]

\[ = \frac{[160 \times 0.066667 \times (1 - 0.066667)]}{0.90 \times 4 \times 500000 \times 250m} = 22.12\mu F \]

Each power stage needs to have a capacitance of 22\(\mu F\) close to the input pins. On the ED8401 evaluation board, considering voltage/temperature derating, the input capacitance...
consists of three 10uF ceramic capacitors along with two 1uF capacitors for each phase. Tighter input switching ripple specification demand more number of MLCC capacitors close to the power stage input pins.

\[
T_{SE\text{LLING}} = \frac{1}{K_{SE\text{T}} \ast FBW} = \frac{1}{3 \ast 75000} = 4.44 \text{.us}
\]

\[
I_{IN\text{STEP}} = \frac{I_{STEP} \ast D}{\eta} = \frac{80 \ast 0.066667}{0.9} = 5.9259 \text{ Amps}
\]

\[
C_{IN\text{AC}} = \left[0.5 \ast I_{IN\text{STEP}} \ast T_{SE\text{LLING}}\right] \Delta VIN\text{AC} - C_{INDC} = \left[0.5 \ast 5.9259 \ast 4.44u\right] - \frac{22u}{400m} = 10.88uF
\]

The evaluation board does not include the front end converter and requires wires for connecting bench power supplies. Long wires result in additional path inductance. In order to avoid the effect of long wires (From bench power supplies to ED8401 Evaluation board), it is required to have bulk capacitors which is why 680uF capacitors can be seen at the input. In real applications, the front end regulator is on the board and large bulk capacitors may not be required. In a four phase application, four (number of phases) times CINDC and CINAC are required to meet input voltage switching ripple specification and input voltage transient ripple specification. As seen in the ED8401 evaluation board, each power stage has three 10uF ceramic capacitors and two 1uF ceramic capacitors placed close to the PVIN pins. The following table highlights the part numbers recommended.

**Table 8. Input Capacitor Parts Recommendation**

<table>
<thead>
<tr>
<th>Description</th>
<th>Manufacturer</th>
<th>P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>10µF, 25V, X6S, 0805 Ceramic Capacitor</td>
<td>Murata</td>
<td>GRM21BC81E106KE51L</td>
</tr>
<tr>
<td>1µF, 25V, X6S, 0402 Ceramic Capacitor</td>
<td>Murata</td>
<td>GRM155C81E105KE11D</td>
</tr>
</tbody>
</table>

**Power Stage Design and Selection**

The ED8401 is designed to closely work with the Intel Enpirion power stage family. The power stage recommended is ET6160 which is a monolithic 70A power stage with integrated current and temperature monitors. The current monitor provides a high-bandwidth current signal proportional to inductor current – 1uA per ampere of inductor current. It offers high system efficiency because of its monolithic structure while switching at frequencies up to 1MHz. The built-in fault management block protects the power stage from over temperature and over
current events and pulls TMON pin high during under voltage (VCC and PVIN) and over voltage events (PVIN).

Table 9. ET6160 Part Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Markings</th>
<th>Package Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ET6160LI</td>
<td>6160</td>
<td>5 mm x 6 mm x 0.9mm LGA</td>
</tr>
</tbody>
</table>

The ET6160 incorporates several internal voltage regulators to derive all required supply and bias voltages from a single external supply voltage to PVCC & AVCC. Decoupling capacitors are required on the AVCC, PVCC, and both VDD1/2 pins. The specified minimum capacitance must consider temperature and voltage therefore a high-quality dielectric like X7S or X7R is recommended. Two different ground connections are available on the outside of the package. These should be connected to a single ground. A differentiation between the grounds is not required - see layout recommendation section for greater detail. While both AVCC & PVCC are supplied from the same rail, a ferrite bead is required to be placed between the two to help filter any noise coupling form PVCC into the quieter AVCC. The Ferrite Bead used must have a DCR value of <1Ω. Both VDD1/2 pins (pins 6 and 31) are for decoupling capacitors only and should have no other electrical connections. The internal 1.8V LDO’s are not designed to support any external loading.

Table 10. Decoupling Capacitor Recommendation for ET6160

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>AVCC</td>
<td>2.2µF &amp; 1µF</td>
<td>Required</td>
</tr>
<tr>
<td>3</td>
<td>PVCC</td>
<td>10µF &amp; 2.2µF</td>
<td>Required</td>
</tr>
<tr>
<td>6</td>
<td>VDD1</td>
<td>22µF &amp; 2.2µF</td>
<td>Required</td>
</tr>
<tr>
<td>31</td>
<td>VDD2</td>
<td>1nF</td>
<td>Required</td>
</tr>
<tr>
<td>32 &amp; 33</td>
<td>PHASE to CBOOT</td>
<td>2.2µF</td>
<td>Required</td>
</tr>
</tbody>
</table>

A BST capacitor of 2.2uF is recommended to be connected between the CBOOT and PHASE pins of the ET6160 power stage. If required, an additional resistor can be added for adjusting the slew rate of the high side MOSFET within the power stage.
Input pins (25 to 30) should have ceramic capacitors placed very close to the pins and the capacitance value is based on the input switching ripple specification. See “Input capacitor design and selection” section.

The ET6160 has a current monitor which outputs 1uA for every ampere of inductor current. The ED8401 makes use of the IMON output from the ET6160 for current balancing and for protecting the regulator from over current or short circuit events. The ED8401 requires a voltage signal which is proportional to the current from the IMON pin of the ET6160. To transform a single ended current (IMON) output from power stage to a differential voltage signal to feed into ED8401, an on board voltage reference is required. AVDD18 (1.8V rail) of ED8401 and a buffer are used to generate the common mode voltage (or voltage reference).
In order to keep the ADCs in the ED8401 within the operating range and to avoid saturation effects, it is recommended to use a 2.7KOhm (R32) resistor for each phase. This maintains the voltage seen by ADCs well below saturation levels. The default ED8401 configurations consider 2.7KOhm for current balancing and protection from over current events. To match impedance, R33 (R30, R26 and R23 for other phases) needs to be same as 2.7KOhms.

**RVSET and RTUNE Selection**

The ED8401 supports a wide range of output voltages in order to power various devices such as FPGAs, ASICs, Processors and Memory devices. The default ED8401 configurations support the following voltages. Other voltages can be supported but requires custom ED8401 configuration. Connect a resistor between RVSET pin and ground with the value corresponding to the output voltage required.

**Table 11. RVSET Table for Different Output Voltages**

<table>
<thead>
<tr>
<th>RVSET Resistor</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0kΩ</td>
<td>Reserved</td>
</tr>
<tr>
<td>0.392kΩ</td>
<td>Reserved</td>
</tr>
<tr>
<td>0.576kΩ</td>
<td>1.3V</td>
</tr>
<tr>
<td>0.787kΩ</td>
<td>1.25V</td>
</tr>
<tr>
<td>1.000kΩ</td>
<td>1.2V</td>
</tr>
<tr>
<td>1.240kΩ</td>
<td>1.175V</td>
</tr>
<tr>
<td>1.500kΩ</td>
<td>1.15V</td>
</tr>
<tr>
<td>1.780kΩ</td>
<td>1.12V</td>
</tr>
<tr>
<td>2.100kΩ</td>
<td>1.1V</td>
</tr>
<tr>
<td>2.430kΩ</td>
<td>1.05V</td>
</tr>
<tr>
<td>RVSET Resistor</td>
<td>VOUT</td>
</tr>
<tr>
<td>---------------</td>
<td>------</td>
</tr>
<tr>
<td>2.800kΩ</td>
<td>1.03V</td>
</tr>
<tr>
<td>3.240kΩ</td>
<td>1.0V</td>
</tr>
<tr>
<td>3.740kΩ</td>
<td>0.975V</td>
</tr>
<tr>
<td>4.220kΩ</td>
<td>0.95V</td>
</tr>
<tr>
<td>4.750kΩ</td>
<td>0.92V</td>
</tr>
<tr>
<td>5.360kΩ</td>
<td>0.9V</td>
</tr>
<tr>
<td>6.040kΩ</td>
<td>0.89V</td>
</tr>
<tr>
<td>6.810kΩ</td>
<td>0.875V</td>
</tr>
<tr>
<td>7.680kΩ</td>
<td>0.85V</td>
</tr>
<tr>
<td>8.660kΩ</td>
<td>0.825V</td>
</tr>
<tr>
<td>9.530kΩ</td>
<td>0.8V</td>
</tr>
<tr>
<td>10.500kΩ</td>
<td>0.775V</td>
</tr>
<tr>
<td>11.800kΩ</td>
<td>0.75V</td>
</tr>
<tr>
<td>13.000kΩ</td>
<td>0.72V</td>
</tr>
<tr>
<td>14.300kΩ</td>
<td>0.7V</td>
</tr>
<tr>
<td>15.800kΩ</td>
<td>0.65V</td>
</tr>
<tr>
<td>17.400kΩ</td>
<td>0.6V</td>
</tr>
<tr>
<td>19.100kΩ</td>
<td>0.55V</td>
</tr>
<tr>
<td>21.000kΩ</td>
<td>0.52V</td>
</tr>
<tr>
<td>23.200kΩ</td>
<td>0.5V</td>
</tr>
</tbody>
</table>

The ED8401 supports direct output voltage feedback without any external components for up to an output voltage of 1.3V. However, adding a high-frequency low-pass filter into the sense path is highly recommended for removing high-frequency disturbances from the sense signals. Placing these components as close as possible to the controller is recommended.

For the switching regulator to respond to transients, be it change in input voltage or load current, and to always maintain the output in the regulation band, closed loop control is required. The ED8401 has an advanced digital controller which works as voltage mode controller using a PID type compensator. It features two parallel compensators, one for steady-state operation and another for fast transient operation. Fast, reliable switching between the different compensation modes ensures good transient performance and quiet steady state.
performance. The ED8401 uses over-sampling techniques to acquire fast, accurate, and continuous information about the output voltage so that the device can react quickly to any changes in output voltage.

To improve the transient performance for a typical point-of-load design, it is common to add output capacitance to the converter. This moves the output LC resonant frequency lower as capacitance increases which results in lower bandwidth, lower phase margin, and longer settling times unless the control loop is compensated for added capacitance. With the default configuration of the ED8401, the user can select from preconfigured PID control loop settings (known as compensators) using pin-strapping. A single resistor from the RTUNE pin to GND informs the ED8401 of the compensator selection to use on power up.

The selection of the compensator is driven by switching frequency, output inductor and by the type of output capacitors used, as the ESL and ESR of different capacitor types demand different PID coefficients to optimize transient deviation and recovery characteristics. The default compensator is a design with a combination of ceramic and polymer capacitors, i.e. SP-CAP.

Figure 13. Advanced Digital Controller with Voltage Mode Scheme

Considering the wide variety of applications based on FPGAs, ASICs and Memory devices, the ED8401 default configurations come with default PID compensators for both steady state and transient loops so that various load steps and corresponding voltage deviation (transient ripple) specifications are met.
Table 12. Base Capacitance for Different Configurations (Phases and Frequency)

<table>
<thead>
<tr>
<th>Phase Configuration</th>
<th>Switching Frequency</th>
<th>Base Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>500 kHz</td>
<td>16x470uF and 16x100uF</td>
</tr>
<tr>
<td>3</td>
<td>500 kHz</td>
<td>6x470uF and 6x100uF</td>
</tr>
<tr>
<td>2</td>
<td>500 kHz</td>
<td>4x470uF and 4x100uF</td>
</tr>
</tbody>
</table>

The ED8401 does come in three basic variants and they are four phase, three phase and two phase variants. Each of these phase variants has one frequency option available (500 kHz). The recommended inductor for all the 500 kHz configurations is 120nH. Different switching frequencies result in different closed loop bandwidths. The bandwidth for 500 kHz operation is selected to be around 75 kHz. The PID compensators are designed considering a base capacitance for each of the phase configurations (4 phase, 3 phase and 2 Phase). See the base capacitance details in the table above.

The ED8401 has provision for five different PID compensators (includes both loops) which can be subdivided into groups of six each whereby the base capacitance value in the appropriate compensator can be scaled by a factor M to match the additional/reduced capacitance. Each ED8401 variant has a compensator which is then divided into six to support different output capacitances. The scaling factor M and compensator corresponding to the new output capacitance (different from Base Capacitance) can be selected by using the RTUNE resistor which is connected between the RTUNE pin and ground.

Table 13. RTUNE Table for 4 Phase 500kHz Configuration – ED8401P01

<table>
<thead>
<tr>
<th>Compensator Description</th>
<th>RTUNE Resistor (Using 1% resistor)</th>
<th>Multiplication factor (M)</th>
<th>Typical Deviation with 80A Load Step (50A/us Slew Rate)</th>
<th>Typical Deviation with 60A Load Step (50A/us Slew Rate)</th>
<th>Typical Deviation with 40A Load Step (50A/us Slew Rate)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default Compensator</td>
<td>0kΩ</td>
<td>1</td>
<td>± 25mV</td>
<td>± 18mV</td>
<td>± 12mV</td>
</tr>
<tr>
<td></td>
<td>0.392kΩ</td>
<td>.25</td>
<td>± 90mV</td>
<td>± 68mV</td>
<td>± 45mV</td>
</tr>
<tr>
<td></td>
<td>0.576kΩ</td>
<td>.5</td>
<td>± 45mV</td>
<td>± 36mV</td>
<td>± 25mV</td>
</tr>
<tr>
<td></td>
<td>0.787kΩ</td>
<td>.75</td>
<td>± 32mV</td>
<td>± 25mV</td>
<td>± 18mV</td>
</tr>
<tr>
<td></td>
<td>1.000kΩ</td>
<td>1.5</td>
<td>± 16mV</td>
<td>± 12mV</td>
<td>± 8mV</td>
</tr>
<tr>
<td></td>
<td>1.240kΩ</td>
<td>2</td>
<td>± 12mV</td>
<td>± 8mV</td>
<td>± 6mV</td>
</tr>
</tbody>
</table>

**Base capacitance** = 16 x 470µF (Polymer) + 16 x 100µF (Ceramic)
For scaling factors 1.5 and 2, use the capacitor combinations of (24x470u and 16x100uF) and (32x470uF and 16x100uF) respectively even though theoretical calculation indicates the capacitor combinations to be used are (24x470uF and 24x100uF) and (32x470uF and 32x100uF). Similarly, for scaling factor of 0.25, it may be useful in reducing the steady state ripple if 8x100uF ceramic capacitors (along with 4x470uF polymer capacitors) are used instead of 4x100uF ceramic capacitors.

The amount of capacitance required can be calculated by using base capacitance, load step (ISTEP) and output voltage deviation specifications given in the RTUNE tables. The required multiplication factor for a given voltage deviation specification (VOUTAC) is

\[ M_{REQ} = \frac{\text{VOUTAC}_\text{BASE}}{\text{VOUTAC}} \times \frac{\text{ISTEP}}{\text{ISTEP}_{\text{BASE}}} \]

\[ C_{OUT}\_\text{REQ} = C_{OUT}\_\text{BASE} \times M_{REQ} \]

- **MREQ** – Required multiplication factor.
- **COUTBASE** – Base capacitance for a given configuration.
- **ISTEPBASE** – Load step from RTUNE table.
- **VOUTACBASE** – Voltage deviation from RTUNE table for a given base capacitance and load step (ISTEPBASE).
- **COUTREQ** – Output capacitance required for a given VOUTAC specification.

For an example, the multiplication factor required for a load step requirement of 80A to keep voltage deviation within 50mV can be calculated as given below.

\[ M_{REQ} = \frac{25}{50} \times \frac{80}{80} = 0.5 \]

\[ C_{OUT}\_\text{REQ} = C_{OUT}\_\text{BASE} \times M_{REQ} = [16\times470uF \text{ and } 16\times100uF] \times 0.5 = 8\times470uF \text{ and } 8\times100uF \]

For most applications, the scaling factor may not exactly match one of the options in the RTUNE tables. Take an example of 1V output application with requirement to have ±2.5% voltage deviation during a load step of 70A.

\[ M_{REQ} = \frac{25}{25} \times \frac{70}{80} = 0.875 \]
\[ C_{O\text{UTREQ}} = C_{O\text{UTBASE}} \times M_{REQ} = [16 \times 470 \mu F \text{ and } 16 \times 100] \times 0.875 = 14 \times 470 \mu F \text{ and } 14 \times 100 \mu F \]

The above application (example) requires less capacitance than the base capacitance which helps reduce the solution size and cost. The compensator can be of base capacitance’s (0KOhms) to assure stability. There is further opportunity to optimize output capacitance in applications with narrow operating zone (in terms of input voltage or temperature).

For specific applications, the ED8401 compensator can also be designed and if no other parameter needs to be changed, it can be simply included into an available blank of RTUNE compensator.

**Scaling Current Limit**

The ED8401 makes use of IMON output from the ET6160 power stages for current balancing and for protecting the regulator from over current events. The over current limits (warning and fault limits) are pre-defined and are a part of the ED8401 configuration. To make sure 40A (per phase) maximum continuous current is delivered, over current warning and fault limits are set at 50A and 53A respectively.

For a four phase configuration, 160A load current is supported continuously over the entire operating range (Including temperature range of -40°C to 85°C ambient temperature). So, when the output current is above 200A (50A per phase), an over current warning is flagged. When the output current is above 212A, over current event is detected, and regulator takes necessary action. IMON resistors (R19, R25, R29 and R32) shown in the schematic are 2.7KOhms for default ED8401 configurations.

The current limit settings of ED8401 can be scaled by using two methods. One is by using PMBus commands and this approach requires a host for writing into the required register. The other simple approach is by scaling the IMON resistor (R19, R25, R29 and R32) which may have impact on the current readouts using PMBus. In order to read the correct current values, appropriate scaling factor needs to be used on top of what is read from the PMBus registers.

The current limit scaling can be done by replacing the existing value of 2.7KOhms with a new value which is calculated using below given equation.

\[ R_{CL\text{NEW}} = \frac{I_{LM\text{DEF}}}{I_{LM\text{NEW}}} \times R_{CL\text{DEF}} \]

- \( R_{CL\text{NEW}} \) – New current sense/limit resistor.
- \( R_{CL\text{DEF}} \) – Default current sense/limit resistor and 2.7KOhms for ET6160.
- \( I_{LM\text{DEF}} \) – Default current limit set for a given ED8401 configuration.
- \( I_{LM\text{NEW}} \) – Desired current limit setting.
For example, ED8401P01 has a default per phase current limit setting of 53A which allows for a maximum continuous current of 40A. If the load current of an application is 120A and prefer four phase configuration to select a low profile inductor with lower saturation current. The current limit for a 120A application (30A per phase) does have to be lower than that of 160A application in order optimize inductor footprint. The new current limit required can be calculated as follows.

\[ \text{ILMNEW} = \frac{\text{ILMDEF} \times \text{IPHNEW}}{\text{IPHDEF}} \]

**IPHNEW** – Required per phase continuous current rating.

**IPHDEF** – Default per phase continuous current rating.

Now, ILMNEW for above mentioned 120A application is

\[ \text{ILMNEW} = \frac{\text{ILMDEF} \times \text{IPHNEW}}{\text{IPHDEF}} = \frac{53 \times 30}{40} = 39.75A = \sim 40A \]

The current sense/limit resistor required for 120A application is

\[ \text{RCLNEW} = \frac{\text{ILMDEF}}{\text{ILMNEW}} \times \text{RCLDEF} = \frac{53}{40} \times 2.7k = 3.5775k\Omega \text{ms} \sim 3.6k\Omega \text{ms} \]

With new current sense/limit resistor, for correct current information through PMBus, a scaling factor is required. Once the current is read from the registers using PMBus, after conversion, it needs to be multiplied with a scaling factor of RCLDEF/RCLNEW.

**ED8401 Supply Rails and Decoupling Requirements**

The ED8401 incorporates several internal voltage regulators to derive all required supply and bias voltages from a single external supply voltage which can be either 5V or 3.3V depending on whether the internal 3.3V regulator is used. If the internal 3.3V regulator is not used, 3.3V must be supplied to VDD33 and VDD50 pins respectively. Decoupling capacitors are required at the VDD33, VDD18, and AVDD18 pins (1.0µF minimum; 4.7µF recommended). If the 5.0V supply voltage is used, i.e. the internal 3.3V regulator is used, a small load current can be drawn from the VDD33 pin. This can be used to supply pull-up resistors, for example. The specified minimum capacitance must take into account temperature and voltage therefore a high quality dielectric like X7R is recommend.
Table 14. ED8401 Decoupling Capacitors

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>VREFP</td>
<td>100nF</td>
<td>Required</td>
</tr>
<tr>
<td>36</td>
<td>VDD18</td>
<td>1µF (minimum)</td>
<td>Required</td>
</tr>
<tr>
<td>37</td>
<td>VDD33</td>
<td>1µF (minimum)</td>
<td>Required</td>
</tr>
<tr>
<td>38</td>
<td>VDD50</td>
<td>1µF(minimum)</td>
<td>Required</td>
</tr>
<tr>
<td>39</td>
<td>AVDD18</td>
<td>1µF (minimum)</td>
<td>Required</td>
</tr>
<tr>
<td>40</td>
<td>ADCVREF</td>
<td>100nF</td>
<td>Required</td>
</tr>
<tr>
<td>2,40</td>
<td>VREFP to</td>
<td>51Ω</td>
<td>Required</td>
</tr>
<tr>
<td></td>
<td>ADCVREF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Three different ground connections are available on the outside of the package. These should be connected to a single ground. A differentiation between analog and digital ground is not required. The reference voltages required for the analog-to-digital converters are generated within the ED8401. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 100nF capacitor is required at the VREFP pin and a 100nF capacitor at ADCVREF pin. The two pins should be connected with approximately 50Ω resistance in order to provide sufficient decoupling between the pins.

**Power Sequencing Recommendation**

Even though there is no specific power up/down sequencing requirement when it comes to ED8401 and ET6160, it is recommended to follow the sequence below.

**During Power Up:**
- PVIN (Input Supply For Power Conversion)
- Supply to ED8401 and ET6160
- Enable

**During Power Down:**
- Enable
- Supply to ED8401 and ET6160
- PVIN (Input Supply For Power Conversion)

As mentioned above, every possible power up/down sequence provides the same performance during start-up and shutdown scenarios and there is no performance deficiency.
Layout Guidelines

Before highlighting various guidelines for ED8401+ET6160 layout, it is essential to make sure the schematic is error free. The checklist below may help make the schematic error free.

❖ Verify the pin out of all the components against the pin out provided in their respective datasheets.
❖ Confirm the choice of ED8401 version (ED8401P01/3/5) to make sure the default configuration is in line with the requirements.
❖ Confirm the choice of inductor and its part number.
❖ Confirm the choice of input capacitors and their part numbers.
❖ Confirm the choice of output capacitors and their part numbers.
❖ Confirm the choice of supply decoupling capacitors for ED8401 and ET6160.
❖ Verify the component values of RCs (Against the design) around ED8401 and ET6160.
❖ Confirm the polarity of the differential pair of voltage sensing network.
❖ Confirm the polarity of differential pair of current sensing.
❖ Verify all the connections thoroughly.

The effectiveness of the layout in isolating noisy signals/zones from quiet or sensitive analog signals is extremely critical for extracting superior performance from the switching regulators i.e to have highest possible noise immunity while reacting to system changes (Load current variation, input voltage variation and temperature variation etc.) as fast as possible. The power dissipation capability, additional path inductance and additional voltage drops can be optimized with better layout. The layout of ED8401 (with ET6160) evaluation board can be used as a reference. System form factors, space constraints and use of heat sinks may drive the way the power supplies are laid out.

The following section highlights key recommendations that can be followed for effective layout.

❖ The ED8401 requires decoupling capacitors at the pins VDD50, VDD33, VDD18, AVDD18, VREFP and ADCVREF. Place the capacitors very close to the pins for effective filtering and to ensure stability of internal regulators (if any).
The voltage feedback coming from the load must be routed as differential pair (distance ≤ 10 mil) all the way to the multi-phase controller ED8401 VFBP and VFBN pins. Recommended trace width is 8-10 mil. Care should be taken to avoid routing over switching node traces. Place the anti-aliasing filter (1k and 22pF) components close to the controller. See figure 15.
The PWM lines should be routed from the ED8401 device to the power stage ET6160 without crossing any switch-node signals. Also, maintain enough clearance from PWM signals to any sensitive analog signals (Feedback signals or current sense signals etc.).

ED8401 makes use of the IMON signal from power stages for active current sharing between phases and for protection from over current scenarios. Clean current information is required for accurate current sharing and current limiting performance of the ED8401. Route the IMON signals from power stages (ET6160) away from noisy signals. Recommended trace width is 8-10 mil. As mentioned in the “Power Stage Design and Selection” section, an external reference is required. The buffer circuitry can be placed near the multiphase controller (ED8401). See figure 17.
Figure 18. Symmetrical Placement of Power Stages

❖ The ED8401 device does not mandate special care in the layout of the power stage components. This is because independent IMON signal is provided to monitor individual power stage currents. If it is possible to lay out the phases in a symmetrical manner, then it is advised to do so. Refer to Figure 18.

❖ Even though, ED8401 does not mandate any special power stage component placement, for efficient power transfer, follow ET6160 layout guidelines (provided in the ET6160 Datasheet). The ET6160 requires decoupling capacitors at the pins AVCC, PVCC, VDD1 and VDD2 and place these capacitors very close to the pins for effective filtering and stability of built in regulators. As shown in Figure 19, if a pin has two capacitors (example: PVCC pin of ET6160 requires 10uF and 2.2uF capacitors), place the high frequency small footprint decoupling capacitor on the same layer as that of the power stage (Top layer in the case of ED8401 evaluation board) and the bulk of two capacitors can be placed on the bottom side.

Figure 19. ET6160 Decoupling Capacitor Placement
Place the bootstrap capacitor (2.2µF, 0402, 25V ceramic capacitor – C29, C38, C63 and C73 in the case of ED8401 evaluation board) close to the BOOT and Phase pins of ET6160. If required, a resistor can be placed in series with the bootstrap capacitor for reducing the slew rate of the high side MOSFET in the ET6160 power stage.

The placement of the input capacitors relative to PVIN and PGND pins of ET6160 device should have the highest priority during component placement. It is critical to minimize these node lengths. As such, place ceramic input capacitors as close as possible to the PVIN and PGND pins. However, system level constraints such as Z height requirements or provision for heat sink to increase thermal capability may restrict the placement of input capacitors (1206 or bigger). In these scenarios, some of the input capacitors may have to be placed on the bottom side. As can be noticed from the ED8401 evaluation board, there are ceramic capacitors on both sides of the evaluation board with an appropriate amount of vias (to reduce path inductance) interconnecting both the capacitors. The ED8401 evaluation board has provisions for a heat sink which limits the height of the components placed under the heat sink.

Figure 20. ET6160 Input Decoupling Capacitor Placement - Top Layer
The ET6160 has current sense and temperature sense blocks built in and for these internal blocks to provide accurate current and temperature signals (IMON and TMON), it is essential to avoid voltage level differences between various ground pins of the ET6160. It is recommended to connect all the ground pins of the ET6160 locally as shown below. This makes sure all the ground pins are at the same potential.

The switching node of the output inductor should be placed relatively close to the Power Stage ET6160 SW pins. Minimizing the switching node length between these two components reduces the PCB conduction losses and minimizes the switching noise level.
(or ringing level). As can be seen from the Figure 22, switch nodes of inductors L6, L7, L8 and L9 are placed very close the SW pins of the corresponding ET6160 power stages (U1, U2, U3 and U4).

Figure 23. Inductor Placement Close ET6160

- Minimize the switching loops as short as possible which helps localize the switching noise. Due to the way switching regulators operate, there are two switching states. One state when the switch is on and one when the switch is off. During each state there will be a switching current loop made by the power components that are conducting during that state. For example, when the high side MOSFET is ON, the switching currents flow from input decoupling capacitors to the High Side MOSFET in the power stage then to the inductor and then to the output decoupling capacitors and back to the input capacitors through their ground terminals and planes/traces. This loop can be minimized by placing a direct and short ground plane/trace connecting high frequency decoupling capacitors of input and output. Similarly, when the low side MOSFET is turned ON, another switching loop forms comprising low side MOSFET, inductor and output decoupling capacitors. A direct and short ground plane/trace connecting power stage PGND pins and output decoupling capacitors (High frequency ones) help minimize the switching loop.

- The ET6160 has the ability to use the ground planes as the primary thermal path. The use of thermal vias is an effective way to pull the heat away from the power stage and into the system board. In order to better spread the current and the heat through the inner layers, arrays of VIAs should be placed in the power pads. 10mils diameter is a good size for the plated in-pad VIAs. See the figure below.
The ET6160 has die temperature sensing logic built in and for accurate reading and reporting by ED8401, place 0.1uF ceramic capacitors very close to the TEMPx pins of ED8401.

It is recommended that at least below the ED8401 and ET6160 module, the next layers to the surface (2 and n-1) are solid ground planes, which provides shielding and lower the ground impedance.

Make all the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381mm) per Ampere on top/bottom layer and 25 mils (0.635mm) per ampere on internal layers. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.
## Revision History

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<tr>
<th>Rev</th>
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<tbody>
<tr>
<td>A</td>
<td>18th March, 2020</td>
<td>Initial Release</td>
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