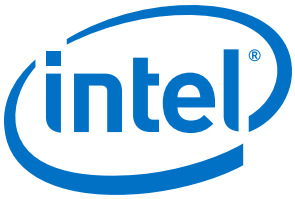

# AN 911: Achieving Timing Closure When Using the Top I/O Sub-Bank in Intel® Agilex™ Devices



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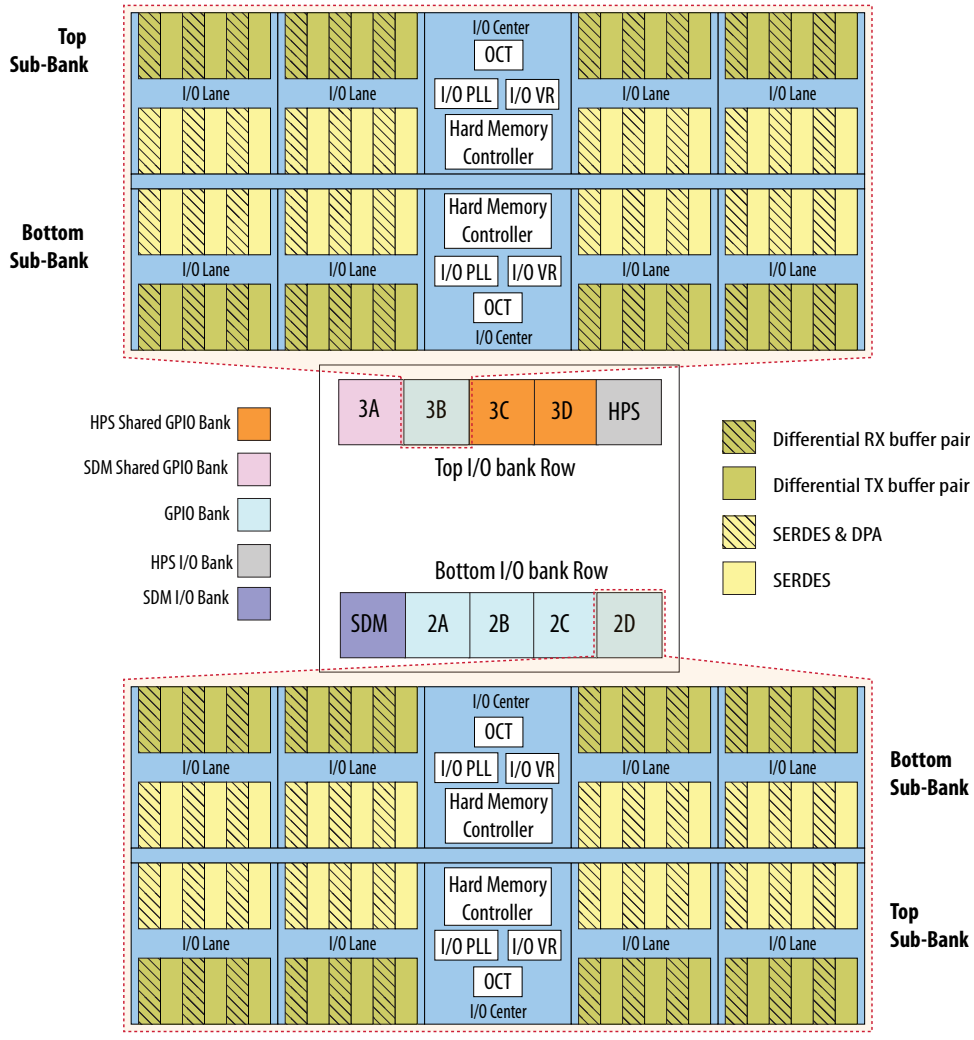
# Contents

# 1. Overview

Intel® Agilex™ devices have general-purpose I/O banks located at the top and bottom of the device. Each I/O bank has two sub-banks. The top I/O sub-bank is located near to the edge of the die while the bottom sub-bank is located near to the FPGA core. In each sub-bank, there is a dedicated I/O PLL and four I/O lanes with 12 I/O pins in each lane for you to design your general-purpose I/O (GPIO) applications.

**Figure 1. Intel Agilex I/O Bank Structure (Top View)**

This figure shows the I/O bank structure of Intel Agilex AGF 014 device. Different device packages have different number of I/O banks. Refer to the device pin-out files for available I/O banks for each device package.



When using the top I/O sub-bank for GPIO applications, you may see timing violations on the half-cycle transfer from the input data pins to the FPGA core due to the long data path. The pins in the top I/O sub-banks are identified as pin index 48 to 95 in the device pin-out files.

This application note describes two methods to resolve these timing violations using the GPIO Intel FPGA IP. The analysis in this document focuses on the input data paths from the GPIO Intel FPGA IP to the FPGA core. Follow the general best practices for timing closure in FPGA designs to resolve timing violations for other data paths.

**Related Information**

- Design Example: Achieving Timing Closure When Using Top I/O Sub Bank in Intel Agilex Devices
- GPIO Intel FPGA IP Architecture, Intel Agilex General-purpose I/O and LVDS SERDES User Guide
  Provides more information about the GPIO Intel FPGA IP.
- Intel Agilex Device Pin-Out Files

## 1.1. GPIO Intel FPGA IP Architecture

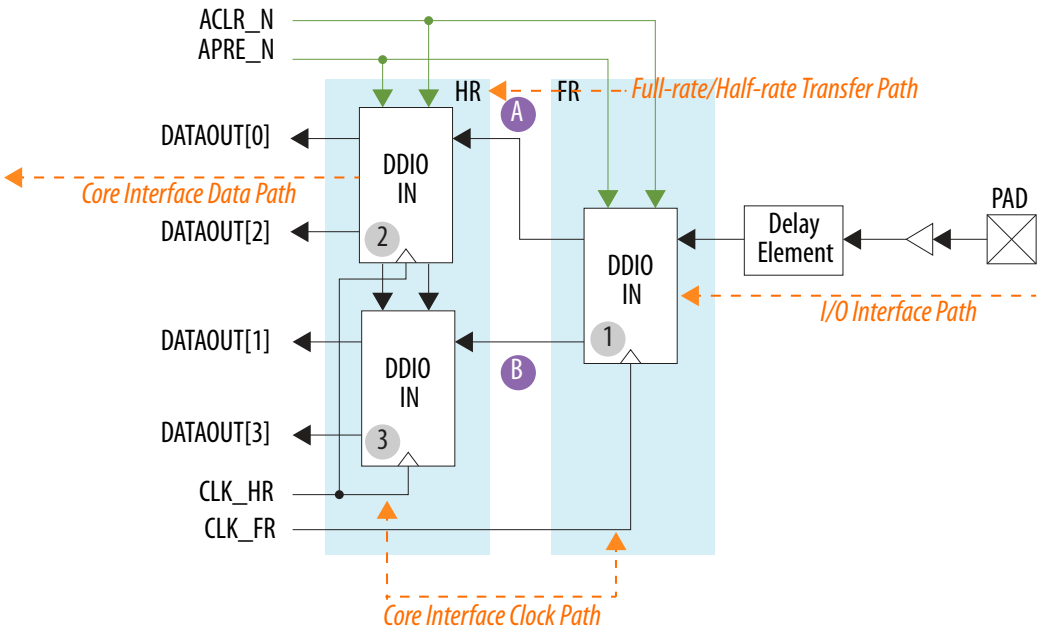
The GPIO Intel FPGA IP comprises of three components:

- Double data rate input/output (DDIO)—halves or doubles the data-rate of a communication channel.
- Delay chains—configure the delay chains to perform specific delay and assist in I/O timing closure.
- I/O buffers—connect the pads to the FPGA.

The GPIO Intel FPGA IP has Double Data Rate I/O (DDIO) blocks in the input path (DDIO IN) and DDIO blocks in the output path (DDIO OUT). Each path consists of one full-rate DDIO block (FR DDIO IN) and two half-rate DDIO blocks (HR DDIO IN). The subsequent content in this document focuses only on the input data path of the GPIO Intel FPGA IP.

The following figure shows the input data path of the GPIO Intel FPGA IP. The pad receives the data and the FR DDIO IN (1) block captures data on the rising and falling edges of the CLK_FR clock. The data is sent through signals (A) and (B) to the HR DDIO IN blocks. HR DDIO IN (2) and HR DDIO IN (3) blocks halve the data rate and presents the data through DATAOUT[3:0].

**Figure 2. Timing Components of a Simplified GPIO Input Path**



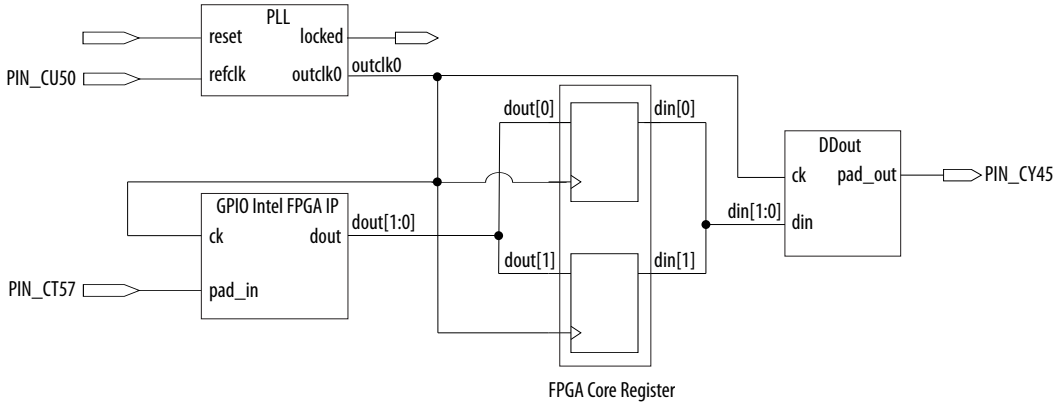

**Related Information**

Timing Components, Intel Agilex General-purpose I/O and LVDS SERDES User Guide.

## 1.2. Input Data Path Timing Violations

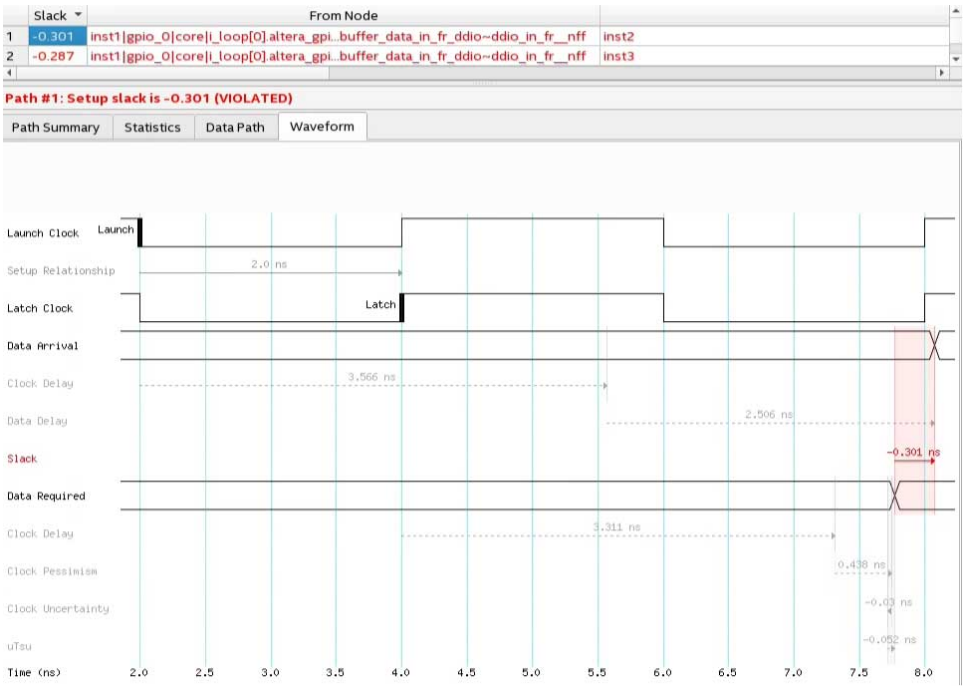
The `top.bdf` design example shows the connections of the GPIO Intel FPGA IP input data pins assigned to PIN CT57 in the top I/O sub-bank. The DDIO IN pins are connected to the FPGA core registers and the registers are using a rising edge clock for data sampling. The GPIO Intel FPGA IP in this design example is set to full-rate data transfer with a clock frequency of 250 MHz. The clock is provided by `outclk0`.

**Figure 3. Block Diagram of Full-Rate Data Transfer from DDIO IN to FPGA Core**



The following figure shows setup violation from the DDIO IN pins to the FPGA core registers. The latch clock occurs at half-cycle of the launch clock with only 2 ns setup relationship. However, the data arrival time is longer than the data required time.

**Figure 4. Setup Violation Timing Waveform**




To resolve this violation, you can use one of the following solutions:

1. Using a falling edge clock for capturing data in the full-rate transfer mode. This solution allows your design to operate in the maximum GPIO clock frequency but requires changes to the clock in user logic.
2. Using GPIO Intel FPGA IP in half-rate transfer mode. This solution operates in a slower clock frequency without changing the user logic clock.

# 2. Design Examples Requirements

## Software Requirements

There are three design example revisions described in this document:

- `top`—original design example with setup timing violation.
- `top_w1`—design example using falling edge clock latching solution.
- `top_w2`—design example using half-rate transfer mode solution.

All three design examples were created using the Intel Agilex AGFA014R243E3V device in the Intel Quartus® Prime Pro Edition software version 20.3.

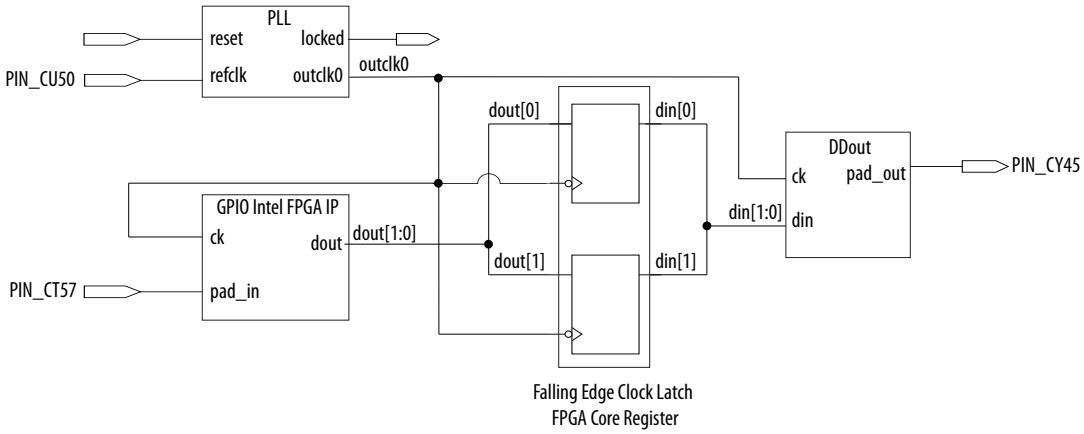
## Related Information

Design Example: Achieving Timing Closure When Using Top I/O Sub Bank in Intel Agilex Devices

# 3. Using A Falling Edge Clock for Data Capturing in Full-rate Transfer Mode

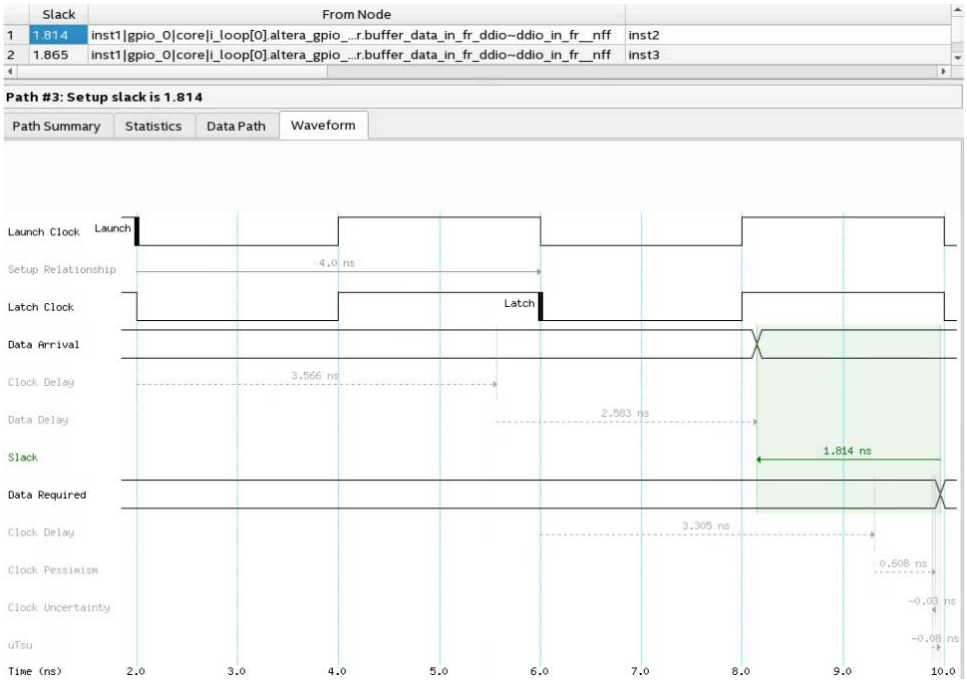
As shown in Figure 2 on page 5, the full-rate transfer mode is represented by signals A and B. In the full-rate mode interface, the two signals bypass the half-rate block. The timing violation on half-cycle transfer from the GPIO Intel FPGA IP to FPGA core is due to a tighter setup requirement. To rectify this, use a falling edge clock to capture the data because the full cycle window provides a larger setup requirement to fulfill the timing as shown in the `top_w1` design example.

**Figure 5. Block Diagram of Falling Edge Clock Core Register**




The following figure shows the timing waveform of the design example using a falling edge clock. The latch clock now has a full cycle window of 4 ns to capture the input data.

**Figure 6. Timing Waveform for Setup Time Using Falling Edge Clock**




This solution provides a setup slack of 1.814 ns with no additional latency to the design.

## 3.1. Design Example Walkthrough

To view the design connections and setup timing for the design example, follow these steps:

1. Download the `an911_design_examples.par` design example from the *Design Store for Intel FPGAs* web page and restore the design using the Intel Quartus Prime Pro Edition software version 20.3.
2. At the Intel Quartus Prime menu, click **Projects ➤ Revisions** and select the `top_w1` revision.
3. To view the design connections, at the Intel Quartus Prime menu, click **File ➤ Open** and select the `top_w1.bdf` schematic file.
4. From the Intel Quartus Prime menu, select **Processing ➤ Start Compilation** to compile the project.

   You must compile the design to view the setup timing for the design.

   Once the compilation completes, the **Timing Analyzer** window displays.
5. From the **Timing Analyzer** menu, select **Reports ➤ Custom Reports ➤ Report Timing**.
6. In the **Report Timing** window, click **OK** to display the timing report for all paths.

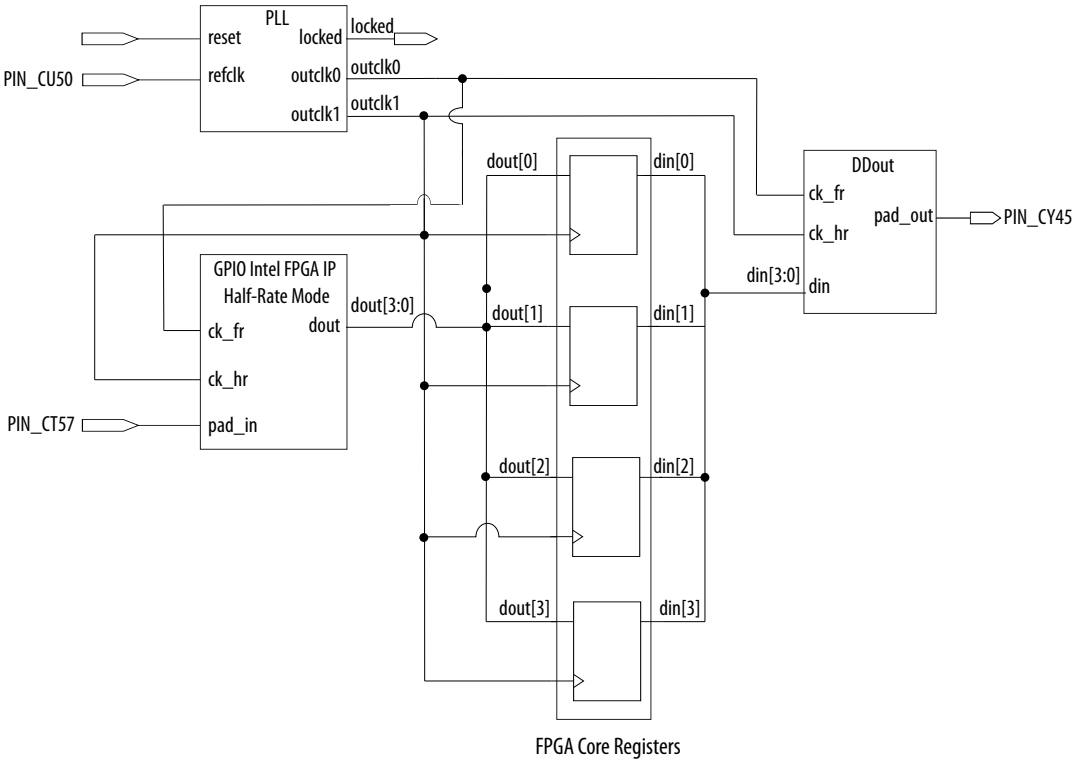
### Related Information

- Design Example: Achieving Timing Closure When Using Top I/O Sub Bank in Intel Agilex Devices
- Getting Started with the Design Store

# 4. Using GPIO Intel FPGA IP in Half-Rate Mode

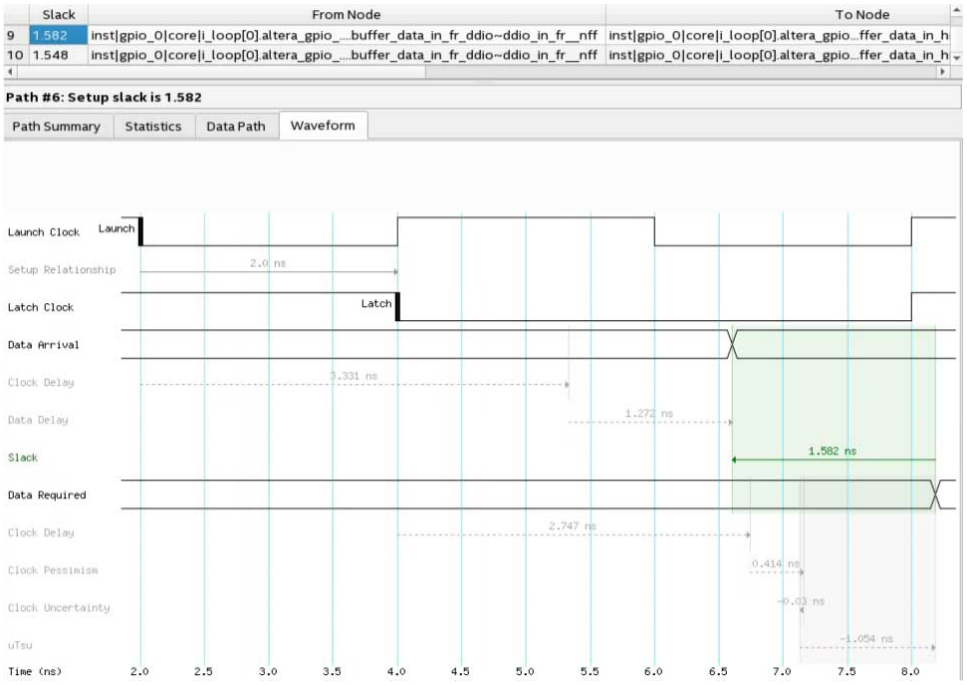
As shown in Figure 2 on page 5, in a half-rate mode interface, the A and B signals go through the HR DDIO IN block and output as DATAOUT[0:3]. Transferring data in half-rate mode reduces the core frequency and therefore augments the setup requirement. However, this solution requires design modifications by changing the GPIO Intel FPGA IP to half-rate mode. The top_w2 design example shows the full implementation of this solution. The outclk0 clock provides 250 MHz as the full-rate frequency and the outclk1 clock provides 125 MHz as the half-rate frequency.

**Figure 7. Block Diagram of Half-Rate Mode Implementation**



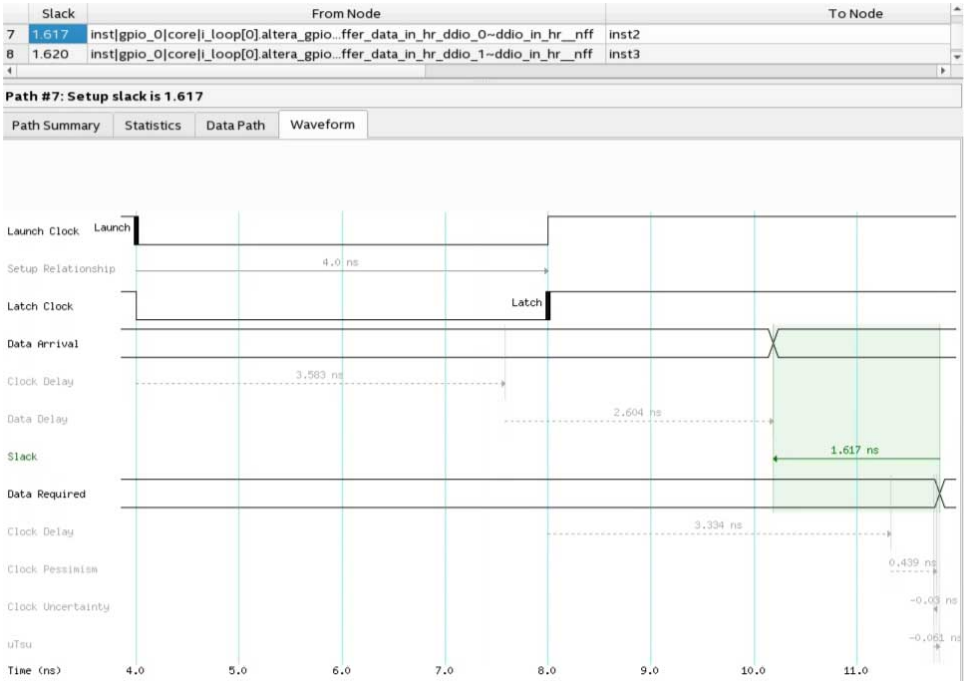

The following figure shows the timing waveform for the FR DDIO IN register to HR DDIO IN registers in the half-rate mode. The launch clock (outclk0) is operating in full-rate mode while the latch clock (outclk1) is operating in half-rate mode. The DDIO IN data is latched at half-cycle of the launch clock at every 2 ns interval.

**Figure 8. Timing Waveform of FR DDIO IN Register to HR DDIO IN Registers**




From the HR DDIO IN registers to the FPGA core registers, the data are latched at half-cycle of the launch clock at every 4 ns interval as shown in the following figure.

**Figure 9. Timing Waveform of HR DDIO IN Registers to FPGA Core Registers**



This design provides a setup slack of 1.617 ns from HR DDIO IN registers to the FPGA core registers. However, this solution utilizes more resources to implement half-rate data transfer in the design.

## 4.1. Design Example Walkthrough

To view the design connections and setup timing for the design example, follow these steps:

1. Download the `an911_design_examples.par` design example from the *Design Store for Intel FPGAs* web page and restore the design using the Intel Quartus Prime Pro Edition software version 20.3.
2. At the Intel Quartus Prime menu, click **Projects ➤ Revisions** and select the `top_w2` revision.
3. To view the design connections, at the Intel Quartus Prime menu, click **File ➤ Open** and select the `top_w2.bdf` schematic file.
4. From the Intel Quartus Prime menu, select **Processing ➤ Start Compilation** to compile the project.

   You must compile the design to view the setup timing for the design.

   Once the compilation completes, the **Timing Analyzer** window displays.
5. From the **Timing Analyzer** menu, select **Reports ➤ Custom Reports ➤ Report Timing**.
6. In the **Report Timing** window, click **OK** to display the timing report for all paths.

### Related Information

- Design Example: Achieving Timing Closure When Using Top I/O Sub Bank in Intel Agilex Devices
- Getting Started with the Design Store

# 5. Solutions Comparison

## Table 1. Solutions Comparison

This table lists the comparison between the two solutions.

| Solution | Setup Relationship | Setup Slack | Timing Path | | Advantages |
|---|---|---|---|---|---|
| | | | From | To | |
| Falling edge clock data capturing | Full cycle latch (4 ns) | 1.814 ns | DDIO IN pin | FPGA core register | • Full rate transfer with maximum operating frequency<br>• Larger setup slack<br>• No additional latency |
| Half-rate transfer mode | Half cycle latch (2 ns) | 1.582 ns | FR DDIO IN pin | HR DDIO IN registers in GPIO Intel FPGA IP | • Adequate setup slack<br>• Larger hold slack (4.820 ns) |
| | Half cycle latch (4 ns) | 1.617 ns | HR DDIO IN registers in GPIO Intel FPGA IP | FPGA core register | |

# 6. Document Revision History for AN 911: Achieving Timing Closure When Using the Top I/O Sub-Bank in Intel Agilex Devices

| Document Version | Changes |
|---|---|
| 2020.12.21 | Initial release. |