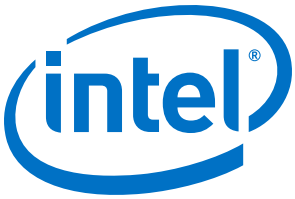


AN 909: JESD204C Intel® FPGA IP and TI ADC12DJ5200RF Interoperability Report for Intel® Stratix® 10 Devices

Subscribe
Send Feedback

AN-909 | 2020.06.09
Latest document on the web: PDF | HTML

Contents

1. JESD204C Intel® FPGA IP and TI ADC12DJ5200RF Interoperability Report for Intel® Stratix® 10 Devices

The JESD204C Intel® FPGA IP is a high-speed point-to-point serial interface intellectual property (IP).

The JESD204C Intel FPGA IP has been hardware-tested with a number of selected JESD204C compliant analog-to-digital converter (ADC) devices.

This report highlights the interoperability of the JESD204C Intel FPGA IP core with the ADC12DJ5200RF converter evaluation module (EVM) from Texas Instruments Inc. (TI). The following sections describe the hardware checkout methodology and test results.

Related Information

JESD204C Intel FPGA IP User Guide

1.1. Hardware Requirements

The hardware checkout test requires the following hardware and software tools:

- Intel Stratix® 10 TX Signal Integrity (SI) Development Kit (Production Rev B Edition) (1ST280EY2F55E1VG) with 12 V power adaptor
- TI ADC12DJ5200RF EVM with 5 V power adaptor
- SMA (Male) to SMP (Female) cables
- USB type A to B cable
- Mini-USB cable

Related Information

Intel Stratix 10 TX Signal Integrity Development Kit

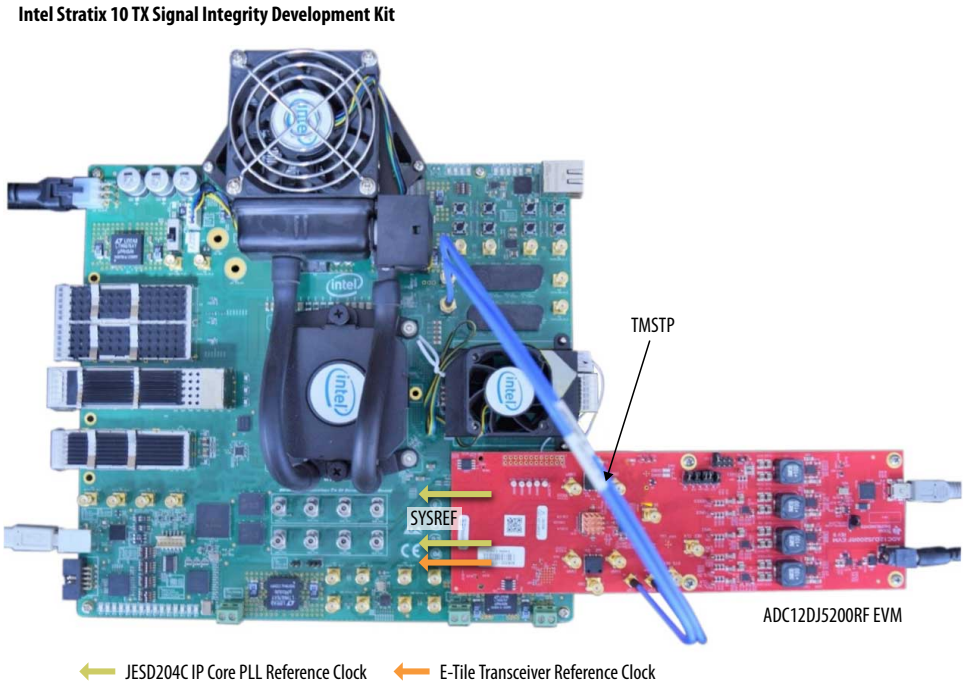
1.2. Hardware Setup

An Intel Stratix 10 TX SI Development Kit (Production Rev B Edition) is used with the TI ADC12DJ5200RF daughter card module installed to the FMC+ connector of the development board.

- The ADC12DJ5200RF EVM derives power from 12 V power adaptor.
- The ADC12DJ5200RF EVM is configured in the onboard clocking option (refer to the *Onboard Clocking Option* section of the *ADC12DJ5200RF Evaluation Module User's Guide*) and all the required clocks are generated by the ADC12DJ5200RF EVM and no external clock signals are required.
- The LMK61E2 programmable oscillator generates the reference frequency. The LMK00304 clock buffer make two copies of the reference signal and sends one copy to the LMX2594 frequency synthesizer to generate the sampling clock for the ADC.
- The LMK04828 clock generator uses the second copy in a clock distribution mode to provide the JESD204C Intel FPGA IP core PLL reference clock, and the E-tile transceiver reference clock through the FMC+ connector.
- For Subclass 1, the LMK04828 clock generator generates the SYSREF signal for the JESD204C Intel FPGA IP and the LMX2594 generates the SYSREF signal for the ADC12DJ5200RF device.

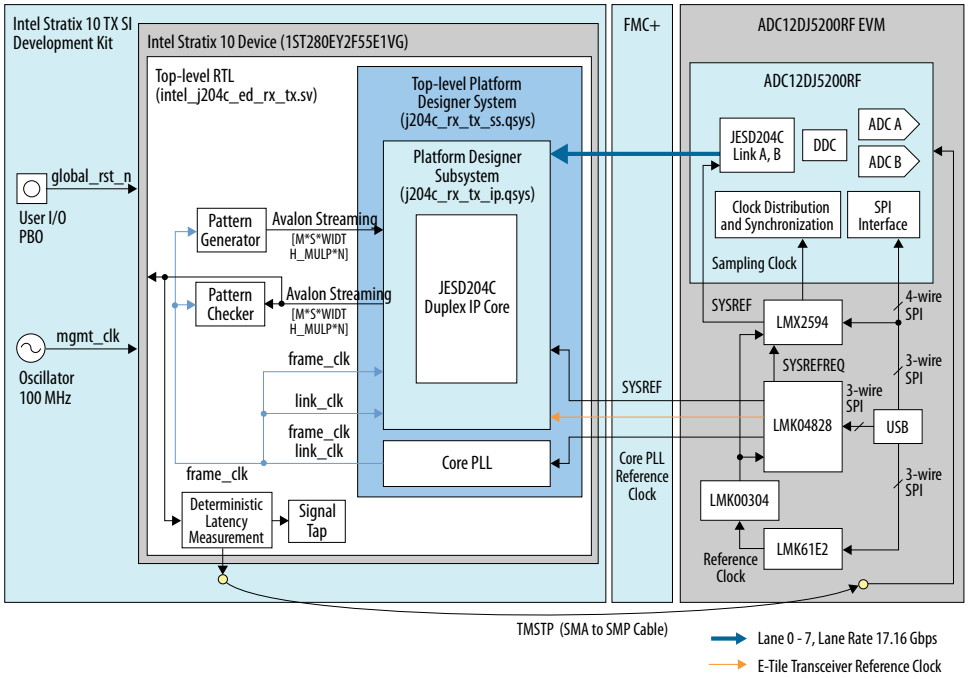
Note: Intel recommends the SYSREF to be provided by the clock generator that sources the JESD204C Intel FPGA IP device clock and sampling clock to ADC.

Figure 1. Hardware Setup



The following system level diagram shows how the different modules connect in this design.

Figure 2. System Diagram



In this setup, where LMF = 828, the data rate of transceiver lanes is 17.16 Gbps.

The LMK61E2 generated 260 MHz reference clock to the LMK00304. The LMK04828 takes the 260 MHz reference clock from the LMK00304 and distributes 260 MHz to JESD204C Intel FPGA IP device clock and E-tile transceiver reference clock through the FMC+ connector.

The LMK04828 also divides the 260 MHz reference clock to 8.125 MHz to provide a periodic SYSREF signal to the JESD204C Intel FPGA IP and the SYSREFREQ pin of the LMX2594.

The LMX2594 takes the 260 MHz reference clock from LMK00304 and generates 5200 MHz sampling clock to ADC12DJ5200RF device.

The LMX2594 is configured in SYSREF REPEATER mode to align the generated sampling clock and SYSREF from LMK04828 through SYSREFREQ pin. It provides a SYSREF of 8.125 MHz to ADC12DJ5200RF device.

The JESD204C Intel FPGA IP is instantiated in duplex mode but only the receiver path is used. For FCLK_MULP = 1, WIDTH_MULP = 2, and S = 1, the core PLL generates 130 MHz frame clock and link clock.

The TMSTP signal from the FPGA to ADC12DJ5200RF is for deterministic latency measurement.

Related Information

ADC12DJ5200RF Evaluation Module User's Guide

1.3. ADC12DJxx00RF EVM Software and JESD204C Example Design Setup

The ADC12DJxx00RF EVM software configures the ADC12DJ5200RF device, LMK61E2 programmable oscillator, LMK04828 clock generator, and LMX2594 frequency synthesizer for JESD204C link operation. Setup files for each parameter configuration are included in the software installation. You must configure the LMK61E2, LMK04828, LMX2594, and ADC12DJ5200RF modules with the correct settings and order, for the JESD204C link to operate at the targeted data rate and JESD204C link parameters.

Follow these steps to set up the configuration via the ADC12DJ5200RF EVM graphical user interface (GUI):

1. Configure the clock modules by loading the configuration from **Script→Load Config Script** menu option in the GUI.

   Note: Use the **Load Config Script** option instead of the **Program clocks and ADC** option in GUI for configuring clock and ADC on ADC12DJ5200RF EVM to execute the test as per the flow defined below.

2. Load the clock modules configuration scripts in the following order:
   a. `LMK61E2_xxxM.cfg`
   b. `LMK04828_JMODE30_to_39.cfg`
   c. `LMX2594_xxxxM_xxxM.cfg`
3. Use the following configuration files for the lane rates specified:

Lane Rate (Gbps)	Configuration File (.cfg)
9.9	LMK61E2_150M
10.3125	LMK61E2_156p25M
16.5	LMK61E2_250M
17.6	LMK61E2_260M

4. All supported lane rates and JESD204C 64B/66B modes of the ADC12DJ5200RF device uses `LMK04828_JMODE30_to_39.cfg` file. Use this file with the following modifications to provide SYSREF to SYSREFREQ pin of LMX2594:
   - `0x134 0x20 // Set SDCLKout13_MUX to SYSREF output & Bypass SDCLKout13 delay`
   - `0x137 0x11 // Set SDCLKout13 output format to LVDS`
5. Use the following LMX2594 configuration files for the lane rates specified with the corresponding modifications to enable SYSREF REPEATER mode:

Lane Rate (Gbps)	Configuration File (.cfg)	Modification
9.9	LMKX2594_3000M_150M	• 0x4B 0x0840 //[10:6]CHDIV • 0x49 0x06E4 //SYSREF Delay Control-Mi • 0x47 0x008D //[3]SYSREF_EN-1, [2]SYSREF_REPEAT-1 • 0x3A 0x0001 //[15]SYSREFREQ Pin enable • 0x2E 0x07FE //[1:0]RFoutB MUX - SYSREF • 0x2C 0x1F23 //[7]RFoutB - Power UP

continued...

Lane Rate (Gbps)	Configuration File (.cfg)	Modification
		• 0x25 0x0404 //[13:8]PFD_DLY_SEL • 0x24 0x0050 //PLL_N • 0x0C 0x5004 //PLL_R_PRE • 0x0B 0x0018 //[11:4]PLL_R • 0x04 0x0F43 //[15:8]ACAL_CMP_DLY • 0x01 0x0808 //CAL_CLK_DIV • 0x00 0x6418 //[14]VCO_PHASE_SYNC_EN - required for SYSREF_REPEAT
10.3125	LMKX2594_2500M_156p25M	• 0x4B 0x0840 //[10:6]CHDIV • 0x49 0x06E4 //SYSREF Delay Control-Min • 0x47 0x008D //[3]SYSREF_EN-1, [2]SYSREF_REPEAT-1 • 0x3A 0x0001 //[15]SYSREFREQ Pin enable • 0x2E 0x07FE //[1:0]RFoutB MUX - SYSREF • 0x2C 0x1F23 //[7]RFoutB - Power UP • 0x25 0x0304 //[13:8]PFD_DLY_SEL • 0x24 0x0040 //PLL_N • 0x0C 0x5004 //PLL_R_PRE • 0x0B 0x0018 //[11:4]PLL_R • 0x04 0x1043 //[15:8]ACAL_CMP_DLY • 0x01 0x0808 //CAL_CLK_DIV • 0x00 0x6418 //[14]VCO_PHASE_SYNC_EN - required for SYSREF_REPEAT
16.5	LMKX2594_4000M_250M	• 0x4B 0x0800 //[10:6]CHDIV • 0x49 0x06E4 //SYSREF Delay Control-Min • 0x47 0x008D //[3]SYSREF_EN-1, [2]SYSREF_REPEAT-1 • 0x3A 0x0001 //[15]SYSREFREQ Pin enable • 0x2E 0x07FE //[1:0]RFoutB MUX - SYSREF • 0x2C 0x1F23 //[7]RFoutB - Power UP • 0x25 0x0304 //[13:8]PFD_DLY_SEL • 0x24 0x0040 //PLL_N • 0x0C 0x5004 //PLL_R_PRE • 0x0B 0x0028 //[11:4]PLL_R • 0x04 0x0C43 //[15:8]ACAL_CMP_DLY • 0x01 0x0809 //CAL_CLK_DIV • 0x00 0x6418 //[14]VCO_PHASE_SYNC_EN - required for SYSREF_REPEAT
17.16	LMKX2594_5200M_260M	• 0x4B 0x0800 //[10:6]CHDIV • 0x49 0x06E4 //SYSREF Delay Control-Min • 0x47 0x008D //[3]SYSREF_EN-1, [2]SYSREF_REPEAT-1 • 0x3A 0x0001 //[15]SYSREFREQ Pin enable • 0x2E 0x07FE //[1:0]RFoutB MUX - SYSREF • 0x2C 0x1F23 //[7]RFoutB - Power UP • 0x25 0x0404 //[13:8]PFD_DLY_SEL • 0x24 0x0028 //PLL_N • 0x0C 0x5004 //PLL_R_PRE • 0x0B 0x0018 //[11:4]PLL_R

continued...

Lane Rate (Gbps)	Configuration File (.cfg)	Modification
		• 0x04 0x0D43 //[15:8]ACAL_CMP_DLY • 0x01 0x0809 //CAL_CLK_DIV • 0x00 0x6418 //[14]VCO_PHASE_SYNC_EN - required for SYSREF_REPEAT

6. Configure the FPGA with the JESD204C Intel FPGA IP example design by setting the PMA parameters GS1-2, GS2-2, RF-B0-3 and RF_B1-4, and SYSREF to use the external SYSREF from the FMC+ connector instead of the SYSREF from the SYSREF generator in the JESD204C Intel FPGA IP example design.
7. Configure the ADC12DJ5200RF device to the supported JESD204C link parameter by loading the configuration script from **Script→Load Config Script** menu option in the GUI.
8. Use the following ADC12DJ5200RF device configuration files with the corresponding modifications for transport layer testing of the mode specified:

LMF	Configuration File (.cfg)	Modification
828	ADC12DJxx00RF_JMODE31	• 0x0204 0x01 // Use SYNCSE input, offset binary data, scrambler enabled • 0x0205 0x05 // Transport Layer test mode • 0x0048 0x00 // Set serializer pre-emphasis to 0
622	ADC12DJxx00RF_JMODE33	
411	ADC12DJxx00RF_JMODE34	
421	ADC12DJxx00RF_JMODE35	
422	ADC12DJxx00RF_JMODE36	
442	ADC12DJxx00RF_JMODE37	
222	ADC12DJxx00RF_JMODE38	
244	ADC12DJxx00RF_JMODE39	
881	ADC12DJxx00RF_JMODE30	• 0x0204 0x01 // Use SYNCSE input, offset binary data, scrambler enabled • 0x0205 0x04 // Ramp test mode • 0x0048 0x00 // Set serializer pre-emphasis to 0
661	ADC12DJxx00RF_JMODE32	

9. Use the following ADC12DJ5200RF device configuration files with the corresponding modifications for deterministic latency measurement of the mode specified:

LMF	Configuration File (.cfg)	Modification
828	ADC12DJxx00RF_JMODE31	• 0x0061 0x00 // Clear CAL_EN (always after JESD_EN) • 0x0029 0x7x // Enable SYSREF Processing, SYSREF receiver circuit, SYSREF_ZOOM & [3:0]SYSREF_SEL (set based on section 7.3.6.3.1 of ADC12DJ5200RF data sheet) • 0x002A 0x02 // Enable SYSREF LVPECL • 0x002A 0x02 // Enable SYSREF LVPECL • 0x003B 0x03 // TMSTP_RECV_EN, TMSTP_LVPECL_EN • 0x0160 0x01 // TIME_STAMP_EN
612	ADC12DJxx00RF_JMODE32	
622	ADC12DJxx00RF_JMODE33	
411	ADC12DJxx00RF_JMODE34	
421	ADC12DJxx00RF_JMODE35	
422	ADC12DJxx00RF_JMODE36	
442	ADC12DJxx00RF_JMODE37	
222	ADC12DJxx00RF_JMODE38	

continued...

LMF	Configuration File (.cfg)	Modification
244	ADC12DJxx00RF_JMODE39	
881	ADC12DJxx00RF_JMODE30	• 0x002A 0x02 // Enable SYSREF LVPECL • 0x003B 0x03 // TMSTP_RECV_EN, TMSTP_LVPECL_EN • 0x0160 0x01 // TIME_STAMP_EN
661	ADC12DJxx00RF_JMODE32	

1.4. Hardware Checkout Methodology

The following section describes the test objectives, procedure, and the passing criteria. The test covers the following areas:

- Receiver data link layer
- Receiver transport layer
- Deterministic Latency (Subclass 1)

1.4.1. Receiver Data Link Layer

This test area covers the test cases for sync header alignment (SHA) and extended multiblock alignment (EMBA).

On link start up, after the receiver reset, the JESD204C Intel FPGA IP starts looking for the sync header stream that is transmitted by the ADC. The Signal Tap logic analyzer tool monitors the receiver data link layer operation.

1.4.1.1. Sync Header Alignment

Table 1. Sync Header Alignment Test Cases

Test Case	Objective	Description	Passing Criteria
SHA.1	Check if Sync Header Lock is asserted after the completion of reset sequence.	The following signals in<*ip_variant_name*>_base.v are tapped: • j204c_rx_rst_n • j204c_rx_sh_lock • j204c_rx_int(1) The rxlink_clk is used as the sampling clock for the Signal Tap.	• The j204c_rx_sh_lock is asserted after the deassertion of _j204c_rx_rst_n. • The j204c_rx_int signal is deasserted if there is no error.
SHA.2	Check Sync Header Lock status after sync header lock is achieved (or during the Extended Multi-Block Alignment phase) and stable.	The following signals in<*ip_variant_name*>_base.v are tapped • j204c_rx_sh_lock • j204c_rx_int(1) The rxlink_clk is used as the sampling clock for the Signal Tap.	• The j204c_rx_sh_lock is asserted. • The j204c_rx_int signal is deasserted if there is no error.

(1) The error interrupts that are enabled by default is sufficient for passing criteria.

1.4.1.2. Extended Multiblock Alignment

Table 2. Extended Multiblock Alignment Test Cases

Test Case	Objective	Description	Passing Criteria
EMBA.1	Check if the Extended Multiblock Lock is asserted only after the assertion of Sync Header Lock.	The following signals in <*ip_variant_name*>_base.v are tapped: • j204c_rx_emb_lock • j204c_rx_sh_lock • j204c_rx_int(2)	• The j204c_rx_emb_lock is asserted after assertion of j204c_rx_sh_lock • The j204c_rx_int signal is deasserted if there is no error.
EMBA.2	Check if the Extended Multiblock Lock status being stable (after extended multiblock lock or until elastic buffer is released) along with no invalid multiblock.	The following signals in <*ip_variant_name*>_base.v are tapped: • j204c_rx_emb_lock • j204c_rx_int(2)	• The j204c_rx_emb_lock should remain asserted. • The j204c_rx_int signal is deasserted if there is no error.
EMBA.3	Check the lane alignment.	The following signals in <*ip_variant_name*>_base.v are tapped: • j204c_rx_dev_lane_align • j204c_rx_int(2)	• The j204c_rx_dev_lane_align is asserted after the assertion of j204c_rx_emb_lock and next LEMC event. • The j204c_rx_int signal is deasserted if there is no error.

1.4.2. Receiver Transport Layer

To check the data integrity of the payload data stream through the receiver (RX) JESD204C Intel FPGA IP and transport layer, the ADC is configured to output short and long transport layer test patterns and ramp test pattern. The ADC is also set to operate with the same configuration as set in the JESD204C Intel FPGA IP. The short and long transport layer test patterns and ramp test pattern (as defined in section 6.6 of the JESD204C specification and the *Short and Long Transport Test Mode* and *Ramp Test Mode* sections in the ADC12DJ5200RF data sheet) are observed at the data output of the RX transport layer. The ramp checker in the FPGA fabric checks ramp data integrity for one minute. For short and long transport layer test pattern, approximately 8k frame clock cycle data captured by the Signal Tap logic analyzer is exported as `.csv` file and checked for compliance. The `j204c_rx_crc_err` and `j204c_rx_cmd_par_err` signals are monitored with raising edge trigger in the Signal Tap logic analyzer for 5 minutes, while the RX JESD204C Intel FPGA IP register `rx_err` is polled continuously for zero value over 10 minutes.

(2) The error interrupts that are enabled by default is sufficient for passing criteria.

Figure 3. Data Integrity Check Using Ramp Checker

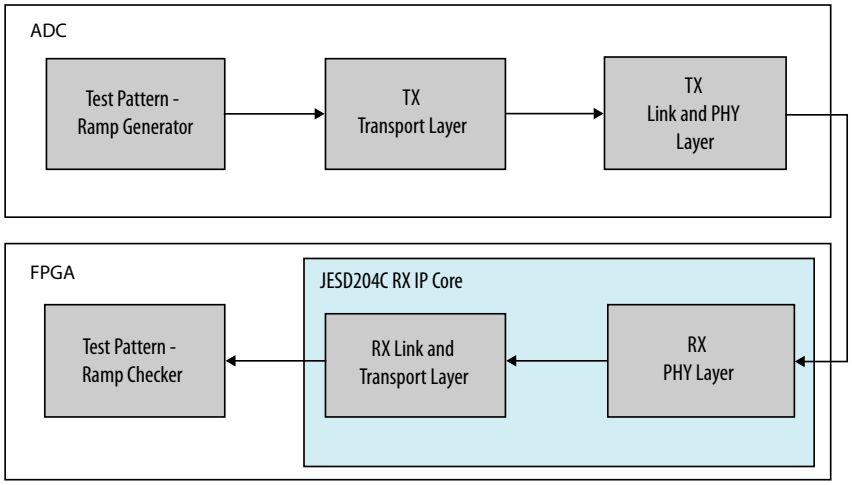


Table 3. Transport Layer Test Cases

Test Case	Objective	Description	Passing Criteria
TL.1	Check the transport layer mapping of the data channel using short transport layer test pattern.	The following signals in <*ip_variant_name*> _base.v are tapped: • j204c_rx_avst_ready • j204c_rx_avst_valid • j204c_rx_avst_data [(M*S*WIDTH_MULP*N)-1:0](3) • j204c_rx_avst_control[(M*S*WIDTH_MULP*CS)-1:0](4)(5)(6) The rxframe_clk is used as the sampling clock for the Signal Tap.	• The j204c_rx_avst_valid is asserted. • The j204c_rx_avst_ready is asserted. • No short transport layer test pattern is mismatched.
TL.2	Check the transport layer mapping of the data channel using long transport layer test pattern.	The following signals in <*ip_variant_name*> _base.v are tapped:	• The j204c_rx_avst_valid is asserted. • The j204c_rx_avst_ready is asserted. • No long transport layer test pattern is mismatched.

continued...

(3) M is the number of converters.

(4) S is the number of transmitted samples per converter per frame.

(5) WIDTH_MULP is the data width multiplier between the application layer and transport layer.

(6) N is the number of conversion bits per converter.

Test Case	Objective	Description	Passing Criteria
		• j204c_rx_avst_ready • j204c_rx_avst_valid • j204c_rx_avst_data [(M*S*WIDTH_MULP*N)-1:0](3)(4)(5)(6) • j204c_rx_avst_control [(M*S*WIDTH_MULP*CS)-1:0](3)(4)(5)(7) The rxframe_clk is used as the sampling clock for the Signal Tap.	
TL.3	Check the transport layer mapping of the data channel using ramp test pattern.	• j204c_rx_avst_ready • j204c_rx_avst_valid • j204c_rx_avst_data [(M*S*WIDTH_MULP*N)-1:0](3)(4)(5)(6) • j204c_rx_avst_control [(M*S*WIDTH_MULP*CS)-1:0](3)(4)(5)(7) The rxframe_clk is used as the sampling clock for the Signal Tap. • rx_patchk_data_error_int The rxframe_clk is used as the sampling clock for the Signal Tap. The rx_patchk_data_error_int signal indicates a pass or fail for the ramp checker.	• The j204c_rx_avst_valid is asserted. • The j204c_rx_avst_ready is asserted. • The rx_patchk_data_error_in signals is deasserted.

Related Information

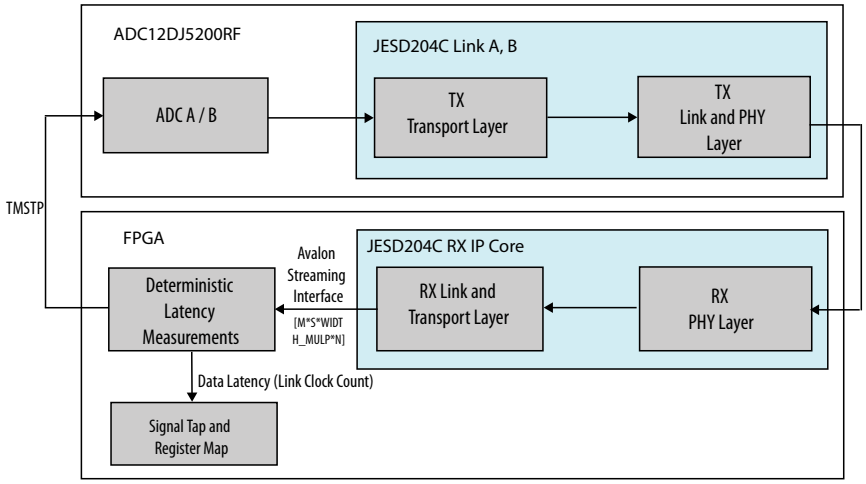
- Serial Interface for Data Converters JEDEC Standard: JESD204C
  Figure 2 —Scope of original JESD204 and revisions A, B, and C in the JESD204C JEDEC Standard visualizes a multipoint link system.
- ADC12DJ5200RF 10.4-GSPS Single-Channel or 5.2-GSPS Dual-Channel, 12-bit, RF-Sampling Analog-to-Digital Converter (ADC) Datasheet

1.4.3. Deterministic Latency (Subclass 1)

Configure the On-board Clocking option of the ADC12DJ5200RF EVM to provide periodic SYSREF to both the ADC12DJ5200RF and JESD204C Intel FPGA IP in the FPGA with the required extended multi-block period.

(7) CS is the number of control bits per conversion samples

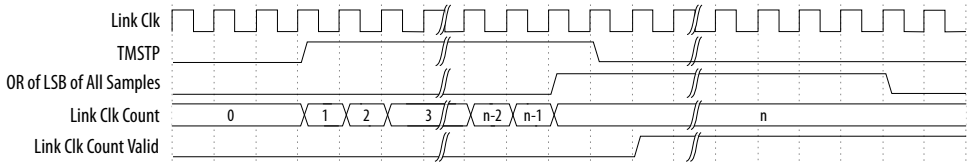
Figure 4. Deterministic Latency Measurement Block Diagram



The Timestamp feature of ADC12DJ5200RF (refer to the *Timestamp* section of the ADC12DJ5200RF data sheet) is enabled for the data latency measurement.

The deterministic latency measurement block checks the deterministic latency by measuring the number of link clock counts between the assertion of the TMSTP and the logic OR of the LSB bit of all sample at the output of the RX JESD204C Intel FPGA IP after the link is established or assertion of `j204c_rx_avst_valid`.

Figure 5. Deterministic Latency Measurement Timing Diagram



With the setup in Figure 2 on page 5, three test cases were defined to prove deterministic latency. The JESD204C Intel FPGA IP does continuous SYSREF detection.

Table 4. Deterministic Latency Test Cases

Test Case	Objective	Description	Passing Criteria
DL.1	Check the FPGA SYSREF single detection.	Check that the FPGA detects the first rising edge of SYSREF pulse. • Read the status of `sysref_singledet` (bit[2]) identifier in `rx_sysref_ctrl` register at address `0x54`. • Read the status of `sysref_lemc_err` (bit[0]) identifier in the `rx_err` register at address `0x60`.	• The value of `sysref_singledet` identifier should be zero. • The value of `sysref_lemc_err` identifier should be zero.
DL.2	Check the SYSREF capture.	Check that FPGA and ADC capture SYSREF correctly and restart the LEM counter. Both FPGA and ADC are also repetitively reset.	If the SYSREF is captured correctly and the LEM counter restarts, for every reset, the `rbd_count` value should only

continued...

Test Case	Objective	Description	Passing Criteria
		• Read the value of `rbd_count` (bit[18:10]) identifier in `rx_status` register at address `0x80`.	drift within 1 to 2 link clocks to accommodate for worst case power cycle variation.
DL.3	Check the data latency during user data phase.	Check that the data latency is consistent for every FPGA and ADC reset and power cycle (using the Timestamp feature of ADC12DJ5200RF shown in Figure 4 on page 13). • The deterministic latency measurement block in Figure 2 on page 5 has a counter to measure the link clock count.	The link clock count value should only drift within 1 to 2 link clocks for at least 10 power cycle tests.

Related Information

ADC12DJ5200RF 10.4-GSPS Single-Channel or 5.2-GSPS Dual-Channel, 12-bit, RF-Sampling Analog-to-Digital Converter (ADC) Datasheet

1.5. JESD204C Intel FPGA IP and ADC Configurations

The JESD204C Intel FPGA IP parameters (L, M, and F) in this hardware checkout are natively supported by the ADC12DJ5200RF device. The transceiver data rate, sampling clock, and other JESD204C parameters comply with the ADC12DJ5200RF operating conditions.

The hardware checkout testing implements the JESD204C Intel FPGA IP with the following parameter configuration

Global setting for all configuration:

- E = 1
- CF = 0
- Subclass = 1
- SH_CONFIG = CRC-12
- FCLK_MULP = 1
- FPGA Management Clock (MHz) = 100

Note:

- The other configurations are retained at default values.
- The polarity of the DB0 to DB7 lanes of ADC12DJ5200RF EVM are inverted.

Table 5. Parameter Configuration

LMF	N	NP	S	CS	HD	ADC Sampling Clock (MHz)	FPGA Device Clock (MHz)(8)	FPGA Frame / Link Clock (MHz) (9)	Lane Rate (Gbps)	DDC Enabled	Decimation Factor	Data Pattern
828	12	12	20	0	0	3000	150.00	75.00	9.9	No	1	Short
612	12	12	8	0	1	2500	156.25	78.125	10.3125	No	1	Short
622	12	12	4	0	1	2500	156.25	78.125	10.3125	No	1	Short
411	8	8	4	0	0	2500	156.25	78.125	10.3125	No	1	Short
421	8	8	2	0	0	2500	156.25	78.125	10.3125	No	1	Short
422	15	16	2	1	0	2500	156.25	78.125	10.3125	Yes	4	Long
442	15	16	1	1	0	2500	156.25	78.125	10.3125	Yes	4	Long
222	15	16	1	1	0	2500	156.25	78.125	10.3125	Yes	8	Long
244	15	16	1	1	0	2500	156.25	78.125	10.3125	Yes	8	Long
881	8	8	1	0	0	3000	150.00	75.00	9.9	No	1	Ramp
661	8	8	1	0	0	2500	156.25	78.125	10.3125	No	1	Ramp
828	12	12	20	0	0	5200	260.00	130.00	17.16	No	1	Short
612	12	12	8	0	1	4000	250.00	125.00	16.5	No	1	Short
622	12	12	4	0	1	4000	250.00	125.00	16.5	No	1	Short
411	8	8	4	0	0	4000	250.00	125.00	16.5	No	1	Short
421	8	8	2	0	0	4000	250.00	125.00	16.5	No	1	Short
422	15	16	2	1	0	4000	250.00	125.00	16.5	Yes	4	Long
442	15	16	1	1	0	4000	250.00	125.00	16.5	Yes	4	Long
222	15	16	1	1	0	4000	250.00	125.00	16.5	Yes	8	Long
244	15	16	1	1	0	4000	250.00	125.00	16.5	Yes	8	Long
881	8	8	1	0	0	5200	260.00	130.00	17.16	No	1	Ramp
661	8	8	1	0	0	4000	250.00	125.00	16.5	No	1	Ramp

1.6. Test Results

The following table contains the possible results and their definition.

(8) The device clock is used to clock the E-tile transceiver as well as the core PLL of the JESD204C IP.

(9) The frame clock and link clock are derived from the device clock using an internal Core PLL.

Table 6. Results Definition

Result	Definition
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with comments	The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included (example: due to time limitations, only a portion of the testing was performed).
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Refer to comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.

The following table shows the results for test cases SHA.1, SHA.2, EMBA.1, EMBA.2, EMBA.3, TL.1/TL.2/TL.3, and TL.4 with different values of L, M, F, data rate, sampling clock, link clock, and SYSREF frequencies.

Table 7. Result for Test Cases SHA.1, SHA.2, EMBA.1, EMBA.2, EMBA.3, TL.1/TL.2/TL.3, and TL.4

Test No.	L	M	F	Data Rate (Gbps)	ADC Sampling Clock (MHz)	Link Clock (MHz)	Result
1	8	2	8	9.9	3000	75.00	PASS
2	6	1	2	10.3125	2500	78.125	PASS
3	6	2	2	10.3125	2500	78.125	PASS
4	4	1	1	10.3125	2500	78.125	PASS
5	4	2	1	10.3125	2500	78.125	PASS
6	4	2	2	10.3125	2500	78.125	PASS
7	4	4	2	10.3125	2500	78.125	PASS
8	2	2	2	10.3125	2500	78.125	PASS
9	2	4	4	10.3125	2500	78.125	PASS
10	8	8	1	9.9	3000	75.00	PASS
11	6	6	1	10.3125	2500	78.125	PASS
12	8	2	8	17.16	5200	130.00	PASS
13	6	1	2	16.5	4000	125.00	PASS
14	6	2	2	16.5	4000	125.00	PASS
15	4	1	1	16.5	4000	125.00	PASS
16	4	2	1	16.5	4000	125.00	PASS
17	4	2	2	16.5	4000	125.00	PASS
18	4	4	2	16.5	4000	125.00	PASS
19	2	2	2	16.5	4000	125.00	PASS
20	2	4	4	16.5	4000	125.00	PASS
21	8	8	1	17.16	5200	130.00	PASS
22	6	6	1	16.5	4000	125.00	PASS

The following table shows the results for test cases DL.1, DL.2, and DL.3 with different values of L, M, F, data rate, sampling clock, link clock, and SYSREF frequencies.

Table 8. Result for Deterministic Latency Test

Test	L	M	F	Data Rate (Gbps)	ADC Sampling Clock (MHz)	Link Clock (MHz)	Result	RBD Count	Link Clock Latency Cycles
DL.1	8	2	8	9.9	3000	75.00	PASS	4	29
DL.2	8	2	8	9.9	3000	75.00	PASS		
DL.3	8	2	8	9.9	3000	75.00	PASS		
DL.1	6	1	2	10.3125	2500	78.125	PASS	4	30
DL.2	6	1	2	10.3125	2500	78.125	PASS		
DL.3	6	1	2	10.3125	2500	78.125	PASS		
DL.1	6	2	2	10.3125	2500	78.125	PASS	4	30
DL.2	6	2	2	10.3125	2500	78.125	PASS		
DL.3	6	2	2	10.3125	2500	78.125	PASS		
DL.1	4	1	1	10.3125	2500	78.125	PASS	4	30
DL.2	4	1	1	10.3125	2500	78.125	PASS		
DL.3	4	1	1	10.3125	2500	78.125	PASS		
DL.1	4	2	1	10.3125	2500	78.125	PASS	4	30
DL.2	4	2	1	10.3125	2500	78.125	PASS		
DL.3	4	2	1	10.3125	2500	78.125	PASS		
DL.1	4	2	2	10.3125	2500	78.125	PASS	4	N/A(10)
DL.2	4	2	2	10.3125	2500	78.125	PASS		
DL.1	4	4	2	10.3125	2500	78.125	PASS	4	N/A(10)
DL.2	4	4	2	10.3125	2500	78.125	PASS		
DL.1	2	2	2	10.3125	2500	78.125	PASS	4	N/A(10)
DL.2	2	2	2	10.3125	2500	78.125	PASS		
DL.1	2	4	4	10.3125	2500	78.125	PASS	4	N/A(10)
DL.2	2	4	4	10.3125	2500	78.125	PASS		
DL.1	8	8	1	9.9	3000	75.00	PASS	4	N/A(10)
DL.2	8	8	1	9.9	3000	75.00	PASS		
DL.1	6	6	1	10.3125	2500	78.125	PASS	4	N/A(10)
DL.2	6	6	1	10.3125	2500	78.125	PASS		
DL.1	8	2	8	17.16	5200	130.00	PASS	5	30
DL.2	8	2	8	17.16	5200	130.00	PASS		

continued...

(10) The Timestamp feature of ADC12DJ5200RF is not supported when decimation or JESD testpattern (ramp/short/long transport test pattern) is enabled in the device and hence latency is not measured for those modes.

Test	L	M	F	Data Rate (Gbps)	ADC Sampling Clock (MHz)	Link Clock (MHz)	Result	RBD Count	Link Clock Latency Cycles
DL.3	8	2	8	17.16	5200	130.00	PASS		
DL.1	6	1	2	16.5	4000	125.00	PASS	5	30
DL.2	6	1	2	16.5	4000	125.00	PASS		
DL.3	6	1	2	16.5	4000	125.00	PASS		
DL.1	6	2	2	16.5	4000	125.00	PASS	5	30
DL.2	6	2	2	16.5	4000	125.00	PASS		
DL.3	6	2	2	16.5	4000	125.00	PASS		
DL.1	4	1	1	16.5	4000	125.00	PASS	5	30
DL.2	4	1	1	16.5	4000	125.00	PASS		
DL.3	4	1	1	16.5	4000	125.00	PASS		
DL.1	4	2	1	16.5	4000	125.00	PASS	5	31
DL.2	4	2	1	16.5	4000	125.00	PASS		
DL.3	4	2	1	16.5	4000	125.00	PASS		
DL.1	4	2	2	16.5	4000	125.00	PASS	5	N/A(10)
DL.2	4	2	2	16.5	4000	125.00	PASS		
DL.1	4	4	2	16.5	4000	125.00	PASS	5	N/A(10)
DL.2	4	4	2	16.5	4000	125.00	PASS		
DL.1	2	2	2	16.5	4000	125.00	PASS	5	N/A(10)
DL.2	2	2	2	16.5	4000	125.00	PASS		
DL.1	2	4	4	16.5	4000	125.00	PASS	5	N/A(10)
DL.2	2	4	4	16.5	4000	125.00	PASS		
DL.1	8	8	1	17.16	5200	130.00	PASS	5	N/A(10)
DL.2	8	8	1	17.16	5200	130.00	PASS		
DL.1	6	6	1	16.5	4000	125.00	PASS	5	N/A(10)
DL.2	6	6	1	16.5	4000	125.00	PASS		

1.7. Test Result Comments

In each test case, the RX JESD204C Intel FPGA IP successfully establishes the sync header alignment, extended multiblock alignment, and until user data phase.

No data integrity issue is observed by the ramp checker for JESD configurations at different lanes rates covering all physical lanes, also no cyclic redundancy check (CRC) and command parity error is observed.

In the deterministic latency measurement, consistent RBD count and total latency between the TMSTP input of the ADC and the JESD Intel FPGA IP transport layer output are observed across multiple power cycles or resets.

The modes LMF 881 and 661 are not valid ADC operation modes supported by the ADC12DJ5200RF device but are JESD204C ramp test pattern modes used to test all the physical lanes involved at different lane rates for data integrity errors.

1.8. Document Revision History for AN 909: JESD204C Intel FPGA IP and TI ADC12DJ5200RF Interoperability Report for Intel Stratix 10 Devices

Document Version	Changes
2020.06.09	• Added a step in *ADC12DJxx00RF EVM Software and JESD204C Example Design Setup*. • Updated *Appendix* to state that this interoperability report refers to the April 2019 version of the ADC12DJ5200RF datasheet and EVM GUI.
2020.05.11	Initial release.

1.9. Appendix

Intel Quartus® Prime Pro Edition software version 19.2 Build 57 is used for compilation of designs.

This interoperability report refers to the April 2019 version of the ADC12DJ5200RF datasheet and EVM GUI.

Additional JESD mode support by ADC

The 64/66 B mode enlisted here have not been validated in this interoperability test, but they are supported by the ADC12DJ5200RF device. It is tabulated here for future reference.

LMF	S	N	N'	Comments
818	40	12	12	S=40 is not supported by JESD204C Intel FPGA IP.