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1. About the 5G Wireless Acceleration Reference Design

The 5G Wireless Acceleration reference design provides additional IP (Intel FPGA IP and software drivers) to support fronthaul IO and 5G channel coding (forward error correction (FEC)).

The Intel FPGA PAC N3000 provides an on-board PCIe switch that connects fronthaul and 5G channel coding functions to a PCIe Gen3x16 edge connector. The Intel FPGA PAC N3000 is a general-purpose acceleration card for networking.

Figure 1. Data flow for the user image, FEC, and Fronthaul IO

1.1. 5G User Image Features

FEC features:
- Functionality independent of 25G I/O (look-aside model)
- Support for one physical function (PF) and 8 virtual functions (VFs) simultaneously accessing acceleration
- 64 queues supported equally split between uplink and downlink.
- LDPC transmitter with interleaving and rate matching
- LDPC receiver with de-interleaving function and reverse rate matching.
- Load balancer distributes the pending requests to transmitter and receiver
- Early termination CRC24B
- Software enablement by baseband device (bbdev) API (targeted to upstream to Data Plane Development Kit (DPDK)
- Function-level reset

Fronthaul IO features:
- 25G MAC and 25G PHY IP connectivity to retimer and a quad small form factor pluggable (QSFP).
- 40G MAC and 40G PHY IP connectivity to Intel XL710 networking device
- Gearbox to enable 25G connectivity to QSFP.
- In-line compression and decompression.
- Software enablement by Open Platform Acceleration Environment (OPAE), DPDK and bbdev.

Related Information
5G LDPC-V Intel FPGA IP User Guide

1.2. About the Intel PAC N3000

You enable the Intel PAC N3000 through six main firmware components. Five components are not specific to wireless but are for FPGA workload. Intel also provides a software package for the Intel PAC N3000.

The Intel PAC N3000 supports the factory image with RSU capability in on-board 1 Gb flash in page 0 as a fail over image. The user image is stored in 1 Gb flash.

Intel develops and owns all of the following Intel PAC N3000 components (including all updates) except the Intel® Arria® 10 flash page 1 user image:
- Intel MAX® 10 Nios flash.
  - Fixed configuration. RSU capable. Intel loads the binary image.
- PCIe software.
  - Intel flashes the binary images.
  - Fixed configuration for PCIe configuration.
  - Not RSU capable.
- Intel C827 retimer.
  - Intel flashes the binary EEPROM.
  - Power-up configuration initialization by Intel Arria 10 soft Nios processor through Intel MAX 10.
  - Fixed configuration for XCVR.
  - Encrypted.
• Intel XL710.
  — Intel flashes the binary images.
  — Fixed configuration for XCVR configuration.
  — RSU capable.
• Intel Arria 10 flash factory image page 0.
  — Intel flashes the binary images.
  — Not RSU capable.
• Intel Arria 10 flash page 1 user image.
  — RSU capable.
  — Intel provides the top-level reference design under a software license agreement.
  — Contains multiple encrypted IP blocks provided under a software license agreement.
  — You own the production image and design.

**Related Information**

- Intel® FPGA PAC N3000 AFU Developer Guide
- Intel® FPGA PAC N3000 Data Sheet
- Intel Acceleration Stack User Guide: Intel FPGA Programmable Acceleration Card N3000

### 1.2.1. Factory Image for 2x2x25 GbE

Page 0 of the flash contains the factory image. This image tests and diagnoses the Intel PAC N3000.

The factory image:

- Tests the image that enables PCIe, Ethernet, and memory diagnostics:
  — PCIe near-end loopback testing
  — Memory testing using DMA reads and writes
  — Ethernet loopback test
- Enables the RSU for the user image in flash

If the user image update fails, the Intel PAC N3000 restarts with the factory image, you can then reload the image.
Figure 2. Factory Image Block Diagram for 2x2x25 GbE
2. 5G User Image Description

The user image performs fronthaul IO and 5G channel coding. Contact Intel for the user image.

Figure 3. 5G User Image

2.1. User Image Power Management

On board power monitoring restricts the board temperature to 100°C. In the event of reaching this limit, the board is automatically shut down. The user image power consumption and thermal profile must fit within this envelope.

For different situations with different functions, the power consumptions are different. As a reference point, the raw power consumption of an FPGA is about 60 W @ 100°C junction temperature. The Intel PAC N3000 card power consumption is about 100 W.
2.2. 5G Channel Coder

You should send and receive code blocks for the encoder and decoder over PCIe to or from the host using the descriptor format defined in the Data Plane Development Kit (DPDK) and the baseband device. Contact Intel for the descriptor format.

The channel coders queue and process these blocks based on the load balancing decisions.

Figure 4. 5G Channel Coder

The downlink FEC accelerator consists of the 5G LDPC-V transmitter and the uplink FEC accelerator consists of the 5G LDPC-V receiver. The input to the downlink FEC accelerator is 32-bit data and the output data is 32-bit wide. For more information on the 5G LDPC-V transmitter and receiver, refer to the 5G LDPC-V Intel FPGA IP User Guide.

Figure 5. Transmitter Signals

This figure does not show the Avalon streaming interface signals.
2.2.1. 5G Channel Coder Throughput

The Intel FPGA PAC N3000 5G channel coder accelerator contains two encoders and two decoders. The throughput depends on the traffic model.

For a single encoder, the clock rate, code block size (base graph number, lifting factor), code rate affect the throughput. The maximum throughput occurs when graph number = 1, lifting factor = 384, and the code rate = 1/3. In this case, the throughput is 5.7 Gbps. Two encoders achieve a maximum throughput of 11.4 Gbps.

For a single decoder, the clock rate, code block size (base graph number, lifting factor), code rate, and iteration number affect the throughput. The maximum throughput occurs when graph number = 1, lifting face = 384, code rate = 8/9 and iteration number = 1. In this case, the throughput is 18.438 Gbps. Two decoders achieve a maximum theoretical throughput of 36.876 Gbps.

2.2.2. 5G LDPC-V Transmitter and Receiver Tests

Intel tests the transmitters and receivers by simulating with 2112 test patterns. Each test uses different values or sizes for base graph, Zc value, K’ value, code rate, Qm, E value, k0 value, ON/OFF code block CRC

Table 1. Test Cases for the Downlink

<table>
<thead>
<tr>
<th>test case</th>
<th>BG</th>
<th>Zc</th>
<th>K’</th>
<th>Code Rate</th>
<th>Qm</th>
<th>E</th>
<th>k0</th>
<th>CRC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>10</td>
<td>184</td>
<td>1/3</td>
<td>1</td>
<td>300</td>
<td>0</td>
<td>ON</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>20</td>
<td>400</td>
<td>1/2</td>
<td>4</td>
<td>520</td>
<td>0</td>
<td>ON</td>
</tr>
</tbody>
</table>

continued...
Table 2. Test Cases for the Uplink

<table>
<thead>
<tr>
<th>Test Case</th>
<th>BG</th>
<th>Zc</th>
<th>K'</th>
<th>Code Rate</th>
<th>Qm</th>
<th>E</th>
<th>K0</th>
<th>CRC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>10</td>
<td>216</td>
<td>1/3</td>
<td>2</td>
<td>280</td>
<td>330</td>
<td>ON</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>20</td>
<td>440</td>
<td>1/2</td>
<td>6</td>
<td>504</td>
<td>440</td>
<td>ON</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>40</td>
<td>880</td>
<td>3/4</td>
<td>6</td>
<td>882</td>
<td>0</td>
<td>ON</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>10</td>
<td>216</td>
<td>8/9</td>
<td>2</td>
<td>240</td>
<td>0</td>
<td>OFF</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>4</td>
<td>80</td>
<td>2/3</td>
<td>2</td>
<td>80</td>
<td>32</td>
<td>OFF</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>5</td>
<td>96</td>
<td>2/3</td>
<td>6</td>
<td>102</td>
<td>0</td>
<td>OFF</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>240</td>
<td>2400</td>
<td>1/2</td>
<td>6</td>
<td>2802</td>
<td>0</td>
<td>ON</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>256</td>
<td>2560</td>
<td>1/3</td>
<td>4</td>
<td>3200</td>
<td>256</td>
<td>ON</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>9</td>
<td>80</td>
<td>1/3</td>
<td>8</td>
<td>96</td>
<td>54</td>
<td>ON</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>80</td>
<td>800</td>
<td>1/3</td>
<td>8</td>
<td>840</td>
<td>1600</td>
<td>OFF</td>
</tr>
</tbody>
</table>

Related Information
5G LDPC-V Intel FPGA IP User Guide

2.2.3. 5G VRAN Universal Verification Methodology

The vRAN universal verification methodology (UVM) simulation test environment for the 5G channel coder incorporates the transmitter or receiver and the DMA subsystem. The test environment does not include the preverified transaction layer packet (TLP) adapter.

The tests randomly select 2,000 test patterns from 110,000 test patterns to test the decoding function and randomly selects 2,000 test patterns from 110,000 test patterns to test the encoding function. The tests also test the randomization (and functional coverage) of system scenarios such as HARQ, physical and virtual function (PF and VF) access, queue flushing, and reset. The reference design includes the UVM test plan, 5G_LDPC_Test_Plan.xls.
2.3. Fronthaul IO

The fronthaul IO is a simple passthrough pipe.

2.3.1. O-RAN Compression and Decompression

The compression and decompression IP supports both block floating point and Mu-Law compression methods.

Internally, the design collects the 12 resource elements in a resource block and determines the maximum magnitude. It then performs block floating-point shifting and Mu-Law compression or decompression.
Figure 10. Compression and Decompression 16:8 bit Example

Related Information
ORAN Alliance

2.4. User Image Software

The user image requires software components and drivers, which support the descriptor format and physical function drivers.

Figure 11. User Image Architecture

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020.01.30</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>