AN 871: Quick Guide for Intel® Arria® 10 and Intel® Cyclone® 10 GX Transceiver High-Speed Link Tuning
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1. High-Speed Link Tuning Requirements

If high channel loss causes bit error rates (BER) higher than the protocol target BER, you must tune your high-speed links to find optimum equalization values.

To determine if the high BER is due to high channel loss, enable serial loopback with RX VGA setting 0; then check if the high BER persists (serial loopback enables an internal datapath that bypasses the high-speed channel).

![Serial Loopback Diagram](image)

If the BER is now acceptable, the high BER was caused by high channel loss. In this case, you must perform high-speed link tuning as described in this document. Else, if the BER is still high, the BER was not caused by high channel loss, and you must debug your transceiver PHY (see Optimizing for Crosstalk at High Datarates).

For a high BER that is caused by high channel loss, transceivers offer equalization techniques on both the TX and RX sides in order to compensate for the high channel loss due to PCB traces, high speed connectors, PDN noise, and crosstalk.

To select the optimum equalization values, use the Auto Sweep feature on the Advanced tab of the Transceiver Toolkit to sweep the analog settings.

Find the optimum equalization values through the following steps. These detailed steps use a 10 inch backplane as the baseline.

1. **Enabling and Setting up the Transceiver Toolkit**
2. **Sweeping Your Settings**
3. **Optimizing Your Settings**
4. **Optimizing for Crosstalk at High Datarates**

**Related Information**
- Enabling and Setting up the Transceiver Toolkit on page 4
- Sweeping Your Settings on page 5
- Optimizing Your Settings on page 6
1. High-Speed Link Tuning Requirements

1.1. Enabling and Setting up the Transceiver Toolkit

1. Follow the steps in the Quartus Debugging Transceiver Links chapter of the Debug Tools User Guide: Intel Quartus Prime Pro Edition to enable the Transceiver Toolkit with the Transceiver PHY.

2. Open the Transceiver Toolkit.

Figure 2. Example: Receiver Channels Tab of the Channel Manager

3. Select the following equalization settings as your starting point (the initial values) for high-speed link tuning.

Table 1. Initial Values

<table>
<thead>
<tr>
<th>Analog Parameter Settings</th>
<th>≤ 5 Gbps</th>
<th>&gt;5 Gbps to 10 Gbps</th>
<th>&gt;10 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX VOD</td>
<td>31</td>
<td>31</td>
<td>31</td>
</tr>
<tr>
<td>TX Pre-emphasis First Post-Tap (1) (2)</td>
<td>-13</td>
<td>-13</td>
<td>-13</td>
</tr>
<tr>
<td>RX Equalizer Stage</td>
<td>1-stage (S1_MODE) or 4-stage (NON_S1_MODE)</td>
<td>4-Stage (NON_S1_MODE)</td>
<td>4-Stage (NON_S1_MODE)</td>
</tr>
</tbody>
</table>

(1) You must adhere to the TX eye mask for specific protocols; thus, post-tap may change per protocol requirements.

(2) Set TX Pre-emphasis 2nd Post-Tap, 1st Pre-Tap and 2nd Pre-Tap to setting value 0.
1. High-Speed Link Tuning Requirements

## Analog Parameter Settings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>≤ 5 Gbps</th>
<th>&gt;5 Gbps to 10 Gbps</th>
<th>&gt;10 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX CTLE AC Gain</td>
<td>10</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>RX CTLE DC Gain</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>RX VGA</td>
<td>0</td>
<td>3</td>
<td>4</td>
</tr>
</tbody>
</table>

4. Disable the settings not listed above.

5. From the following table, select the test pattern based on the encoding scheme used in your design.

### Table 2. Test Pattern

<table>
<thead>
<tr>
<th>Line Code</th>
<th>≤ 5 Gbps</th>
<th>&gt;5 Gbps to 10 Gbps</th>
<th>&gt;10 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>No encoding</td>
<td>PRBS7</td>
<td>PRBS15</td>
<td>PRBS31</td>
</tr>
<tr>
<td>8b/10b encoding</td>
<td>PRBS15</td>
<td>PRBS23</td>
<td>-</td>
</tr>
<tr>
<td>64b/66b encoding</td>
<td>PRBS23</td>
<td>PRBS23</td>
<td>PRBS31</td>
</tr>
</tbody>
</table>

**Related Information**
- Transceiver Toolkit

### 1.2. Sweeping Your Settings

1. Capture the BER for 5 to 10 seconds for each setting. This is your initial equalization setting.

2. If your initial equalization setting shows an acceptable BER, proceed to *Optimizing Your Settings*.

3. If your initial equalization setting shows a high BER, use the Auto Sweep feature on the Advanced tab of the Transceiver Toolkit to sweep the RX settings in the following order (refer to the "Acceptable BER Example Values" table for the starting and ending sweep values):
   - CTLE AC gain
   - VGA up to a maximum of four (depending on the data rate)
   - CTLE DC gain/EQ, increasing

4. If the BER is now acceptable, proceed to *Optimizing Your Settings*.

5. For the Intel® Arria® 10 device only, if the BER remains high, enable DFE trigger adaptation (3). If the BER is now acceptable, proceed to *Optimizing Your Settings*. If the BER remains high, disable DFE trigger adaptation.

6. If the BER remains high, change the settings back to the initial equalization setting (as shown in Table 1 on page 4) and sweep the TX settings in the following order (refer to the "Acceptable BER Example Values" table for the starting and ending sweep values):
   - TX Pre-emphasis Post-Tap 1
   - TX VOD

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(3) DFE is only available in Intel Arria 10 devices. All steps involving DFE usage mentioned in this chapter are only applicable to Intel Arria 10 devices, and not to Intel Cyclone® 10 GX devices.
c. TX Pre-emphasis Post-Tap 2  
d. TX Pre-emphasis Pre-Tap 1  
e. TX Pre-emphasis Pre-Tap 2

7. If the BER is now acceptable, proceed to Optimizing Your Settings.
8. For the Intel Arria 10 device only, if the BER remains high, return to the initial TX analog settings shown above based on datarate, enable DFE trigger adaptation, and sweep the TX settings again as described in Step 6 on page 5. If the BER is now acceptable, proceed to Optimizing Your Settings.
9. If the BER remains high, follow the instructions in Optimizing for Crosstalk at High Datarates.

Related Information
- Refer to the "Acceptable BER Example Values" table for the starting and ending sweep values on page 6
- Optimizing Your Settings on page 6
- Optimizing for Crosstalk at High Datarates on page 7
- Transceiver Toolkit

1.3. Optimizing Your Settings

1. When the BER is acceptable, use the Auto Sweep feature on the Advanced tab of the Transceiver Toolkit to sweep the values in the Transceiver Toolkit to determine the settings that meet the BER $10^{-12}$ condition.

Table 3. Acceptable BER Example Values

<table>
<thead>
<tr>
<th>Datarate</th>
<th>Acceptable BER(4)</th>
<th>Auto Sweep Range(5)</th>
<th>Range Guide</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX VOD</td>
<td>31</td>
<td>31</td>
<td>If the maximum VOD is used, do not sweep the VOD. Otherwise, sweep ± 5 of the values.</td>
</tr>
<tr>
<td>Pre-emphasis First Post-Tap</td>
<td>-8</td>
<td>0 to -18</td>
<td>If negative, only sweep across negative values. If positive, only sweep across positive values. Sweep ± 10 of the values.</td>
</tr>
<tr>
<td>Pre-emphasis First Pre-Tap</td>
<td>-3</td>
<td>-3 to -12 (maximum)</td>
<td>If negative, only sweep across negative values. If positive, only sweep across positive values. Sweep all positive or negative values.</td>
</tr>
<tr>
<td>Equalizer Stage</td>
<td>Single</td>
<td>Single</td>
<td>Fixed</td>
</tr>
<tr>
<td>CTLE AC Gain</td>
<td>15</td>
<td>5 to 25</td>
<td>Sweep ± 10 of the values.</td>
</tr>
</tbody>
</table>

(4) Example settings after there has been an acceptable BER for 5 seconds

(5) Range of values derived from the Auto Sweep feature on the Advanced tab of the Transceiver Toolkit that meet the BER $10^{-12}$ condition
1. High-Speed Link Tuning Requirements

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### Table 4. BER 10⁻¹² Condition PASS Settings Example

The green boxes indicate settings that pass, and the red boxes indicate settings that fail.

<table>
<thead>
<tr>
<th>CTLE AC gain settings</th>
<th>BER</th>
<th>BER</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>BER</th>
<th>BER</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTLE AC gain settings</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>14</td>
<td>15</td>
</tr>
<tr>
<td>VGA</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>BER</td>
<td>BER</td>
<td>BER</td>
<td>BER</td>
<td>BER</td>
<td>BER</td>
<td>BER</td>
</tr>
<tr>
<td>DFE Adaptation</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>14</td>
<td>15</td>
</tr>
</tbody>
</table>

In this example, the following settings can be selected as optimum values:
- CTLE AC gain = 10 or 11
- VGA = 3
- TX Pre-emphasis Post-Tap 1 = -11 (Make sure your Post-Tap setting is a negative value.)

3. Using the Transceiver Toolkit, test the optimized BER 10⁻¹² PASS settings across more channels, boards, or both. If you are unable to, repeat Step 2 on page 7 to determine the overlapping range across more channels and the board.

### Related Information

Transceiver Toolkit

### 1.4. Optimizing for Crosstalk at High Datarates

A high-speed link may suffer from near-end crosstalk at high datarates (rates greater than 17 Gbps). The higher the datarate, the more likely it is for crosstalk to contribute to a high BER. When the Transceiver Toolkit’s **Auto Sweep** feature does not yield a satisfactory result, you must compensate for crosstalk components.

1. Use TX Pre-emphasis Post-Tap 1 and RX CTLE to mitigate the crosstalk effect.
   a. Tune each channel sequentially with all neighboring channels disabled.
   b. After tuning each channel, enable all channels concurrently with the respective channels’ optimized settings.

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(4) Example settings after there has been an acceptable BER for 5 seconds
(5) Range of values derived from the **Auto Sweep** feature on the **Advanced** tab of the Transceiver Toolkit that meet the BER 10⁻¹² condition
c. If not all channels have acceptable BERs, evaluate each channel with the Transceiver Toolkit.

2. When you run multiple concurrent channels, a crosstalk component may cause one or more (not all) channels to have a high BER. For the victim channel, repeat Optimizing Your Settings to increase the (TX) Post-Tap and (RX) CTLE until the BER is acceptable.

Related Information
- Optimizing Your Settings on page 6
- Intel Arria 10 Transceiver PHY User Guide
- Intel Cyclone 10 GX Transceiver PHY User Guide
- Transceiver Toolkit

1.5. Document Revision History for AN 871: Quick Guide for Intel Arria 10 and Intel Cyclone 10 GX Transceiver High-Speed Link Tuning

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Changes</th>
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<tbody>
<tr>
<td>2018.09.26</td>
<td>Initial release.</td>
</tr>
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</table>