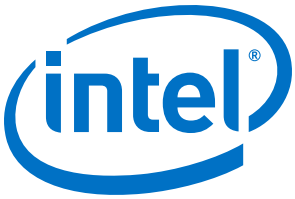

AN 871: Quick Guide for Intel® Arria® 10 and Intel® Cyclone® 10 GX Transceiver High-Speed Link Tuning

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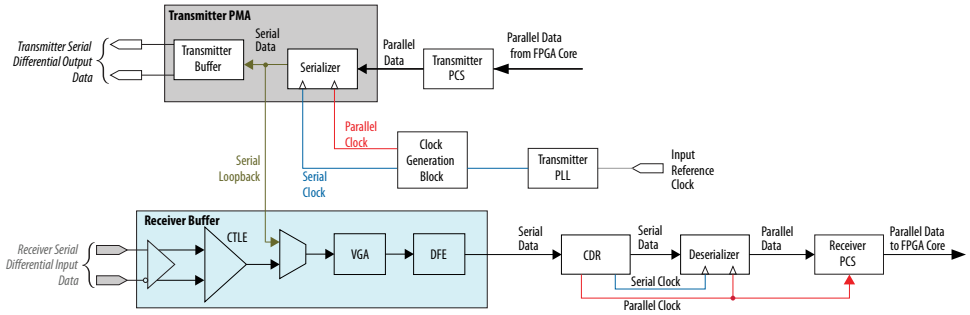
Contents

1. High-Speed Link Tuning Requirements

If high channel loss causes bit error rates (BER) higher than the protocol target BER, you must tune your high-speed links to find optimum equalization values.

To determine if the high BER is due to high channel loss, enable serial loopback with RX VGA setting 0; then check if the high BER persists (serial loopback enables an internal datapath that bypasses the high-speed channel).

Figure 1. Serial Loopback



If the BER is now acceptable, the high BER was caused by high channel loss. In this case, you must perform high-speed link tuning as described in this document. Else, if the BER is still high, the BER was not caused by high channel loss, and you must debug your transceiver PHY (see *Optimizing for Crosstalk at High Datarates*).

For a high BER that is caused by high channel loss, transceivers offer equalization techniques on both the TX and RX sides in order to compensate for the high channel loss due to PCB traces, high speed connectors, PDN noise, and crosstalk.

To select the optimum equalization values, use the **Auto Sweep** feature on the **Advanced** tab of the Transceiver Toolkit to sweep the analog settings.

Find the optimum equalization values through the following steps. These detailed steps use a 10 inch backplane as the baseline.

1. *Enabling and Setting up the Transceiver Toolkit*
2. *Sweeping Your Settings*
3. *Optimizing Your Settings*
4. *Optimizing for Crosstalk at High Datarates*

Related Information

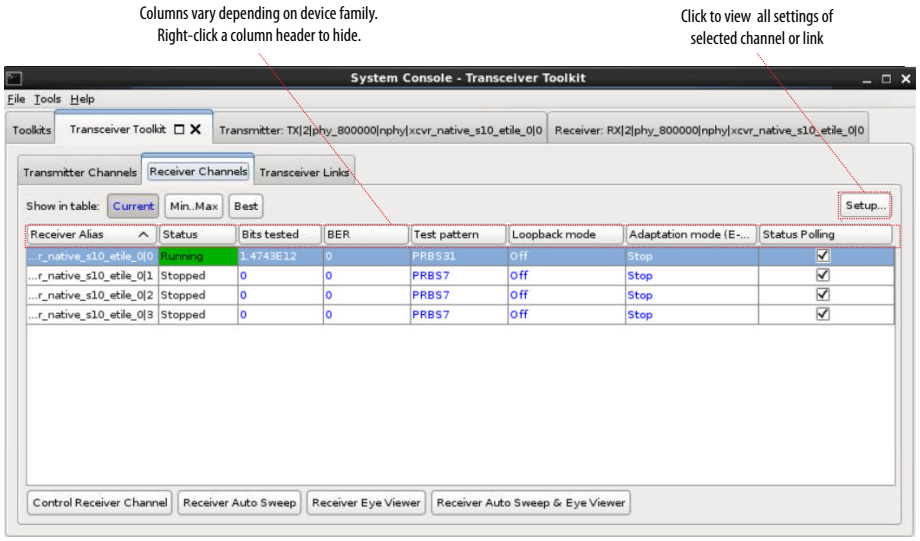
- Enabling and Setting up the Transceiver Toolkit on page 4
- Sweeping Your Settings on page 5
- Optimizing Your Settings on page 6

- Optimizing for Crosstalk at High Datarates on page 7
- Intel® Arria® 10 Transceiver PHY User Guide
- Intel® Cyclone® 10 GX Transceiver PHY User Guide
- Transceiver Toolkit

1.1. Enabling and Setting up the Transceiver Toolkit

1. Follow the steps in the Quartus Debugging Transceiver Links chapter of the *Debug Tools User Guide: Intel Quartus Prime Pro Edition* to enable the Transceiver Toolkit with the Transceiver PHY.
2. Open the Transceiver Toolkit.

Figure 2. Example: Receiver Channels Tab of the Channel Manager



3. Select the following equalization settings as your starting point (the initial values) for high-speed link tuning.

Table 1. Initial Values

Analog Parameter Settings	≤ 5 Gbps	>5 Gbps to 10 Gbps	>10 Gbps
TX VOD	31	31	31
TX Pre-emphasis First Post-Tap(1) (2)	-13	-13	-13
RX Equalizer Stage	1-stage (S1_MODE) or 4-stage (NON_S1_MODE)	4-Stage (NON_S1_MODE)	4-Stage (NON_S1_MODE)

continued...

(1) You must adhere to the TX eye mask for specific protocols; thus, post-tap may change per protocol requirements.

(2) Set TX Pre-emphasis 2nd Post-Tap, 1st Pre-Tap and 2nd Pre-Tap to setting value 0.

Analog Parameter Settings	≤ 5 Gbps	>5 Gbps to 10 Gbps	>10 Gbps
RX CTLE AC Gain	10	15	15
RX CTLE DC Gain	1	1	1
RX VGA	0	3	4

4. Disable the settings not listed above.
5. From the following table, select the test pattern based on the encoding scheme used in your design.

Table 2. Test Pattern

Line Code	≤ 5 Gbps	>5 Gbps to 10 Gbps	>10 Gbps
No encoding	PRBS7	PRBS15	PRBS31
8b/10b encoding	PRBS15	PRBS23	-
64b/66b encoding	PRBS23	PRBS23	PRBS31

Related Information

- Transceiver Toolkit
- Debug Tools User Guide: Intel Quartus Prime Pro Edition

1.2. Sweeping Your Settings

1. Capture the BER for 5 to 10 seconds for each setting. This is your initial equalization setting.
2. If your initial equalization setting shows an acceptable BER, proceed to *Optimizing Your Settings*.
3. If your initial equalization setting shows a high BER, use the **Auto Sweep** feature on the **Advanced** tab of the Transceiver Toolkit to sweep the RX settings in the following order (refer to the "Acceptable BER Example Values" table for the starting and ending sweep values):
   a. CTLE AC gain
   b. VGA up to a maximum of four (depending on the datarate)
   c. CTLE DC gain/EQ, increasing
4. If the BER is now acceptable, proceed to *Optimizing Your Settings*.
5. For the Intel® Arria® 10 device only, if the BER remains high, enable DFE trigger adaptation [(3)]. If the BER is now acceptable, proceed to *Optimizing Your Settings*. If the BER remains high, disable DFE trigger adaptation.
6. If the BER remains high, change the settings back to the initial equalization setting (as shown in Table 1 on page 4) and sweep the TX settings in the following order (refer to the "Acceptable BER Example Values" table for the starting and ending sweep values):
   a. TX Pre-emphasis Post-Tap 1
   b. TX VOD

(3) DFE is only available in Intel Arria 10 devices. All steps involving DFE usage mentioned in this chapter are only applicable to Intel Arria 10 devices, and not to Intel Cyclone® 10 GX devices

c. TX Pre-emphasis Post-Tap 2
d. TX Pre-emphasis Pre-Tap 1
e. TX Pre-emphasis Pre-Tap 2

7. If the BER is now acceptable, proceed to *Optimizing Your Settings*.
8. For the Intel Arria 10 device only, if the BER remains high, return to the initial TX analog settings shown above based on datarate, enable DFE trigger adaptation, and sweep the TX settings again as described in Step 6 on page 5. If the BER is now acceptable, proceed to *Optimizing Your Settings*.
9. If the BER remains high, follow the instructions in *Optimizing for Crosstalk at High Datarates*.

Related Information

- Refer to the "Acceptable BER Example Values" table for the starting and ending sweep values on page 6
- Optimizing Your Settings on page 6
- Optimizing for Crosstalk at High Datarates on page 7
- Transceiver Toolkit

1.3. Optimizing Your Settings

1. When the BER is acceptable, use the **Auto Sweep** feature on the **Advanced** tab of the Transceiver Toolkit to sweep the values in the Transceiver Toolkit to determine the settings that meet the BER 10^{-12} condition.

Table 3. Acceptable BER Example Values

Datarate	Acceptable BER(4)	Auto Sweep Range(5)	Range Guide
TX VOD	31	31	If the maximum VOD is used, do not sweep the VOD. Otherwise, sweep ± 5 of the values.
Pre-emphasis First Post-Tap	-8	0 to -18	If negative, only sweep across negative values. If positive, only sweep across positive values. Sweep ± 10 of the values.
Pre-emphasis First Pre-Tap	-3	-3 to -12 (maximum)	If negative, only sweep across negative values. If positive, only sweep across positive values. Sweep all positive or negative values.
Equalizer Stage	Single	Single	Fixed
CTLE AC Gain	15	5 to 25	Sweep ± 10 of the values.

continued...

(4) Example settings after there has been an acceptable BER for 5 seconds

(5) Range of values derived from the **Auto Sweep** feature on the **Advanced** tab of the Transceiver Toolkit that meet the BER 10^{-12} condition

Datarate	Acceptable BER[4]	Auto Sweep Range[5]	Range Guide
CTLE DC Gain	1	1	If DC gain setting 0 is used for acceptable BER, do not sweep. Else, sweep DC gain settings 1 - 4..
VGA	2	1 to 4	If the VGA setting for acceptable BER is > 0, sweep across VGA settings 1 - 4.
DFE Adaptation	Enabled	Enabled	

2. Select the middle value for the settings range that PASS for the BER 10^{-12} condition. The middle value is the optimized value.

Table 4. BER 10^{-12} Condition PASS Settings Example

The green boxes indicate settings that pass, and the red boxes indicate settings that fail.

CTLE AC gain settings	5	6	7	8	9	10	11	12	13	14	15	16	17
	BER	BER	0	0	0	0	0	0	0	0	BER	BER	BER
VGA	1	2	3	4									
	BER	0	0	0									
DFE Adaptation	5	6	7	8	9	10	11	12	13	14	15	16	17
	BER	BER	BER	BER	0	0	0	0	0	BER	BER	BER	BER

In this example, the following settings can be selected as optimum values:

- CTLE AC gain = 10 or 11
- VGA = 3
- TX Pre-emphasis Post-Tap 1 = -11 (Make sure your Post-Tap setting is a negative value.)

3. Using the Transceiver Toolkit, test the optimized BER 10^{-12} PASS settings across more channels, boards, or both. If you are unable to, repeat Step 2 on page 7 to determine the overlapping range across more channels and the board.

Related Information

Transceiver Toolkit

1.4. Optimizing for Crosstalk at High Datarates

A high-speed link may suffer from near-end crosstalk at high datarates (rates greater than 17 Gbps). The higher the datarate, the more likely it is for crosstalk to contribute to a high BER. When the Transceiver Toolkit's **Auto Sweep** feature does not yield a satisfactory result, you must compensate for crosstalk components.

1. Use TX Pre-emphasis Post-Tap 1 and RX CTLE to mitigate the crosstalk effect.
   a. Tune each channel sequentially with all neighboring channels disabled.
   b. After tuning each channel, enable all channels concurrently with the respective channels' optimized settings.

(4) Example settings after there has been an acceptable BER for 5 seconds
(5) Range of values derived from the **Auto Sweep** feature on the **Advanced** tab of the Transceiver Toolkit that meet the BER 10^{-12} condition

c. If not all channels have acceptable BERs, evaluate each channel with the Transceiver Toolkit.

2. When you run multiple concurrent channels, a crosstalk component may cause one or more (not all) channels to have a high BER. For the victim channel, repeat *Optimizing Your Settings* to increase the (TX) Post-Tap and (RX) CTLE until the BER is acceptable.

Related Information

- Optimizing Your Settings on page 6
- Intel Arria 10 Transceiver PHY User Guide
- Intel Cyclone 10 GX Transceiver PHY User Guide
- Transceiver Toolkit

1.5. Document Revision History for AN 871: Quick Guide for Intel Arria 10 and Intel Cyclone 10 GX Transceiver High-Speed Link Tuning

Document Version	Changes
2018.09.26	Initial release.