AN 837: Design Guidelines for Intel FPGA HDMI
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1 Design Guidelines for Intel® FPGA HDMI

The design guidelines help you implement the Intel High-Definition Multimedia Interface (HDMI) IP cores using FPGA devices.

These guidelines facilitate board designs for the Intel® FPGA HDMI IP video interfaces.

Related Links
• Intel FPGA HDMI IP Core User Guide
• Schematic Diagram for HSMC HDMI Daughter Card Revision 8
• Schematic Diagram for FMC HDMI Daughter Card Revision 6
• AN 745: Design Guidelines for Intel FPGA DisplayPort Interface

1.1 Intel FPGA HDMI Design Guidelines

The Intel FPGA HDMI interface has Transition Minimized Differential Signaling (TMDS) data and clock channels. The interface also carries a Video Electronics Standards Association (VESA) Display Data Channel (DDC).

The TMDS channels carry video, audio, and auxiliary data. The DDC is based on I^2C protocol. The Intel FPGA HDMI IP core uses the DDC to read Extended Display Identification Data (EDID) and exchange configuration and status information between an HDMI source and sink.

1.2 Intel FPGA HDMI Board Design Tips

When you are designing your Intel FPGA HDMI system, consider the following board design tips.

• Use no more than two vias per trace and avoid via stubs
• Match the differential pair impedance to the impedance of the connector and cable assembly (100 ohm ±10%)
• Minimize inter-pair and intra-pair skew to meet the TMDS signal skew requirement
• Avoid routing a differential pair over a gap in the underneath plane
• Use standard high speed PCB design practices

1.3 Hot-Plug Detect (HPD)

The HPD signal depends on the incoming +5V Power signal, for example, the HPD pin may be asserted only when the +5V Power signal from the source is detected.
To interface with an FPGA, you need to translate the 5V HPD signal to the FPGA I/O voltage level (VCCIO), using a voltage level translator such as TI TXB0102, which does not have pull-up resistors integrated. An HDMI source needs to pull down the HPD signal so that it can reliably differentiate between a floating HPD signal and a high voltage level HPD signal.

An HDMI sink +5V Power signal must be translated to FPGA I/O voltage level (VCCIO). The signal must be weakly pulled down with a resistor (10K) to differentiate a floating +5V Power signal when not driven by an HDMI source. An HDMI source +5V Power signal has over-current protection of no more than 0.5A.

1.4 Intel FPGA HDMI Display Data Channel (DDC)

The Intel FPGA HDMI DDC is based on the I²C signals (SCL and SDA) and require pull-up resistors.

To interface with an Intel FPGA, you need to translate the 5V SCL and SDA signal level to the FPGA I/O voltage level (VCCIO) using a voltage level translator.
# Document Revision History for AN 837: Design Guidelines for Intel FPGA HDMI

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| January 2018 | 2018.01.22 | Initial release.  
\textit{Note:} This document contains Intel FPGA HDMI design guidelines that were removed from AN 745: Design Guidelines for DisplayPort and HDMI Interfaces and renamed AN 745: Design Guidelines for Intel FPGA DisplayPort Interface. |