AN 830: Intel FPGA Triple-Speed Ethernet and On-Board PHY Chip Reference Design
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1. Intel® FPGA Triple-Speed Ethernet and On-Board PHY Chip Reference Design for Intel® Stratix® 10 Devices

The Intel® FPGA Triple-Speed Ethernet and on-board PHY chip reference design demonstrates Ethernet operation between the Triple-Speed Ethernet Intel FPGA IP core and on-board Marvell 88E1111 PHY chip in Intel Stratix® 10 GX FPGA Development Board. In this reference design, the Triple-Speed Ethernet Intel FPGA IP is connected to the on-board PHY chip through Serial Gigabit Media Independent Interface (SGMII).

1.1. Features

- Single-channel Triple-Speed Ethernet Intel FPGA IP operating at data rate of 10/100/1000 Mbps.
- Implementation of the SGMII auto-negotiation feature in order to communicate with on-board PHY chip.
- Sequential random burst test is supported in the hardware test and users are allowed to configure the number of packets, payload-data pattern, packet length, source MAC address, and destination MAC address of each burst.
- Support for Ethernet packet transmission and reception through internal MAC loopback path or Avalon® streaming reverse loopback path.
- Support for packet monitoring on both TX and RX data paths.
- Support for packet statistics report on both MAC transmitter (TX) and MAC receiver (RX).
- Support for System Console user interface. Users can make use of this TCL-based interface to dynamically configure and monitor any registers in this reference design.

1.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the reference design in a Linux system:

- Intel Quartus® Prime Pro Edition software version 20.4
- For hardware testing:
  - Intel Stratix 10 GX L-Tile FPGA Development Board (1SG280LU2F50E2VG)
  - Micro USB cable
  - External Ethernet packet generator (for Avalon streaming reverse loopback test only)
  - Ethernet Cat5e cable (for Avalon streaming reverse loopback test only)
1.3. Functional Description

The reference design consists of various components. The following figure shows the design components and the top-level signals of the reference design.

Figure 1. Block Diagram

Legend:
M = Avalon Memory-Mapped Master Port
S = Avalon Memory-Mapped Slave Port
Scr = Avalon Streaming Source Port
Sink = Avalon Streaming Sink Port
### 1.3.1. Design Components

Table 1. Design Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
</table>
| **Triple-Speed Ethernet Intel FPGA IP** | • This IP provides an integrated Ethernet MAC, PCS, and PMA solution for Ethernet applications.  
• During data transmission, the Triple-Speed Ethernet Intel FPGA IP transmits Ethernet packets from Avalon streaming interface to a 1.25-Gbps serial LVDS I/O interface and the Ethernet packets receiving operation is done with the opposite way. |
| **Ethernet Packet Generator** | • This module is a Platform Designer custom component that generates Ethernet packets.  
• It consists of sub-components such as Ethernet packet generation block, CRC generator, Avalon memory-mapped registers, and shift register. |
| **Ethernet Packet Monitor** | • This module is a Platform Designer custom component that verifies the payload of all received packets and collects the statistics of each received packet such as number of bytes received.  
• It consists of sub-components such as CRC checker and Avalon memory-mapped registers. |
| **Error Adapter** | • This adapter is a Platform Designer custom component that used to connect mismatched Avalon streaming source and sink interface.  
• By using this adapter, data source and data sink with different bit width can be connected together. For RX-to-TX Avalon streaming reverse loopback in this reference design, ff tx err is a 1-bit error signal while rx err is a 6-bit error signal.  
• This adapter can match the error conditions that are handled by the Avalon streaming source and Avalon streaming sink. |
| **Avalon Streaming Multiplexer** | • This multiplexer is a Platform Designer custom component that accepts data on its two Avalon streaming sink interfaces and multiplexes the data for transmission on its Avalon streaming source interface.  
• One of the Avalon streaming sink interface is connected to the Avalon streaming source interface of Ethernet Packet Generator (For forward MAC loopback) and another Avalon streaming sink interface is connected to the Avalon streaming source interface of Error Adapter (for reverse loopback).  
• The packets on Avalon streaming source interface of this multiplexer will be transmitted to Triple-Speed Ethernet Intel FPGA IP. |
| **Avalon Streaming Splitter** | • This splitter is a Platform Designer custom component that accepts data from Triple-Speed Ethernet Intel FPGA IP through Avalon streaming sink interface and splits the data on its two Avalon streaming source interfaces.  
• One of its Avalon Streaming source interface is connected to the Avalon streaming sink interface of Ethernet Packet Monitor (for forward MAC loopback) and another Avalon streaming source interface is connected to the Avalon streaming sink interface of Error Adapter (for reverse loopback). |
| **JTAG to Avalon Master Bridge Intel FPGA IP** | This IP provides a connection between System Console and Platform Designer system through the physical interface. The System Console initiates Avalon memory-mapped transactions by sending encoded streams of bytes through bridge's physical interface. |
| **IOPLL Intel FPGA IP** | • This IP generates a 100 MHz PLL output clock (clk_100M).  
• This output clock is the clock source for Platform Designer system. All components in this reference design use this output clock. |
1.3.2. Clocking Scheme

Figure 2. Clocking Scheme
1.3.3. Reset Scheme

Figure 3. Reset Scheme

1.4. Hardware Testing

Related Information
Getting Started with the Design Store

1.4.1. Test Case—Internal MAC Loopback

To run the hardware test case, follow these steps:

1. Download the reference design from Design Store and restore the design using Intel Quartus Prime software.
2. Launch the Intel Quartus Prime software and open the project file (top.qpf).
3. Click Processing ➤ Start Compilation to compile the design.
4. After the design is compiled successfully, a programming file (top.sof) is generated and located in the <project_directory>/output_files directory.

*Note: Warning (21608) appears in the compilation report because this design uses I/Os on the 3V I/O bank, which requires you to ensure that the VCCR_GXB and VCCT_GXB rails on the corresponding tile are powered up to avoid any configuration issues. Refer to the Intel Stratix 10 Device Family Pin Connection Guidelines for more details about the power rails. The Intel Stratix 10 GX L-Tile FPGA Development Board powers up the VCCR_GXB and VCCT_GXB rails by default, hence you can safely ignore this warning.

5. Set up the Intel Stratix 10 GX L-Tile FPGA Development Board.
a. Connect the programming cable to the JTAG connection port (CN1).
b. Connect the power adapter to the power supply input (J27).

6. In the Intel Quartus Prime software, select **Tools ➤ Programmer** to launch the programmer.

7. Download the generated programming file (**top.sof**) to the development board using the **Programmer** application.

8. Reset the Ethernet design by either these methods:
   - Press the **USER_PB0** push button.
   - Toggle the In-System Source and Probes bit[0] from 0 to 1 and back to 0 based on **Figure 4** on page 8.
      a. In the Intel Quartus Prime software, on the **Tools** menu, click **In-System Sources and Probes Editor** to open the In-System Sources and Probes Editor.
      b. In the **JTAG Chain Configuration** pane, point to Hardware, and then select **Intel Stratix 10 GX L-Tile FPGA Development Board**, as shown in the Programmer application.
      c. From the **Device** list, select **Intel Stratix 10 Device**, as shown in the Programmer application.
      d. Click the plus sign (+) on the side of **source[0..0]** to expand the bits list.
      e. Toggle the bit **source[0]** from 0 to 1 and back to 0.

   **Note:** The design must be reset whenever you begin a new test. The reset must assert for at least 10 ms because the RESET_N pin of the Marvell PHY needs to be kept low for 10 ms, which is the minimum reset requirement of the Marvell PHY.

**Figure 4.** Reset Through In-System Sources and Probes Editor
9. Open the `config.tcl` script using text editor, which is located in the `<project_directory>/sc_tcl` directory. Ensure that you set the following parameters accordingly to achieve intended operating speed rate and mode. For more information, refer to Configuration Script on page 21.
   a. Selection of speed rate:
      i. For 10 Mbps, set `ETH_SPEED` to 0 and to `ENA_10` to 1.
      ii. For 10/100/1000 Mbps, set `ETH_SPEED` to 0 and `ENA_10` to 0.
      iii. For 1000 Mbps only, set `ETH_SPEED` to 1 and `ENA_10` to 0 or 1. However, Intel does not recommend this setting because it causes link failure if the PHY is running at 10/100 Mbps.
   b. Mode enablement for MAC loopback or PHY loopback:
      i. For MAC loopback, set `LOOP_ENA` to 1 and `PHY_LOOPBACK` to 1 or 0.
      ii. For PHY loopback, set `LOOP_ENA` to 0 and `PHY_LOOPBACK` to 1.

10. In the Intel Quartus Prime software, select Tools ➤ System Debugging Tools ➤ System Console to launch the system console.

11. In the System Console command shell, change the directory to `<project_directory>/sc_tcl`.

12. Run the following command in the System Console command shell to start TSE MAC, TSE PCS, and on-board PHY chip configurations:
   ```
   source config.tcl
   ```

13. Run the following command in System Console command shell to start generating and monitoring Ethernet packets:
   ```
   source eth_gen_start.tcl
   ```
   
   **Note:** Open the `eth_gen_start.tcl` script which located in `<project_directory>/sc_tcl` directory to set to desired configurations. For more information, refer to Configuration Script on page 21.

   The Ethernet Packet Monitor automatically starts after the Ethernet packet is generated. The System Console displays the number of packets with/without error received by the Ethernet Packet Monitor (refer to Figure 8 on page 13).

14. Run the following command to view the TSE MAC statistic counters:
   ```
   source tse_stat_read.tcl
   ```
Figure 5. Sample Output—MAC Configuration Summary

Starting TSE MAC Configuration System Console

Info: Opened JTAG Master Service

Info: Configure TSE MAC

TSE MAC Rev = 0x00001304
TSE MAC write Scratch = 0xaaaaaaaa
TSE MAC read Scratch = 0xaaaaaaaa
Command Config(Value) = 33
Command Config(Pre-write) = 0x00000030
Command Config(Post-write) = 0x00000033
MAC Address 0 = 0x22334450
MAC Address 1 = 0x0000ee11
Frame Length = 0x000005ee
Pause Quanta = 0x0000ffff
RX Section Empty = 0x00001ff0
RX Section Full = 0x00000100
TX Section Empty = 0x00001ff0
TX Section Full = 0x00000100
RX Almost Empty = 0x00000008
RX Almost Full = 0x00000008
TX Almost Empty = 0x00000008
TX Almost Full = 0x00000003
MDIO Address 0 = 0x00000000
MDIO Address 1 = 0x00000000
Register Status = 0x00000000
TX IPG Length = 0x000000c
TX Command Status = 0x00000000
RX Command Status = 0x00000000

Info: Closed JTAG Master Service
Figure 6. Sample Output—PCS Configuration Summary

Starting TSE PCS Configuration System Console

Info: Opened JTAG Master Service

Info: Configure TSE PCS

TSE PCS rev = 0x00001301
TSE PCS write scratch = 0x0000aaaa
TSE PCS read scratch = 0x0000aaaa
TSE PCS if_mode = 0x0000000b
TSE PCS control register = 0x00001140
Waiting Link Up.....
Link is established!
Partner Ability:

Copper link interface is up.
Copper operating in Full Duplex mode.
Copper operating Speed 1000Mbps

Info: Closed JTAG Master Service
Figure 7. Sample Output—On-Board PHY Chip Configuration Summary

Starting Marvell PHY Configuration System Console

Info: Opened JTAG Master Service

Info: Configure On Board Ethernet PHY Chip

Configure PHY.
Set PHY SPEED to 1000Mbps
Enable PHY Auto-Negotiation
Enable PHY In Full Duplex Mode
PHY read Control Register = 0x00001140
Advertise PHY 100BASE-TX & 10BASE-T Full Duplex
PHY read AN Advertisement Register = 0x00000141
Advertise PHY 100BASE-T Full Duplex
PHY read 100BASE-T Control Register = 0x00000000
Set PHY Synchronizing FIFO to maximum
Enable PHY MIIx crossover
Set PHY HWCFG_MODE for SGMII to Copper Without Clock
PHY read Extended PHY Specific Status Register = 0x00000484
PHY Link Up.
PHY Speed and Duplex Resolved.
PHY operating in Full Duplex mode.
PHY operating Speed 1000Mbps
PHY read Status Register = 0x00007969
PHY read Control Register = 0x00001140

Info: Closed JTAG Master Service
Figure 8. Sample Output—Ethernet Packet Generator and Ethernet Packet Monitor Statistics

Starting Ethernet Generator / Monitor System Console

Info: Opened JTAG Master Service

Use Ethernet Generator
Number of packets = 10000
Configuration setting:
- Length : Random
- Packets length : 1500
- Pattern : Random
Random seed 0 = 0x56789abc
Random seed 1 = 0x00001234
Source address 0 = 0x23456789
Source address 1 = 0x0000eeff
Destination address 0 = 0x23456789
Destination address 1 = 0x0000eeff
Start Ethernet Generator
Monitor receive done
Number of packets received OK = 10000
Number of packets received error = 0

Info: Closed JTAG Master Service
### Figure 9. Sample Output—TX and RX MAC Statistic Counters

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Read Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x8</td>
<td>aFramesTransmittedESK</td>
<td>0x00002710</td>
</tr>
<tr>
<td>0x0c</td>
<td>aFramesReceivedESK</td>
<td>0x00002710</td>
</tr>
<tr>
<td>0x70</td>
<td>aFrameCheckSequenceErrors</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x74</td>
<td>aAlignmentErrors</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x78</td>
<td>aOctetsTransmittedESK</td>
<td>0x0055f3b9</td>
</tr>
<tr>
<td>0x7c</td>
<td>aOctetsReceivedESK</td>
<td>0x0055f3b9</td>
</tr>
<tr>
<td>0x80</td>
<td>aEthRXSERMACCtrlFrames</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x84</td>
<td>aEthRXSERMACCtrlFrames</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x88</td>
<td>ifInErrors</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x90</td>
<td>ifInDiscardFmts</td>
<td>0x00002710</td>
</tr>
<tr>
<td>0x94</td>
<td>ifInMulticastFmts</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x98</td>
<td>ifInBroadcastFmts</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x9c</td>
<td>ifInBytes</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0xa0</td>
<td>ifInOctets</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0xa4</td>
<td>ifInMulticastFmts</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0xa8</td>
<td>ifInBroadcastFmts</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0xac</td>
<td>etherStatsDropEvents</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0xb0</td>
<td>etherStatsOctets</td>
<td>0x0061faa</td>
</tr>
<tr>
<td>0xb4</td>
<td>etherStatsFmts</td>
<td>0x00002710</td>
</tr>
<tr>
<td>0xb8</td>
<td>etherStatsUndersizeFmts</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0xbc</td>
<td>etherStats oversizedFmts</td>
<td>0x00000000</td>
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<tr>
<td>0xc0</td>
<td>etherStatsFramed4Octets</td>
<td>0x000001a8</td>
</tr>
<tr>
<td>0xc4</td>
<td>etherStatsFramed4Octets</td>
<td>0x00000271</td>
</tr>
<tr>
<td>0xcf</td>
<td>etherStatsFramed128Octets</td>
<td>0x00000532</td>
</tr>
<tr>
<td>0xd0</td>
<td>etherStatsFramed48Octets</td>
<td>0x00000942</td>
</tr>
<tr>
<td>0xd4</td>
<td>etherStatsFramed1024Octets</td>
<td>0x0000094f</td>
</tr>
<tr>
<td>0xd8</td>
<td>etherStatsFramed1536Octets</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0xe0</td>
<td>etherStats errors</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0xe0</td>
<td>etherStatsFragments</td>
<td>0x00000000</td>
</tr>
</tbody>
</table>

### Related Information
- Marvell 88E1111 PHY Configuration Steps
- Intel Stratix 10 GX FPGA Development Kit
- Intel Stratix 10 Device Family Pin Connection Guidelines
1.4.2. Test Case—Avalon Streaming Reverse Loopback

To run the hardware test case, follow these steps:

1. Download the reference design from Design Store and restore the design using Intel Quartus Prime software.

2. Launch the Intel Quartus Prime software and open the project file (top.qpf).

3. Click Processing ➤ Start Compilation to compile the design.

4. After the design is compiled successfully, a programming file (top.sof) is generated and located in the <project_directory>/output_files directory.

5. Set up the Intel Stratix 10 GX L-Tile FPGA Development Board.
   a. Connect the external packet generator to the RJ-45 port of the development board (J10) by using Ethernet Cat5e cable.
   b. Connect the programming cable to the JTAG connection port (CN1).
   c. Connect the power adapter to the power supply input (J27).

6. In the Intel Quartus Prime software, select Tools ➤ Programmer to launch the programmer.

7. Download the generated programming file (top.sof) to the development board using the Programmer application.

8. Reset the Ethernet design by either these methods:
   - Press the USER_PB0 push button.
   - Toggle the In-System Source and Probes bit[0] from 0 to 1 and back to 0.
   
   Note: The design must be reset whenever you begin a new test. The RESET_N pin of the Marvell PHY needs to be kept low for 10 ms because the minimum reset requirement of the Marvell PHY is 10 ms.

9. Open the config.tcl script using text editor, which is located in the <project_directory>/sc_tcl directory. Ensure that you set the following parameters accordingly to achieve intended operating speed rate and mode. For more information, refer to Configuration Script on page 21.
   a. Ensure that you set ETH_SPEED to 0 and to ENA_10 to 0 so that the MAC is not forced to operate at 1000 Mbps only. This allows the MAC to follow the speed rate of the PHY set in step 9.c on page 15.
   b. If you want to operate the MAC in 1000 Mbps only, set ETH_SPEED to 1. However, Intel does not recommend this setting because it causes link failure if the PHY is running at 10/100 Mbps only.
   c. Selection of speed rate:
      i. For 10 Mbps only, set PHY_ETH_SPEED to 10.
      ii. For 10/100 Mbps only, set PHY_ETH_SPEED to 100.
      iii. For 10/100/1000 Mbps, set PHY_ETH_SPEED to 1000.
   d. Ensure that you set the LOOP_ENA and PHY_LOOPBACK parameters to 0 so that the MAC/PHY loopback mode or PHY loopback mode is disabled.

10. In the Intel Quartus Prime software, select Tools ➤ System Debugging Tools ➤ System Console to launch the System Console.
11. In the System Console command shell, change the directory to 
<project_directory>/sc_tcl.

12. Run the following command in the System Console command shell to start TSE 
MAC, TSE PCS, and on-board PHY chip configurations:

```bash
source config.tcl
```

The System Console displays the copper link connection status and the resolved 
operating speed and duplex mode of on-board PHY Chip (refer to Figure 12 on 
page 19).

13. Start to transmit the Ethernet packets from the external packet generator to the 
development board. Verify the number of packets that successfully loop back to 
the external packet generator.

14. Run the following command to view the TSE MAC statistic counters:

```bash
source tse_stat_read.tcl
```
Figure 10. Sample Output—MAC Configuration Summary

Starting TSE MAC Configuration System Console

Info: Opened JTAG Master Service

Info: Configure TSE MAC

TSE MAC Rev = 0x00001304
TSE MAC write Scratch = 0xaaaaaaaa
TSE MAC read Scratch = 0xaaaaaaaa
Command Config(Value) = 33
Command Config(Pre-write) = 0x00000030
Command Config(Post-write) = 0x00000033
MAC Address 0 = 0x22334450
MAC Address 1 = 0x0000ee11
Frame Length = 0x000005ee
Pause Quanta = 0x0000ffff
RX Section Empty = 0x00000fff
RX Section Full = 0x00000010
TX Section Empty = 0x00001fff
TX Section Full = 0x00000010
RX Almost Empty = 0x00000008
RX Almost Full = 0x00000008
TX Almost Empty = 0x00000008
TX Almost Full = 0x00000003
MDIO Address 0 = 0x00000000
MDIO Address 1 = 0x00000000
Register Status = 0x00000000
TX IEG Length = 0x00000000
TX Command Status = 0x00000000
RX Command Status = 0x00000000

Info: Closed JTAG Master Service
Sample Output—PCS Configuration Summary

Starting TSE PCS Configuration System Console

Info: Opened JTAG Master Service

Info: Configure TSE PCS

TSE PCS rev = 0x00001301
TSE PCS write scratch = 0x0000aaaa
TSE PCS read scratch = 0x0000aaaa
TSE PCS if_mode = 0x00000000b
TSE PCS control register = 0x00001140
Waiting Link Up.....
Link is established!
Partner Ability:

Copper link interface is up.
Copper operating in Full Duplex mode.
Copper operating Speed 1000Mbps

Info: Closed JTAG Master Service
Figure 12. Sample Output—On-Board PHY Chip Configurations

Starting Marvell PHY Configuration System Console

Info: Opened JTAG Master Service

Info: Configure On Board Ethernet PHY Chip

Configure PHY.
Set PHY SPEED to 1000Mbps
Enable PHY Auto-Negotiation
Enable PHY In Full Duplex Mode
PHY read Control Register = 0x00001140
PHY read AN Advertisement Register = 0x00000001
Advertise PHY 1000BASE-T Full Duplex
PHY read 1000BASE-T Control Register = 0x000000e0
Set PHY Synchronizing FIFO to maximum
Set PHY HECPS_NODE for SSMII to Copper Without Clock
PHY read Extended PHY Specific Status Register = 0x00008484
PHY Link Up.
PHY Speed and Duplex Resolved.
PHY operating in Full Duplex mode.
PHY operating Speed 1000Mbps
PHY read Status Register = 0x00007869
PHY read Control Register = 0x00001140

Info: Closed JTAG Master Service
Figure 13. Sample Output—TX and RX MAC Statistic Counters

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Read Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>aFramesTransmittedOK</td>
<td>0x01e0400</td>
</tr>
<tr>
<td>0x00</td>
<td>aFramesReceivedOK</td>
<td>0x01e0400</td>
</tr>
<tr>
<td>0x70</td>
<td>aFramesCRCERR</td>
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<td>0x74</td>
<td>alignmentErrors</td>
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<tr>
<td>0x94</td>
<td>etherStatusOverloadPackets</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x94</td>
<td>etherStatusLoopbackPackets</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x94</td>
<td>etherStatusMulticastPackets</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x94</td>
<td>etherStatusUnknownPackets</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x94</td>
<td>etherStatusAdminErrors</td>
<td>0x00000000</td>
</tr>
<tr>
<td>0x94</td>
<td>etherStatusConfigErrors</td>
<td>0x00000000</td>
</tr>
</tbody>
</table>

Info: Closed JLINK Master Service

Related Information

- **Marvell 88E1111 PHY Configuration Steps**
- **Intel Stratix 10 GX FPGA Development Kit**
1.5. TCL Script

You can use any text editor to edit the TCL scripts, which is located in
<project_directory>/sc_tcl. However, Intel recommends that you do not modify the
following TCL scripts:

• tse_mac_config.tcl
• tse_marvel_phy.tcl
• eth_gen_mon.tcl
• tse_stat_read.tcl

1.5.1. Configuration Script

The configuration script, config.tcl contains the settings and parameters that
configure the Triple-Speed Ethernet MAC, Triple-Speed Ethernet PCS and Marvell PHY
registers in this reference design.

• Triple-Speed Ethernet MAC configurations can be changed by configuring the MAC
  registers. For more information about Triple-Speed Ethernet MAC configuration
  register space, refer to Triple-Speed Ethernet Intel FPGA IP User Guide.

• Triple-Speed Ethernet PCS configurations can be changed by configuring the PCS
  registers. For more information about Triple-Speed Ethernet PCS configuration
  register space, refer to Triple-Speed Ethernet Intel FPGA IP User Guide.

• Marvell PHY configurations can be changed by configuring the on-board PHY chip
  register.

Related Information

Triple-Speed Ethernet Intel FPGA IP User Guide

1.5.2. Ethernet Packet Generator Script

The Ethernet Packet Generator script, eth_gen_start.tcl contains the parameters
and settings to configure the Ethernet Packet Generator registers in this reference
design.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>number_packet</td>
<td>Sets the total number of packets to be generated by the packet generator.</td>
</tr>
<tr>
<td>eth_gen</td>
<td>Enables or disables the packet generator.</td>
</tr>
<tr>
<td>length_sel</td>
<td>Selects fixed or random packet length.</td>
</tr>
<tr>
<td>pkt_length</td>
<td>Sets the fixed packet length. The packet length can be a value between 24 to 9600 bytes.</td>
</tr>
<tr>
<td>pattern_sel</td>
<td>Selects the data pattern for the random packet length.</td>
</tr>
<tr>
<td>rand_seed</td>
<td>Sets the initial random seed for the PRBS generator. This parameter is only valid when you select random packet length.</td>
</tr>
<tr>
<td>source_addr</td>
<td>Sets the source MAC address.</td>
</tr>
<tr>
<td>destination_addr</td>
<td>Sets the destination MAC address.</td>
</tr>
</tbody>
</table>
1.6. Interface Signals

Table 3. **Clock and Reset Signals**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk_clk</td>
<td>Input</td>
<td>1</td>
<td>This is the reference design clock, which derived from the IOPLL Intel FPGA IP.</td>
</tr>
<tr>
<td>reset_reset</td>
<td>Input</td>
<td>1</td>
<td>A single reset signal that used to reset all logic in the reference design. This reset signal is connected to a push button (USER_PB0).</td>
</tr>
<tr>
<td>triple_speed_ethernet_0_pcs_ref_clk_clock_connection_clk</td>
<td>Input</td>
<td>1</td>
<td>The 125 MHz reference clock for the 1.25 Gbps serial LVDS I/O interface. This clock is sourced from a dedicated reference clock source, which is in the same IO bank as triple_speed_ethernet_0_serial_connection_txp_0 and triple_speed_ethernet_0_serial_connection_rxp_0 pins.</td>
</tr>
</tbody>
</table>

Table 4. **1.25 Gbps Serial Interface Signals**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>triple_speed_ethernet_0_serial_connection_txp_0</td>
<td>Output</td>
<td>1</td>
<td>SGMII serial differential transmit interface. Connect this interface to the on-board PHY chip.</td>
</tr>
<tr>
<td>triple_speed_ethernet_0_serial_connection_rxp_0</td>
<td>Input</td>
<td>1</td>
<td>SGMII serial differential receive interface. Connect this interface to the on-board PHY chip.</td>
</tr>
</tbody>
</table>

Related Information

Triple-Speed Ethernet Intel FPGA IP User Guide

1.7. Configuration Registers and Status Registers

Table 5. **System Register Map**

<table>
<thead>
<tr>
<th>Base Address</th>
<th>Block</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000</td>
<td>Triple-Speed Ethernet Intel FPGA IP</td>
</tr>
<tr>
<td>0x00000400</td>
<td>Avalon Streaming Multiplexer</td>
</tr>
<tr>
<td>0x00000800</td>
<td>Ethernet Packet Monitor</td>
</tr>
<tr>
<td>0x00000c00</td>
<td>Ethernet Packet Generator</td>
</tr>
</tbody>
</table>
### Table 6. Ethernet Packet Generator Configuration Registers Map

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Name</th>
<th>Width</th>
<th>R/W</th>
<th>HW Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>number_packet</td>
<td>32</td>
<td>RW</td>
<td>0x00</td>
<td>Used to specify the number of packets to be generated.</td>
</tr>
</tbody>
</table>
| 0x04        | config_register  | 32    | RW  | 0x00           | • Bit 0 — 0: Fixed packet length — 1: Random packet length  
• Bits [14:1]—Specifies the fixed packet length and the valid values are between 24 to 9600 bytes. It is applicable only when you set bit 0 to 0.  
• Bit 15—Specifies the data pattern for random packet length. Set this bit to 0 for incremental data pattern. For random data pattern, set this bit to 1.  
• Bits [31:16]—Reserved.                                                                                                              |
| 0x08        | rand_seed0       | 32    | RW  | 0x00           | • The lower 32 bits of the random seed.  
• Occupies bits 31:0 of the PBRS generator when you set the data pattern to random (bit 15 of the configuration register).                                                                                               |
| 0x0c        | rand_seed1       | 32    | RW  | 0x00           | • The upper 32 bits of the random seed.  
• Occupies bits 63:32 of the PBRS generator when you set the data pattern to random (bit 15 of the configuration register).                                                                                               |

*continued...*
<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Name</th>
<th>Width</th>
<th>R/W</th>
<th>HW Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x10</td>
<td>source_addr0</td>
<td>32</td>
<td>RW</td>
<td>0x00</td>
<td>• Used to specify 6-bytes source/destination MAC address.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• source_addr0/destination_addr0 = last four bytes of the address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Bits [15:0] of source_addr1/destination_addr1 = first two bytes of the address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Bits [31:16] of source_addr1/destination_addr1 = unused</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• For example, if the source MAC address is 00-1C-23-17-4A-CB, you</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>get the following assignments:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>— source_addr0 = 0x17231C00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>— source_addr1 = 0x0000CB4A</td>
</tr>
<tr>
<td>0x14</td>
<td>source_addr1</td>
<td>32</td>
<td>RW</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0x18</td>
<td>destination_addr0</td>
<td>32</td>
<td>RW</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0x1C</td>
<td>destination_addr1</td>
<td>32</td>
<td>RW</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0x20</td>
<td>operation</td>
<td>32</td>
<td>RW/RO</td>
<td>0x00</td>
<td>• Bit 0—Set this bit to 1 to trigger packet generation. This bit clears</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>after the packet generation is started.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Bit 1—Set this bit to 1 to stop the packets generation. The generator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>will complete its current packet transmission 1st before terminates the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>packet generation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Bit 2—A value of 1 indicates that the packet generator completes generating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the total number of packets specified in the number_packet register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit clears each time packet generation triggers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Bit [31:3]—Reserved.</td>
</tr>
<tr>
<td>0x24</td>
<td>packet_tx_count</td>
<td>32</td>
<td>RO</td>
<td>0x00</td>
<td>This register will keep track the number of packets that the generator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>transmitted successfully. This register will clear if the packet generation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>is triggered.</td>
</tr>
</tbody>
</table>
### Table 7. Ethernet Packet Monitor Configuration Registers Map

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Name</th>
<th>Width</th>
<th>R/W</th>
<th>HW Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>number_packet</td>
<td>32</td>
<td>RO</td>
<td>0x00</td>
<td>Total number of packets that the monitor expects to receive.</td>
</tr>
<tr>
<td>0x04</td>
<td>packet_rx_ok</td>
<td>32</td>
<td>RO</td>
<td>0x00</td>
<td>Total number of received good packets.</td>
</tr>
<tr>
<td>0x08</td>
<td>packet_rx_error</td>
<td>32</td>
<td>RO</td>
<td>0x00</td>
<td>Total number of received packets with errors.</td>
</tr>
<tr>
<td>0x0C</td>
<td>byte_rx_count[31:0]</td>
<td>32</td>
<td>RO</td>
<td>0x00</td>
<td>• 64-bit counter that keeps track of the total number of bytes received.</td>
</tr>
<tr>
<td>0x10</td>
<td>byte_rx_count[63:32]</td>
<td>32</td>
<td>RO</td>
<td>0x00</td>
<td>• byte_rx_count[31:0] represents the lower 32 bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• byte_rx_count[63:32] represents the upper 32 bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Read byte_rx_count[31:0] followed by byte_rx_count[63:32] in the subsequent cycle to get an accurate count.</td>
</tr>
<tr>
<td>0x14</td>
<td>cycle_rx_count[31:0]</td>
<td>32</td>
<td>RO</td>
<td>0x00</td>
<td>• 64-bit counter that keeps track of the total number of cycles the monitor takes to receive all packets.</td>
</tr>
<tr>
<td>0x18</td>
<td>cycle_rx_count[63:32]</td>
<td>32</td>
<td>RO</td>
<td>0x00</td>
<td>• cycle_rx_count[31:0] represents the lower 32 bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• cycle_rx_count[63:32] represents the upper 32 bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Read cycle_rx_count[31:0] followed by cycle_rx_count[63:32] in the subsequent cycle to get an accurate count.</td>
</tr>
<tr>
<td>0x1C</td>
<td>rx_control_status</td>
<td>32</td>
<td>RW/RO</td>
<td>0x00</td>
<td>• Bit 0—Set this bit to 1 to trigger packets reception. This bit clears after packet reception is started.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Bit 1—Set this bit to 1 to stop packet reception. This bit clears when packet reception starts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Bit 2—A value of 1 indicates that the packet monitor has received the total number of packets specified in the number_packet register.</td>
</tr>
</tbody>
</table>

*continued...*
### 1.8. Regenerating Triple-Speed Ethernet Intel FPGA IP

The on-chip termination of the LVDS SERDES Intel FPGA IP reference clock within the Triple-Speed Ethernet Intel FPGA IP is turned on by default. The reference clock is pinned out to REF_CLK port in this reference design. Because an external termination resistor is present on the Intel Stratix 10 GX FPGA Development Kit at the REF_CLK port, the generated QIP file of the Triple-Speed Ethernet Intel FPGA IP is modified to turn off the on-chip termination. When upgrading the reference design to a newer Intel Quartus Prime software version or modification is made to the Triple-Speed Ethernet Intel FPGA IP, the QIP file is regenerated as part of the IP regeneration process. To turn off the on-chip termination, follow these steps to modify the QIP file after the IP regeneration:

1. Locate the QIP file of the Triple-Speed Ethernet Intel FPGA IP at
   `<project_directory>/platform/ip/qsys_top/qsys_top_eth_tse_0/qsys_top_eth_tse_0.qip`

2. Search the INPUT TERMINATION keyword for the LVDS SERDES Intel FPGA IP reference clock:
   ```
   set_instance_assignment -entity "qsys_top_eth_tse_0.altera_lvds_core14_191_ofc4bti" -library altera_lvds_core14_191 -name INPUT TERMINATION DIFFERENTIAL -to inclock
   ```

3. Comment out or remove this assignment.

4. Compile the reference design.

Failure to follow these steps will result in a critical warning:

```
Critical Warning(16643): Found INPUT TERMINATION assignments found for "REF_CLK" pin with multiple values. Using value: "OFF"
```

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>December 2017</td>
<td>2017.12.15</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2021.05.19       | • Updated the steps in the following topics:  
|                  |   — Test Case—Internal MAC Loopback  
|                  |   — Test Case—Avalon Streaming Reverse Loopback  
|                  | • Updated the software requirement in Hardware and Software Requirements.  
|                  | • Made editorial edits throughout the document. |
| 2020.10.14       | • Updated Table: Ethernet Packet Generator Configuration Registers Map to remove rand_seed2.  
|                  | • Updated Table: Ethernet Packet Monitor Configuration Registers Map to update the names and descriptions for the following registers:  
|                  |   — byte_rx_count  
|                  |   — cycle_rx_count  
|                  | • Made minor editorial edits throughout the document. |
| 2019.10.18       | • Updated the development kit name from Intel Stratix 10 GX Signal Integrity (SI) development kit to Intel Stratix 10 GX FPGA development kit.  
|                  | • Added a new topic—Regenerating Triple-Speed Ethernet Intel FPGA IP.  
|                  | • Updated the Intel FPGA Triple-Speed Ethernet and On-Board PHY Chip Reference Design for Intel Stratix 10 Devices topic.  
|                  | • Updated the Hardware and Software Requirements topic.  
|                  | • Updated the Test Case—Internal MAC Loopback topic:  
|                  |   — Updated the steps to run the hardware test case.  
|                  |   — Updated Figures:  
|                  |     • Sample Output—MAC Configuration Summary  
|                  |     • Sample Output—PCS Configuration Summary  
|                  |     • Sample Output—On-Board PHY Chip Configuration Summary  
|                  | • Updated the Test Case—Avalon-ST Reverse Loopback topic:  
|                  |   — Updated the steps to run the hardware test case.  
|                  |   — Updated Figures:  
|                  |     • Sample Output—MAC Configuration Summary  
|                  |     • Sample Output—PCS Configuration Summary  
|                  |     • Sample Output—On-Board PHY Chip Configuration Summary  
|                  |     • Sample Output—TX and RX MAC Statistic Counters  
|                  | • Updated Table: Design Components to update the descriptions for the following components:  
|                  |   — Triple-Speed Ethernet IP core  
|                  |   — I/O Phase-Locked Loop (PLL) core  
|                  | • Updated Figures:  
|                  |   — Block Diagram  
|                  |   — Clocking Scheme  
|                  |   — Reset Scheme  
|                  | • Removed Figure: Configuration of US OUT8 Frequency in Clock Controller.  
|                  | • Updated for latest Intel branding standards. |
| 2019.04.18       | • Updated Figure: Block Diagram.  
|                  | • Updated for latest Intel branding standards. |