AN 823: Intel FPGA JESD204B IP Core and ADI AD9625 Hardware Checkout Report for Intel Stratix 10 Devices
1 Intel FPGA JESD204B IP Core and ADI AD9625 Hardware Checkout Report for Intel® Stratix® 10 Devices

1.1 Hardware Requirements ........................................................................................................ 3
1.2 Hardware Setup .................................................................................................................. 3
1.3 Hardware Checkout Methodology ....................................................................................... 5
   1.3.1 Receiver Data Link Layer ..................................................................................... 5
   1.3.2 Receiver Transport Layer ............................................................................... 7
   1.3.3 Descrambling .............................................................................................. 8
   1.3.4 Deterministic Latency (Subclass 1) .............................................................. 9
1.4 JESD204B IP Core and ADC Configurations .................................................................... 10
1.5 Test Results ................................................................................................................... 10
1.6 Test Result Comments .................................................................................................... 11
1.7 Document Revision History for AN 823: Intel FPGA JESD204B IP Core and ADI AD9625 Hardware Checkout Report for Intel Stratix 10 Devices .................................................... 14
1.8 Appendix ....................................................................................................................... 14
1 Intel FPGA JESD204B IP Core and ADI AD9625 Hardware Checkout Report for Intel® Stratix® 10 Devices

The Intel FPGA JESD204B IP core is a high-speed point-to-point serial interface intellectual property (IP).

The JESD204B IP core has been hardware-tested with a number of selected JESD204B-compliant ADC (analog-to-digital converter) and DAC (digital-to-analog converter) devices.

This report highlights the interoperability of the JESD204B IP core with the AD9625 converter evaluation module (EVM) from Analog Devices Inc. (ADI). The following sections describe the hardware checkout methodology and test results.

Related Links
JESD204B IP Core User Guide

1.1 Hardware Requirements

The hardware checkout test requires the following hardware and software tools:
- Intel® Stratix® 10 GX L-Tile FPGA Development Kit (ES Edition) (1SG280LU3F50E3VGS1)
- ADI AD9625 EVM
- Mini-USB cable

Related Links
Intel Stratix 10 GX FPGA Development Kit

1.2 Hardware Setup

An Intel Stratix 10 GX L-Tile FPGA Development Kit (ES Edition) is used with the ADI AD9625 daughter card module installed to the development board’s FMC connector.

- The AD9625 EVM derives power from FMC pins.
- An internal on-board oscillator present on the AD9625 EVM provides 2.5 GHz device clock to the ADC.
- The AD9625 provides a divide by 4 version of this clock (625 MHz) to FPGA through FMC pins.
- For subclass 1, the FPGA generates SYSREF for the JESD204B IP core as well as the AD9625 device.
- The SYSREF is provided to the ADC through FMC pins.
The following system-level diagram shows how the different modules connect in this design.

In this setup, where $LMF = 811$, the data rate of transceiver lanes is 6.25 Gbps. The oscillator on the EVM is used for clocking both the EVM and the FPGA. The oscillator generates a fixed clock of frequency 2500 MHz. This clock is used as sampling.
frequency by the ADC. A divide by 4 version of this clock (625 MHz) is made available to FPGA through FMC pins. FPGA uses this clock as the reference clock for transceiver and generate internal link and frame clocks. The ADC registers are programmed through 3-wire SPI interface. Although the maximum lane rate supported by the JESD converter is 6.5 Gbps, the fixed oscillator on the EVM restricts the lane rate to 6.25 Gbps. The converter operates in a single JESD link in all configurations with a maximum of 8 lanes.

1.3 Hardware Checkout Methodology

The following section describes the test objectives, procedure, and the passing criteria. The test covers the following areas:

- Receiver data link layer
- Receiver transport layer
- Descrambling
- Deterministic latency (Subclass 1)

1.3.1 Receiver Data Link Layer

This test area covers the test cases for code group synchronization (CGS) and initial frame and lane synchronization (ILA).

On link start up, the receiver issues a synchronization request and the transmitter transmits /K/ (K28.5) characters. The Signal Tap Logic Analyzer tool monitors the receiver data link layer operation.

1.3.1.1 Code Group Synchronization (CGS)

Table 1. CGS Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| CGS.1     | Check whether sync request is deasserted after correct reception of four successive /K/ characters. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:
  - `jesd204_rx_pcs_data[(L*32)-1:0]`
  - `jesd204_rx_pcs_data_valid[L-1:0]`
  - `jesd204_rx_pcs_kchar_data[(L*4)-1:0]` (1) |
  The following signals in `<ip_variant_name>.v` are tapped:
  - `rx_dev_sync_n`
  - `jesd204_rx_int`
  The rxlink_clk is used as the sampling clock for the Signal Tap. | /K/ character or K28.5 (0xBC) is observed at each octet of the jesd204_rx_pcs_data bus. |
  - The jesd204_rx_pcs_data_valid signal is asserted to indicate data from the PCS is valid. |
  - The jesd204_rx_pcs_kchar_data signal is asserted whenever control characters like /K/, /R/, /Q/, or /A/ characters are observed. |
  - The rx_dev_sync_n signal is deasserted after correct reception of at least four successive /K/ characters. |
  - The jesd204_rx_int signal is deasserted if there is no error. |

(1) L is the number of lanes.

continued...
Test Case | Objective | Description | Passing Criteria
--- | --- | --- | ---
Each lane is represented by 32-bit data bus in `jesd204_rx_pcs_data` signal. The 32-bit data bus for is divided into 4 octets.

CGS.2 | Check full CGS at the receiver after correct reception of another four 8B/10B characters. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped: • `jesd204_rx_pcs_errdetect[(L*4)-1:0]` • `jesd204_rx_pcs_disperr[(L*4)-1:0]` (1) The following signals in `<ip_variant_name>.v` are tapped: • `jesd204_rx_int` The rxlink_clk is used as the sampling clock for the Signal Tap. | The `jesd204_rx_pcs_errdetect`, `jesd204_rx_pcs_disperr`, and `jesd204_rx_int` signals should not be asserted during CGS phase.

### 1.3.1.2 Initial Frame and Lane Synchronization (ILA)

#### Table 2. Initial Frame and Lane Synchronization Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>ILA.1</td>
<td>Check whether the initial frame synchronization state machine enters FS_DATA state upon receiving non /K/ characters.</td>
<td>The following signals in <code>&lt;ip_variant_name&gt;_inst_phy.v</code> are tapped: • <code>jesd204_rx_pcs_data[(L*32)-1:0]</code> • <code>jesd204_rx_pcs_data_valid[L-1:0]</code> • <code>jesd204_rx_pcs_kchar_data[(L*4)-1:0]</code> (2) The following signals in <code>&lt;ip_variant_name&gt;.v</code> are tapped: • <code>rx_dev_sync_n</code> • <code>jesd204_rx_int</code> The rxlink_clk is used as the sampling clock for the Signal Tap. Each lane is represented by 32-bit data bus in <code>jesd204_rx_pcs_data</code>. The 32-bit data bus for is divided into 4 octets.</td>
<td>• /R/ character or K28.0 (0x1C) is observed after /K/ character at the <code>jesd204_rx_pcs_data</code> bus. • The <code>jesd204_rx_pcs_data_valid</code> signal must be asserted to indicate that data from the PCS is valid. • The <code>rx_dev_sync_n</code> and <code>jesd204_rx_int</code> signals are deasserted. • Each multiframe in ILAS phase ends with /A/ character or K28.3 (0x7C). • The <code>jesd204_rx_pcs_kchar_data</code> signal is asserted whenever control characters like /K/, /R/, /Q/, or /A/ characters are observed.</td>
</tr>
<tr>
<td>ILA.2</td>
<td>Check the JESD204B configuration parameters from ADC in second multiframe.</td>
<td>The following signals in <code>&lt;ip_variant_name&gt;_inst_phy.v</code> are tapped: • <code>jesd204_rx_pcs_data[(L*32)-1:0]</code> • <code>jesd204_rx_pcs_data_valid[L-1:0]</code> (2) The following signal in <code>&lt;ip_variant_name&gt;.v</code> is tapped: • <code>jesd204_rx_int</code> The rxlink_clk is used as the sampling clock for the Signal Tap.</td>
<td>• /R/ character is followed by /Q/ character or K28.4 (0x9C) at the beginning of second multiframe. • The <code>jesd204_rx_int</code> is deasserted if there is no error. • Octets 0-13 read from these registers match with the JESD204B parameters in each test setup.</td>
</tr>
</tbody>
</table>

---

(2) L is the number of lanes.
### 1.3.2 Receiver Transport Layer

To check the data integrity of the payload data stream through the JESD204B receiver IP Core and transport layer, the ADC is configured to output PRBS-23 and Ramp test data pattern. The ADC is also set to operate with the same configuration as set in the JESD204B IP Core. The PRBS checker/Ramp checker in the FPGA fabric checks data integrity for one minute.

This figure shows the conceptual test setup for data integrity checking.

**Figure 3. Data Integrity Check Using PRBS/Ramp Checker**

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| ILA.3 | Check the lane alignment | The following signals in <ip_variant_name>._inst_phy.v are tapped:  
- jesd204_rx_pcs_data[(L*32)-1:0]  
- jesd204_rx_pcs_data_valid[L-1:0]  
The following signals in <ip_variant_name>.v are tapped:  
- rx_somf[3:0]  
- dev_lane_aligned  
- jesd204_rx_int  
The rxlink_clk is used as the sampling clock for the Signal Tap. |  
- The dev_lane_aligned is asserted upon the last /A/ character of the ILAS is received, which is followed by the first data octet.  
- The rx_somf marks the start of multiframe in user data phase.  
- The jesd204_rx_int is deasserted if there is no error. |
### Table 3. Transport Layer Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| TL.1      | Check the transport layer mapping using Ramp test pattern. | The following signals in `altera_jesd204_transport_rx_to_p.sv` are tapped:  
  • `jesd204_rx_data_valid`  
  The following signals in `jesd204b_ed.sv` are tapped:  
  • `data_error`  
  • `jesd204_rx_int`  
The `rxframe_clk` is used as the sampling clock for the Signal Tap. The `data_error` signal indicates a pass or fail for the PRBS checker. |  
  • The `jesd204_rx_data_valid` signal is asserted.  
  • The `data_error` and `jesd204_rx_int` signals are deasserted. |
| TL.2      | Check the transport layer mapping using PRBS-23 test pattern. | The following signals in `altera_jesd204_transport_rx_to_p.sv` are tapped:  
  • `jesd204_rx_data_valid`  
  The following signals in `jesd204b_ed.sv` are tapped:  
  • `data_error`  
  • `jesd204_rx_int`  
The `rxframe_clk` is used as the sampling clock for the Signal Tap. The `data_error` signal indicates a pass or fail for the PRBS checker. |  
  • The `jesd204_rx_data_valid` signal is asserted.  
  • The `data_error` and `jesd204_rx_int` signals are deasserted. |

### 1.3.3 Descrambling

The PRBS/Ramp checker at the receiver transport layer checks the data integrity of descrambler. The Signal Tap Logic Analyzer tool monitors the operation of the receiver transport layer.

### Table 4. Descrambler Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| SCR.1     | Check the functionality of the descrambler using Ramp test pattern. | Enable scrambler at the ADC and descrambler at the JESD204B receiver IP Core. 
The signals that are tapped in this test case are similar to test case TL.1 |  
  • The `jesd204_rx_data_valid` signal is asserted.  
  • The `data_error` and `jesd204_rx_int` signals are deasserted. |
| SCR.2     | Check the functionality of the descrambler using PRBS-23 test pattern. | Enable scrambler at the ADC and descrambler at the JESD204B receiver IP Core. 
The signals that are tapped in this test case are similar to test case TL.2 |  
  • The `jesd204_rx_data_valid` signal is asserted.  
  • The `data_error` and `jesd204_rx_int` signals are deasserted. |
1.3.4 Deterministic Latency (Subclass 1)

The figure below shows the block diagram of deterministic latency test setup. A SYSREF generator in the FPGA provides a periodic SYSREF pulse for both the AD9625 and JESD204B IP Core. The SYSREF generator is running in the link clock domain and the period of SYSREF pulse is configured to the desired multiframe size. The SYSREF pulse restarts the LMF counter and realigns it to the LMFC boundary.

**Figure 4. Deterministic Latency Test Setup Block Diagram**

The deterministic latency measurement block checks deterministic latency by measuring the number of link clock counts between the start of de-assertion of SYNC~ to the first user data output.

**Figure 5. Deterministic Latency Measurement Timing Diagram**

With the setup above, four test cases were defined to prove deterministic latency. The JESD204B IP Core does continuous SYSREF detection. The SYSREF continuous mode is enabled on the AD9625 for this deterministic latency measurement.
Table 5. Deterministic Latency Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL.1</td>
<td>Check the FPGA SYSREF single detection.</td>
<td>Check that the FPGA detects the first rising edge of SYSREF pulse. Read the status of <code>sysref_singledet (bit[2])</code> identifier in <code>syncn_sysref_ctrl</code> register at address 0x54. Read the status of <code>csr_sysref_lmfc_err (bit[1])</code> identifier in the <code>rx_err0</code> register at address 0x60.</td>
<td>The value of <code>sysref_singledet</code> identifier should be zero. The value of <code>csr_sysref_lmfc_err</code> identifier should be zero.</td>
</tr>
<tr>
<td>DL.2</td>
<td>Check the SYSREF capture.</td>
<td>Check that FPGA and ADC capture SYSREF correctly and restart the LMF counter. Both FPGA and ADC are also repetitively reset. Read the value of <code>rbd_count (bit[10:3])</code> identifier in <code>rx_status0</code> register at address 0x80.</td>
<td>If the SYSREF is captured correctly and the LMF counter restarts, for every reset, the <code>rbd_count</code> value should only drift within 1-2 link clocks due to word alignment.</td>
</tr>
<tr>
<td>DL.3</td>
<td>Check the latency from start of SYNC~ deassertion to first user data output.</td>
<td>Check that the latency is fixed for every FPGA and ADC reset and power cycle. Record the number of link clocks count from the start of SYNC~ deassertion to the first user data output, which is the assertion of <code>jesd204_rx_link_valid</code> signal. The deterministic latency measurement block in Figure 4 on page 9 has a counter to measure the link clock count.</td>
<td>Consistent latency from the start of SYNC~ deassertion to the assertion of <code>jesd204_rx_link_valid</code> signal.</td>
</tr>
<tr>
<td>DL.4</td>
<td>Check the data latency during user data phase.</td>
<td>Check that the data latency is fixed during user data phase. Observe the ramp pattern from the Signal Tap Logic Analyzer.</td>
<td>The ramp pattern should be in perfect shape with no distortion.</td>
</tr>
</tbody>
</table>

1.4 JESD204B IP Core and ADC Configurations

The JESD204B IP Core parameters (L, M, and F) in this hardware checkout are natively supported by the AD9625 device's quick configuration register at address 0x05E. The transceiver data rate, sampling clock frequency, and other JESD204B parameters comply with the AD9625 operating conditions.

The hardware checkout testing implements the JESD204B IP Core with the following parameter configuration.
Global setting for all configuration:
- \(CS = 0\)
- \(CF = 0\)
- Subclass = 1
- FPGA Management Clock (MHz) = 100
- Character Replacement = Enabled
- PCS Option = Hard PCS

### Table 6. Parameter Configuration

<table>
<thead>
<tr>
<th>LMF</th>
<th>HD</th>
<th>S</th>
<th>N</th>
<th>N'</th>
<th>ADC Sampling Clock (MHz)</th>
<th>FPGA Device Clock (MHz)</th>
<th>FPGA Link Clock (MHz)</th>
<th>FPGA Frame Clock (MHz)</th>
<th>Lane Rate (Gbps)</th>
<th>DDC enabled</th>
<th>Data Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>118</td>
<td>0</td>
<td>4</td>
<td>16</td>
<td>16</td>
<td>2500</td>
<td>625</td>
<td>156.25</td>
<td>78.125</td>
<td>6.25</td>
<td>Yes</td>
<td>PRBS-23 Ramp</td>
</tr>
<tr>
<td>214</td>
<td>0</td>
<td>4</td>
<td>16</td>
<td>16</td>
<td>2500</td>
<td>625</td>
<td>156.25</td>
<td>156.25</td>
<td>6.25</td>
<td>Yes</td>
<td>PRBS-23 Ramp</td>
</tr>
<tr>
<td>412</td>
<td>0</td>
<td>4</td>
<td>16</td>
<td>16</td>
<td>2500</td>
<td>625</td>
<td>156.25</td>
<td>156.25</td>
<td>6.25</td>
<td>Yes</td>
<td>PRBS-23 Ramp</td>
</tr>
<tr>
<td>611</td>
<td>1</td>
<td>4</td>
<td>12</td>
<td>12</td>
<td>2500</td>
<td>625</td>
<td>156.25</td>
<td>156.25</td>
<td>6.25</td>
<td>No</td>
<td>PRBS-23 Ramp</td>
</tr>
<tr>
<td>811</td>
<td>1</td>
<td>4</td>
<td>12</td>
<td>16</td>
<td>2500</td>
<td>625</td>
<td>156.25</td>
<td>156.25</td>
<td>6.25</td>
<td>No</td>
<td>PRBS-23 Ramp</td>
</tr>
</tbody>
</table>

### 1.5 Test Results

The following table contains the possible results and their definition.

<table>
<thead>
<tr>
<th>Result</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>PASS</td>
<td>The Device Under Test (DUT) was observed to exhibit conformant behavior.</td>
</tr>
<tr>
<td>PASS with comments</td>
<td>The DUT was observed to exhibit conformant behavior. However, an additional</td>
</tr>
<tr>
<td></td>
<td>explanation of the situation is included, such as due to time limitations</td>
</tr>
<tr>
<td></td>
<td>only a portion of the testing was performed.</td>
</tr>
<tr>
<td>FAIL</td>
<td>The DUT was observed to exhibit non-conformant behavior.</td>
</tr>
<tr>
<td>Warning</td>
<td>The DUT was observed to exhibit behavior that is not recommended.</td>
</tr>
<tr>
<td>Refer to comments</td>
<td>From the observations, a valid pass or fail could not be determined. An</td>
</tr>
<tr>
<td></td>
<td>additional explanation of the situation is included.</td>
</tr>
</tbody>
</table>

The following table shows the results for test cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, TL.2, SCR.1, and SCR.2 with different values of \(L\), \(M\), \(F\), \(K\), subclass, data rate, sampling clock, link clock, and SYSREF frequencies.

---

(3) The device clock is used to clock the transceiver.

(4) The frame clock and link clock are derived from the device clock using an internal PLL.

(5) The 16-bit test pattern is an output from the JESD204 test pattern generator block in the AD9625.
Table 8. Results for Test Cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, TL.2, SCR.1, and SCR.2

<table>
<thead>
<tr>
<th>Test</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>SCR</th>
<th>K</th>
<th>Data rate (Gbps)</th>
<th>ADC Sampling Clock (MHz)</th>
<th>Link Clock (MHz)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td>0</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td>1</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td>0</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td>1</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>0</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>1</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>0</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>1</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>9</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>10</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>11</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>12</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>13</td>
<td>6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS with comments</td>
</tr>
<tr>
<td>14</td>
<td>6</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS with comments</td>
</tr>
<tr>
<td>15</td>
<td>6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>20</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS with comments</td>
</tr>
<tr>
<td>16</td>
<td>6</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>20</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS with comments</td>
</tr>
<tr>
<td>17</td>
<td>8</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>18</td>
<td>8</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>32</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>19</td>
<td>8</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>20</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
<tr>
<td>20</td>
<td>8</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>20</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
</tr>
</tbody>
</table>

The following table shows the results for test cases DL.1, DL.2, DL.3, and DL.4 with different values of L, M, F, K, subclass, data rate, sampling clock, link clock, and SYSREF frequencies.

Table 9. Results for Deterministic Latency Test

<table>
<thead>
<tr>
<th>Test</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>Subclass</th>
<th>K</th>
<th>Data rate (Gbps)</th>
<th>Sampling Clock (MHz)</th>
<th>Link Clock (MHz)</th>
<th>Result</th>
<th>Latency (Link Clock Cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL.1</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td>1/32</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
<td>195 (K=16) 323 (K=32)</td>
</tr>
<tr>
<td>DL.2</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td>1/32</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
<td></td>
</tr>
<tr>
<td>DL.3</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td>1/32</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
<td></td>
</tr>
<tr>
<td>DL.4</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td>1/32</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
<td></td>
</tr>
<tr>
<td>DL.1</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>1/32</td>
<td>16</td>
<td>6.25</td>
<td>2500</td>
<td>156.25</td>
<td>PASS</td>
<td>115 (K=16) 195 (K=32)</td>
</tr>
</tbody>
</table>

continued...
### Test Result Comments

In each test case, the JESD204B receiver IP core successfully initialize from CGS phase, ILA phase, and until user data phase.

No data integrity issue is observed by the PRBS and Ramp checker for all JESD configurations. In one of the JESD configuration modes (LMF=611), the result status is marked with 'Pass with comments' because data integrity tests were not performed.
The Intel FPGA transport layer doesn’t support configurations with \( N' = 12 \) and \( F = 1 \) which is the case with this configuration mode. However, all other test cases were found to be PASS.

In the deterministic latency measurement, consistent total latency is observed across multiple power cycles or resets.

For a few JESD configurations, to avoid lane de-skew error or achieve deterministic latency on FPGA, RBD offset register needs to be programmed. The modes and the corresponding values used are tabled below.

<table>
<thead>
<tr>
<th>Mode (LMF)</th>
<th>csr_rbd_offset (syncn_sysref_ctrl [10:3])</th>
</tr>
</thead>
<tbody>
<tr>
<td>611 K=32</td>
<td>4</td>
</tr>
</tbody>
</table>

Related Links
Programmable RBD Offset

1.7 Document Revision History for AN 823: Intel FPGA JESD204B IP Core and ADI AD9625 Hardware Checkout Report for Intel Stratix 10 Devices

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>December 2017</td>
<td>2017.12.18</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>

1.8 Appendix

Quartus Tool Version

Intel Quartus® Prime Pro Edition software version 17.0IR2 Build 116 (with patch version 0.02IR2) is used for compilation of designs.

Core PLL

Intel Stratix 10 fPLL is used as core PLL in the design to generate link and frame clocks from the reference clock received from converter.

SYSREF Detection

Continuous SYSREF detection mode is enabled on ADC. Without continuous sysref detection on ADC side few modes exhibit variable link latency. The modes that exhibit variable link latency are LMF = 118, 214, and 412. For uniformity, all the JESD configurations are enabled with continuous SYSREF generation.

DDC Enable Modes

Figure 7 on page 15 shows the JESD configurations supported by the ADC. The highlighted rows in the table are the configurations that are implemented in reference designs.
The criteria for selection of mode was the sampling rate of ADC. Note that the maximum sampling rate for all the selected JESD configurations in the table is 2500 MSPS. The AD9625 EVM has a fixed oscillator of 2500 MHz (also highlighted in Figure 2 on page 4). This oscillator generates the ADC sampling clock. As a result, the ADC sampling rate is always fixed to 2500 Msps.

This was the rationale behind selection of JESD modes. It is observed that modes with 1, 2, and 4 lanes have DDC enabled.

**JESD Lane Rate Selection**

As explained in previous section, the ADC sampling rate is fixed to 2500 Msps. This also restricts the flexibility to change JESD lane rates. In all the variants, the maximum JESD lane rate achievable is 6250 Mbps.