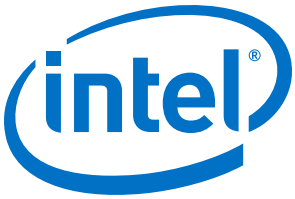

AN 808: Migration Guidelines from Arria 10 to Stratix 10 for 10G Ethernet Subsystem

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Contents

Migration Guidelines from Arria® 10 to Stratix® 10 for 10G Ethernet Subsystem

The Low Latency (LL) Ethernet 10G (10GbE) Media Access Controller (MAC) IP core includes Stratix® 10 and Arria® 10 design examples that are compliant with IEEE 802.3-2008 specification. The interfaces between Stratix 10 LL 10GbE MAC IP core and physical interface (PHY) IP core are different compared to Arria 10 LL 10GbE MAC IP core with PHY IP core.

These migration guidelines are meant for those are familiar with Arria 10 LL 10GbE MAC IP core. Use these migration guidelines if you want to migrate your Arria 10 LL 10GbE MAC design to use Stratix 10 devices.

Note: Stratix 10 devices are not supported in the 17.0 Quartus® Prime software. For more information, contact Intel.

Figure 1. Stratix 10 LL 10GbE MAC System

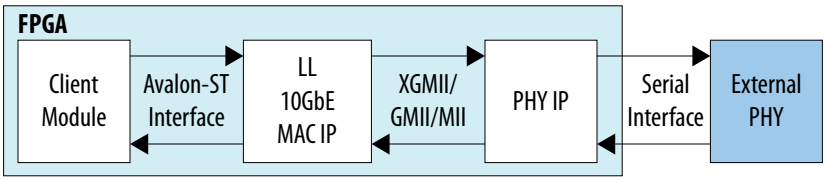


Table 1. Comparison between Stratix 10 and Arria 10 Design Examples for LL 10GbE MAC IP Core

Design Example	MAC Variant	PHY	Development Kit	Arria 10	Stratix 10
10GBase-R Ethernet	10G	Native PHY (Support L/H-tile Native PHY for Stratix 10)	Arria 10/Stratix 10 GX Transceiver Signal Integrity	Yes	Yes
1G/2.5G Ethernet with 1588	1G/2.5G	1G/2.5G/5G/10G Multi-rate Ethernet PHY	Arria 10/Stratix 10 GX Transceiver Signal Integrity	Yes	Yes
1G/2.5G/10G Ethernet	1G/2.5G/10G	1G/2.5G/5G/10G Multi-rate Ethernet PHY	Arria 10/Stratix 10 GX Transceiver Signal Integrity	Yes	Yes
10GBase-R Register Mode Ethernet	10G	Native PHY	Arria 10 GX Transceiver Signal Integrity	Yes	Not available
XAUI Ethernet	10G	XAUI PHY	Arria 10 GX FPGA	Yes	Not available
1G/10G Ethernet	1G/10G	1G/10GbE and 10GBASE-KR PHY	Arria 10 GX Transceiver Signal Integrity	Yes	Not available

continued...

Design Example	MAC Variant	PHY	Development Kit	Arria 10	Stratix 10
1G/10G Ethernet with 1588	1G/10G	1G/10GbE and 10GBASE-KR PHY	Arria 10 GX Transceiver Signal Integrity	Yes	Not available
10M/ 100M/1G/10G Ethernet	10M/ 100M/1G/10G	1G/10GbE and 10GBASE-KR PHY	Arria 10 GX Transceiver Signal Integrity	Yes	Not available
10M/ 100M/1G/10G Ethernet with 1588	10M/ 100M/1G/10G	1G/10GbE and 10GBASE-KR PHY	Arria 10 GX Transceiver Signal Integrity	Yes	Not available
1G/2.5G Ethernet	1G/2.5G	1G/2.5G/5G/10G Multi-rate Ethernet PHY	Arria 10 GX Transceiver Signal Integrity	Yes	Not available
10G USXGMII Ethernet	1G/2.5G/5G/10G (USXGMII)	1G/2.5G/5G/10G Multi-rate Ethernet PHY	Arria 10 GX Transceiver Signal Integrity	Yes	Not available

Note: You can access the listed design examples through the LL 10GbE MAC parameter editor in the Quartus Prime Pro Edition software.

Related Links

- Low Latency Ethernet 10G MAC User Guide
- Stratix 10 Low Latency Ethernet 10G MAC Design Example User Guide
- Stratix 10 L-Tile Transceiver PHY User Guide
- Stratix 10 H-Tile Transceiver PHY User Guide

Supported Configurations for Stratix 10 and Arria 10 LL 10GbE MAC Designs

The following table lists all the possible Stratix 10 and Arria 10 Ethernet IP configurations.

Table 2. Supported Configurations for Arria 10 and Stratix 10 Ethernet IP Configuration

IP Core		Arria 10	Stratix 10
LL 10GbE MAC	Speed	• 10G • 1G/10G • 10M/100M/1G/10G • 1G/2.5G • 1G/2.5G/10G • 1G/2.5G/5G/10G (USXGMII interface) • 10M/100M/1G/2.5G • 10M/100M/1G/2.5G/10G	
	IEEE 1588v2 feature	• 10G • 1G/10G • 10M/100M/1G/10G • 1G/2.5G	• 10G • 1G/10G • 10M/100M/1G/10G • 1G/2.5G • 1G/2.5G/10G

continued...

IP Core		Arria 10	Stratix 10
1G/2.5G/5G/10G Multi-rate Ethernet PHY	Speed	• 2.5G • 1G/2.5G • 1G/2.5G/10G (MGBASE-T PHY) • 1G/2.5G/5G/10G (USXGMII interface/NBASE-T PHY)	
	IEEE 1588v2 feature	• 2.5G • 1G/2.5G	• 2.5G • 1G/2.5G • 1G/2.5G/10G Not supported for enabled SGMII mode.
	SGMII Mode	Not available	• 1G/2.5G • 1G/2.5G/10G
XAUI PHY		Available	Not available
Stratix 10 L-tile/H-tile Transceiver Native PHY		Not available	Supported presets: • 10GBASE-R • 10GBASE-R 1588 • 10GBASE-R Low Latency • 10GBASE-R with KR FEC
Arria 10 Transceiver Native PHY		Supported presets: • 10GBASE-R • 10GBASE-R Register Mode • 10GBASE-R Low Latency • 10GBASE-R with KR FEC	Not available
Arria 10 1G/10GbE and 10GBASE-KR PHY		Available	Not available
Stratix 10 10GBASE-KR PHY		Not available	Available

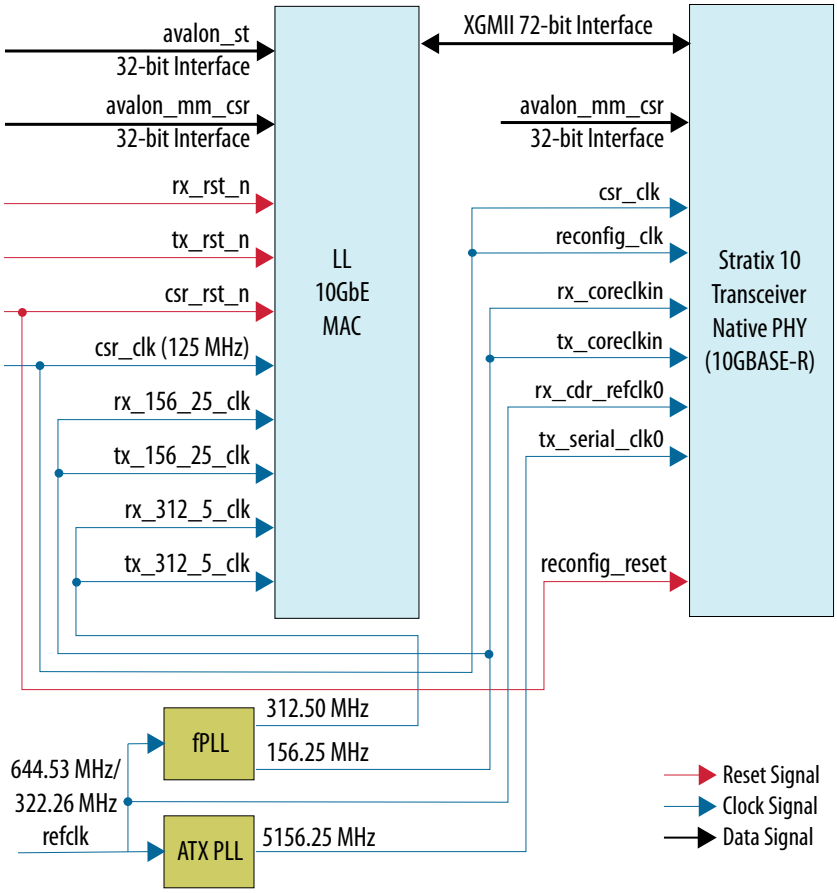
Clocking and Reset Infrastructure

Stratix 10 LL 10GbE MAC and Stratix 10 Transceiver Native PHY IP Cores

You can configure the Stratix 10 Transceiver Native PHY IP core to implement 10GBASE-R PHY with the Ethernet-specific physical layer running at 10.3125 Gbps data rate as defined in Clause 49 of IEEE 802.3-2008 specification. This configuration provides an XGMII to LL 10GbE MAC IP core and implements a single-channel 10.3125Gbps PHY for a direct connection to a small form factor pluggable plus (SFP+) optical module using the small form factor interface (SFI) electrical specification.

The following figure illustrates the migration from an Arria 10 design to a Stratix 10 design.

Figure 2. Clocking and Reset Scheme for LL 10GbE MAC and Stratix 10 Transceiver Native PHY in 10GBASE-R Design Example Interface



Related Links

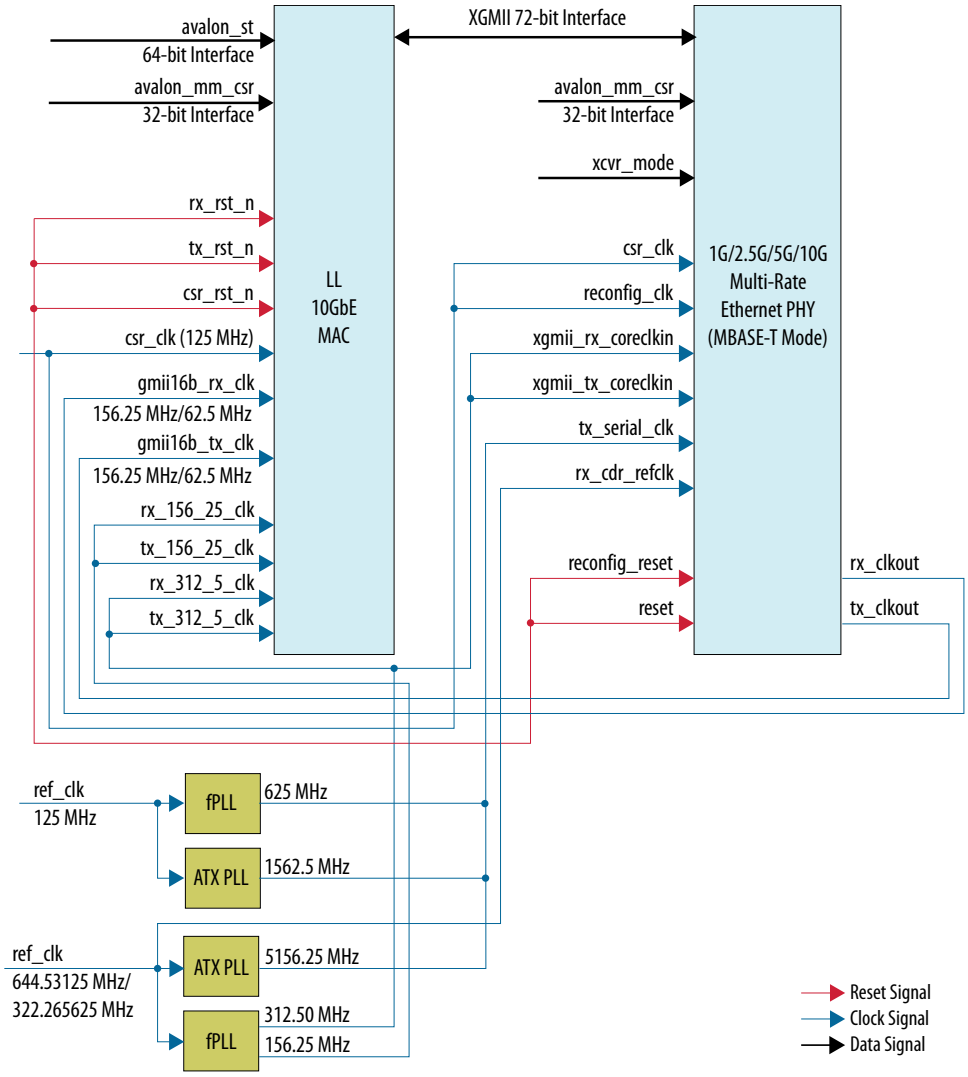
AN795: Implementing Guidelines for 10G Ethernet Subsystem Using Low Latency 10G MAC IP Core in Arria 10 Devices

Stratix 10 LL 10GbE MAC and Stratix 10 1G/2.5G/5G/10G Multi-Rate Ethernet PHY IP Cores

Stratix 10 1G/2.5G/5G/10G Multi-Rate Ethernet PHY IP core provides GMII and XGMII to the LL 10GbE MAC IP core. The Stratix 10 1G/2.5G/5G/10G Multi-Rate Ethernet PHY IP core implements a single channel 1G/2.5G/5G/10Gbps serial PHY. The design provides a direct connection to 1G/2.5GbE dual speed SFP+ pluggable modules, MGBASE-T copper external PHY devices, or chip-to-chip interfaces. These IP cores support reconfigurable data rates.

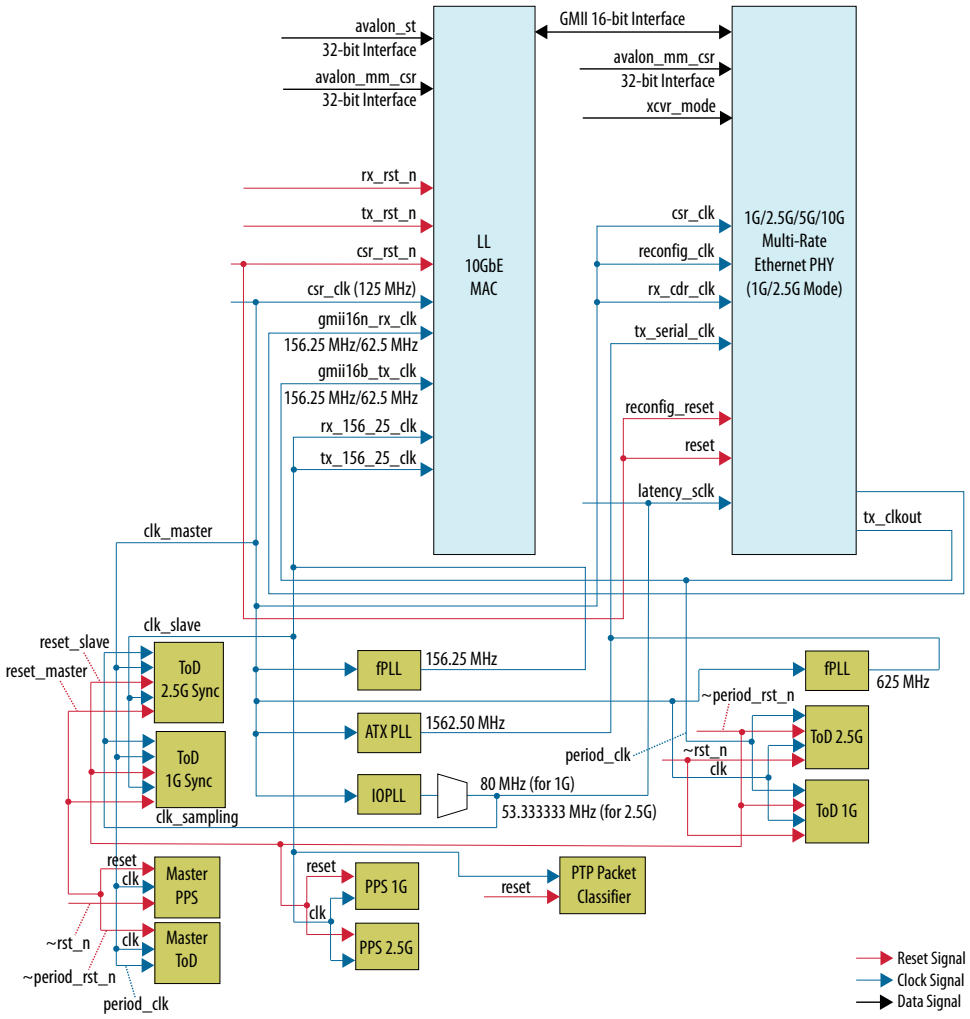
The following figure illustrates then migration from an Arria 10 design to a Stratix 10 design.

Figure 3. Clocking and Reset Scheme for Stratix 10 LL 10GbE MAC and Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY Design Example (1G/2.5G/10G Mode)



The following figure illustrates the latest clocking and reset scheme of the 1G/2.5G Ethernet with IEEE 1588v2 feature design example targeted on Stratix 10. There are differences between this solution and the version that was introduced in Arria 10. Modification is needed when migrating design from Arria 10 to Stratix 10.

Figure 4. Clocking and Reset Scheme for Stratix 10 LL 10GbE MAC and Stratix 10 1G/2.5G/5G/10G Multi-rate Ethernet PHY Design Example (1G/2.5G Mode with 1588)

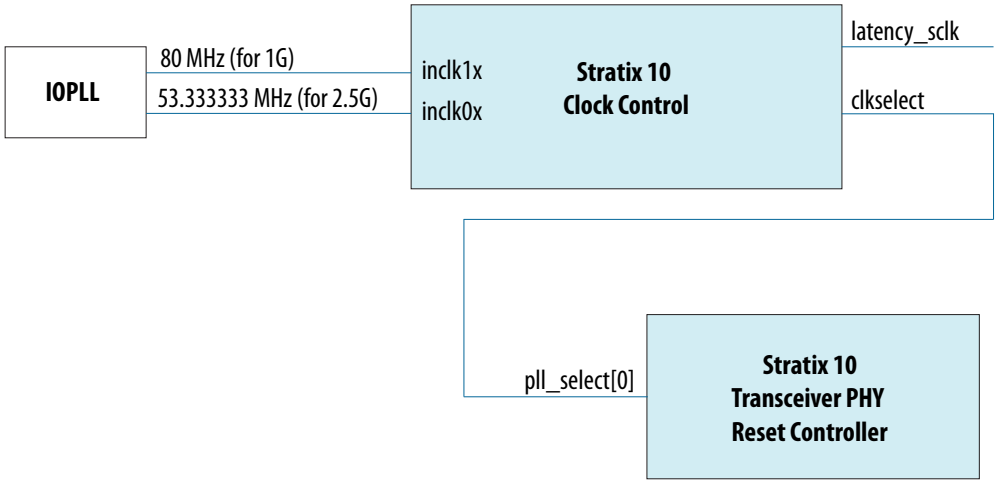


A new input clock port `latency_sclk` is available in Stratix 10. This port is available when you turn on the **Enable latency measurement ports** parameter in the Stratix 10 L/H-Tile Transceiver Native PHY IP core or the **Enable IEEE 1588 Precision Time Protocol** parameter in the 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP core. This port is required for deterministic latency measurement model for Stratix 10 devices. For more information, refer to the Deterministic Latency Use Model chapter in *Stratix 10 L/H-Tile Transceiver PHY User Guide*.

To connect an I/O phase-locked loop (IOPLL), add a Stratix 10 Clock Control (stratix10_clkctrl) IP from the IP Catalog. The IOPLL provides two sampling clocks in this design: 53.33 MHz for 2.5G mode and 80 MHz for 1G mode.

The following figure illustrates the connectivity details based on the 1G/2.5G Ethernet design.

Figure 5. Connectivity Diagram for Stratix 10 1G/2.5G Ethernet with 1588 Design



You must ensure that the `inclk0x` port connects to 2.5G sampling clock and the `inclk1x` port connects to 1G sampling clock. The output clock port of clock control becomes the `latency_sclk` port. For design migration from Arria 10 to Stratix 10, you can reuse the similar connectivity between the 1G/2.5G reconfiguration block and transceiver reset controller.

Related Links

- Stratix 10 L-Tile Transceiver PHY User Guide
- Stratix 10 H-Tile Transceiver PHY User Guide
- AN795: Implementing Guidelines for 10G Ethernet Subsystem Using Low Latency 10G MAC IP Core in Arria 10 Devices
- Stratix 10 Clocking and PLL User Guide

IP Register Mapping

The Stratix 10 LL 10GbE MAC IP core uses the same register map as Arria 10 LL 10GbE MAC IP core. The Multi-rate Ethernet PHY and 10GBASE-R PHY presets also use the same register map for both Stratix 10 and Arria 10 designs. The Stratix 10 LL 10GbE MAC IP core still supports backward compatibility with 10GbE IP with 64-bit Avalon Memory-Mapped (MM) adapter.

Related Links

Low Latency Ethernet 10G MAC User Guide

Signal Connectivity Differences between Stratix 10 and Arria 10 Ethernet Design Examples

For LL 10GbE MAC IP core, there are no new signals introduced for Stratix 10 devices. There are new asynchronous reset status signals introduced in Stratix 10 L/H-Tile Transceiver Native PHY IP Core. The differences apply to all Ethernet PHY IP cores, which include all variants of Multi-rate Ethernet PHY IP cores and 10GBASE-R PHY IP core.

Table 3. Interface signal differences between Stratix 10 L/H-Tile Transceiver Native PHY/Multi-rate Ethernet PHY and Arria 10 Transceiver Native PHY/Multi-rate Ethernet PHY

Note: <n> = The number of lanes.

Stratix 10 Interface Signals	Arria 10 Interface Signals	Comments
tx_analogreset_stat[<n>-1:0]	Not available	These reset status ports are newly introduced in Stratix 10 only. Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device.
rx_analogreset_stat[<n>-1:0]	Not available	
tx_digitalreset_stat[<n>-1:0]	Not available	
rx_digitalreset_stat[<n>-1:0]	Not available	
latency_sclk	Not available	Latency measurement input reference clock. Sampling clock for measuring the latency of the transceiver application interface block (AIB) datapath. This port is available when the latency measurement ports option in the Stratix 10 L/H-Tile Transceiver Native PHY IP core or the IEEE 1588 Precision Time Protocol option in the 1G/2.5G/5G/10G Multi-rate Ethernet PHY IP core is enabled.
reconfig_address [log_2<n>+10:0]	reconfig_address [log_2<n>+9:0]	Reconfiguration address signal connected to the reconfiguration block. Address bus that used to specify address to be accessed for both read and write operations.

Table 4. Interface signal differences between the Stratix 10 Transceiver Reset Controller IP and Arria 10 Transceiver Reset Controller IP

Note: <n> = The number of lanes.

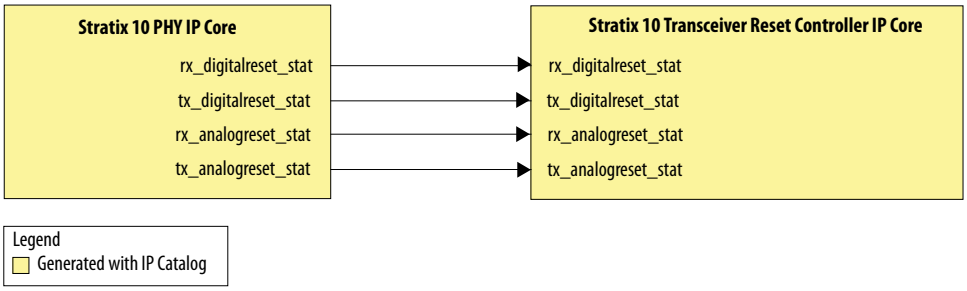
Stratix 10 Interface Signals	Arria 10 Interface Signals	Comments
tx_analogreset_stat[<n>-1:0]	Not available	This is reset status signal from the Transceiver Native PHY IP Core. There is one tx_analogreset_stat per channel. When asserted, reset sequence for TX PMA begins. When deasserted, reset sequence for TX PMA ends.
rx_analogreset_stat[<n>-1:0]	Not available	This is reset status signal from the Transceiver Native PHY IP Core. There is one rx_analogreset_stat per channel. When asserted, reset sequence for RX PMA begins. When deasserted, reset sequence for RX PMA ends.
tx_digitalreset_stat[<n>-1:0]	Not available	This is reset status signal from the Transceiver Native PHY IP Core. There is one tx_digitalreset_stat per channel. When asserted, reset sequence for TX PCS begins.

continued...

Stratix 10 Interface Signals	Arria 10 Interface Signals	Comments
		When deasserted, reset sequence for TX PCS ends.
`rx_digitalreset_stat[<n>-1:0]`	Not available	This is reset status signal from the Transceiver Native PHY IP Core. There is one `rx_digitalreset_stat` per channel. When asserted, reset sequence for RX PCS begins. When deasserted, reset sequence for RX PCS ends.

The following figure illustrates the connectivity of reset status signals for the Stratix 10 Ethernet 10G subsystem design. This is applicable if you use either the Stratix 10 L-tile/H-tile Native PHY IP core or the Multi-rate PHY IP core.

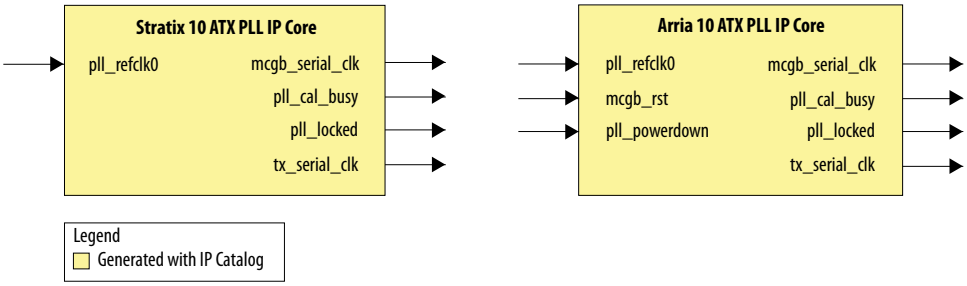
Figure 6. Reset Status Signals Connectivity Diagram for Stratix 10 PHY IP Core and Reset Controller IP Core



There are some changes to the ATX PLL and fPLL interface signals for the Stratix 10 devices compared to the Arria 10 devices. If you are migrating Ethernet designs from a Arria 10 device to a Stratix 10 device, remove the `mcgb_rst` and `pll_powerdown` reset signals because they are not available in Stratix 10.

The following figure illustrates the difference between Stratix 10 L-Tile/H-Tile ATX PLL and Arria 10 ATX PLL.

Figure 7. Comparison between Interface Signals for Stratix 10 L-Tile/H-Tile Transceiver ATX PLL and Arria 10 Transceiver ATX PLL

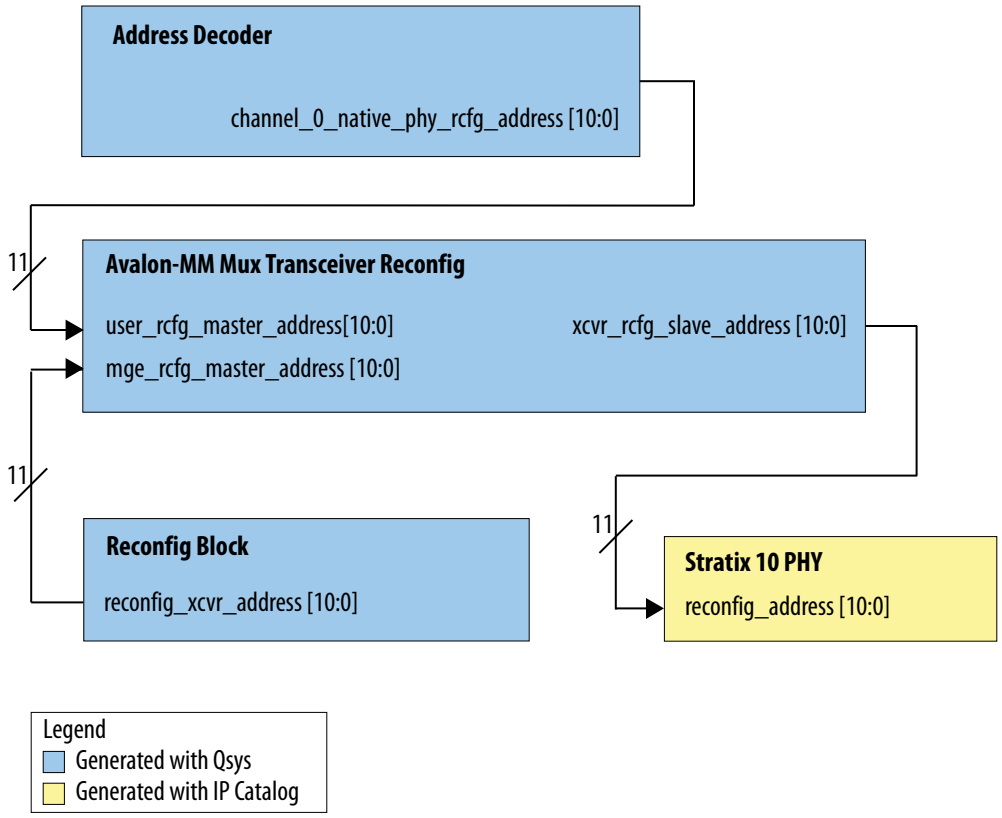


Another change on Stratix 10 L-Tile/H-Tile Transceiver PHY is the additional 1 bit added to the `reconfig_address` bus, compared to the Arria 10 Transceiver PHY version. The same change is required for the Multi-rate PHY as it is created by using the Native PHY as the baseline.

The following figure illustrates how to connect the `reconfig_address`.

Figure 8. Block Diagram on Reconfiguration Address Connectivity for Stratix 10 Ethernet Subsystem Design

The example shown is based on the Ethernet design example model. For the blocks that are generated by Qsys, you can obtain the modules from the design example files.



Related Links

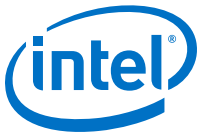
- Stratix 10 Low Latency Ethernet 10G MAC Design Example User Guide
- Stratix 10 L-Tile Transceiver PHY User Guide
- Stratix 10 H-Tile Transceiver PHY User Guide
- Intel Stratix 10 Clocking and PLL User Guide

Migration Flow

Only Quartus Prime Pro Edition software offers Stratix 10 designs. If you are using an Arria 10 Ethernet design from the Quartus Prime Standard Edition, you need to migrate to Quartus Prime Pro Edition version for any Stratix 10 design.

Related Links

Intel Quartus Prime Pro Edition Handbook Volume 1: Design and Compilation
Provides more information about upgrading IP cores and Qsys Pro systems to Quartus Prime Pro Edition software.



Revision History

Date	Version	Changes
June 2017	2017.06.19	Initial release.