AN 784: Partial Reconfiguration over PCI Express* Reference Design for Intel® Arria® 10 Devices

Updated for Intel® Quartus® Prime Design Suite: 18.1
1. Partial Reconfiguration over PCI Express* Reference Design for Intel® Arria® 10 Devices

The Partial Reconfiguration (PR) over PCI Express* (PCIe*) reference design demonstrates reconfiguring the FPGA fabric through the PCIe link in Intel® Arria® 10 devices. This reference design runs on a Linux system with the Intel Arria 10 GX FPGA development board. Adapt this reference design to your requirements by implementing the PR region logic using the given template. Run your custom design on this fully functional system that enables communication over PCIe.

Intel Arria 10 devices use the PR over PCIe solution to reconfigure the device, rather than Configuration via Protocol (CvP) update. Partial reconfiguration allows you to reconfigure a portion of the FPGA dynamically, while the remaining FPGA design continues to function. Create multiple personas for a particular region in your design, without impacting operation in areas outside this region. Partial reconfiguration enables the implementation of more complex FPGA systems.

Partial reconfiguration provides the following advancements to a flat design:

- Allows run-time design reconfiguration
- Increases scalability of the design through time-multiplexing
- Lowers cost and power consumption through efficient use of board space
- Supports dynamic time-multiplexing functions in the design
- Improves initial programming time through smaller bitstreams
- Reduces system down-time through line upgrades
- Enables easy system update by allowing remote hardware change

Intel Quartus® Prime Pro Edition software v.18.1 introduces a new and simplified compilation flow for partial reconfiguration.

Related Information

- Creating a Partial Reconfiguration Design
  For complete information on the partial reconfiguration design flow.
- Partially Reconfiguring a Design on Intel Arria 10 GX FPGA Development Board
  For a step-by-step tutorial on creating a partial reconfiguration design.
- Intel Arria 10 FPGA Development Kit User Guide
  For information on Intel Arria 10 GX FPGA development board overview and setup procedure.

1.1. Reference Design Overview

The reference design consists of the following components:
- **a10_pcie_reference_design**—top-level wrapper for the reference design, connecting the board support package (BSP) subsystem to the device pins.

- **bsp_top**—top-level of the design that contains all subsystems of the design. This module consists of three main sub-components - the PCIe IP core, the DDR4 External Memory Interfaces IP core, and the design top module. This layer of abstraction allows simulation of the design top module through simulated Avalon® Memory-Mapped (Avalon-MM) transactions.

- **design_core**—core of the design that handles generation of the PR region, the interface components such as clock crossing Avalon-MM logic and pipeline logic, clocks, and the global reset.

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**Figure 1. Intel Arria 10 PCIe Reference Design Block Diagram**

![Block Diagram](image)
1.1.1. Clocking Scheme

The reference design creates a separate Altera IOPLL IP core-generated clock. This clock creation decouples the PR logic clocking from both the PCIe clocking domain that runs at 250 MHz and the external memory interface (EMIF) clocking domain that runs at 330 MHz. The clock for PR Logic is set at 250 MHz. To ensure timing closure, modify the parameterization of the IOPLL IP core to a lower clock frequency.

![Timing Closure](image)

1.1.2. Memory Address Mapping

The PCIe IP core connects to the design core through two Avalon-MM master interfaces. These Avalon-MM master interfaces are base address registers (BARs), BAR 2 and BAR 4.

BAR 2 connects the PR driver to the following components:
- The PR IP core
- The system description ROM

The BAR 4 Avalon-MM connects to the following components:
- The freeze bridges
- The PR region controller
- Up to 8 kilobytes (KB) of memory in the PR region

The following table lists the memory address mapping for the PCIe IP core:

<table>
<thead>
<tr>
<th>Domain</th>
<th>Address Map</th>
<th>Base</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAR 2</td>
<td>System Description ROM</td>
<td>0x0000_0000</td>
<td>0x0000_0FFF</td>
</tr>
<tr>
<td>BAR 2</td>
<td>PR IP</td>
<td>0x0000_1000</td>
<td>0x0000_103F</td>
</tr>
<tr>
<td>BAR 4</td>
<td>PR Region</td>
<td>0x0000_0000</td>
<td>0x0000_FFFF</td>
</tr>
<tr>
<td>BAR 4</td>
<td>PR Region Controller</td>
<td>0x0001_0000</td>
<td>0x0001_000F</td>
</tr>
<tr>
<td>BAR 4</td>
<td>DDR4 Calibration Export</td>
<td>0x0001_0010</td>
<td>0x0001_001F</td>
</tr>
</tbody>
</table>

The EMIF IP provides status on DDR4 calibration. During initialization, the EMIF IP performs training to reset the DDR4 interface. The EMIF calibration flag reports the training success or the failure to the host. The host takes the necessary action in the event of a DDR4 training failure.

The following table lists the memory address mapping from the EMIF IP to the PR logic:

<table>
<thead>
<tr>
<th>Domain</th>
<th>Address Map</th>
<th>Base</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMIF</td>
<td>AVMM</td>
<td>0x0000_0000</td>
<td>0x0000_0FFF</td>
</tr>
<tr>
<td>DDR4 Calibration Export</td>
<td>AVMM Crossing Bridge</td>
<td>0x0001_0000</td>
<td>0x0001_000F</td>
</tr>
</tbody>
</table>
Table 2. DDR4 External Memory Interfaces (EMIF) Memory Address Map

<table>
<thead>
<tr>
<th>Address Map</th>
<th>Base</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>0x0000_0000</td>
<td>0x7fff_ffff</td>
</tr>
</tbody>
</table>

The PR logic accesses the 2 gigabyte (GB) DDR4 memory space using an Avalon-MM master interface.

1.1.3. Floorplanning

The floorplan constraints in your partial reconfiguration design physically partitions the device. This partitioning ensures that the resources available to the PR region are the same for any persona that you implement.

To maximize the fabric amount available for the PR region, the reference design constrains the static region to the smallest possible area.
Figure 3. Reference Design Floorplan

For more information about floorplanning, refer to Floorplan the Partial Reconfiguration Design section in Volume 1 of the Intel Quartus Prime Pro Edition Handbook.

Related Information
Floorplan the Partial Reconfiguration Design
1.2. Getting Started

This section describes the requirements and the procedure to run the reference design.

1.2.1. Hardware and Software Requirements

The reference design requires and uses the following hardware and software tools:

- Intel Arria 10 GX FPGA development board with the DDR4 module connected to Hi-Lo interface
- Linux Operating System - kernel version 3.10 or above
- Super user access on the host machine
- PCIe slot to plug-in the Intel Arria 10 GX FPGA development board
- Open source driver for this PR over PCIe reference design
- Intel Quartus Prime Pro Edition software v.18.1
- Intel FPGA Download Cable driver

Note:

- Validation testing used CentOS 7 to test the open source driver for this PR over PCIe reference design.
- The Linux driver accompanying this reference design is not a production driver. You must adapt this driver based on your design.

1.2.2. Installing the Intel Arria 10 GX FPGA Development Kit

For complete instructions on installing and powering the Intel Arria 10 GX FPGA development board in your Linux system, refer to Intel Arria 10 FPGA Development Kit User Guide.

Note:

Before powering the board, set the switch 4 (FACTORY) of the DIP switch bank (SW6) to ON. Setting this switch to ON loads the factory image area of the flash memory at boot time. Program the reference design into this factory image area. For complete instructions on flashing the reference design onto the board, refer to Bringing Up the Reference Design.

Related Information

- Intel Arria 10 FPGA Development Kit User Guide
- Bringing Up the Reference Design on page 10

1.2.3. Installing the Linux Driver

The reference design includes the complete source code for the open source Linux driver, developed and tested for this reference design.

The Linux driver for this design requires the debugfs. Run the following command verify that the debugfs is available:

```
mount | grep ^debugfs
```

For more information on the debugfs file system, please refer to the CentOS documentation.
**Important:** This driver only supports CentOS 7.

You must install all the prerequisite packages before installing this driver. To install the prerequisite packages, run the following commands:

```bash
yum groupinstall "Development Tools"
yum install ncurses-devel
yum install qt-devel
yum install hmaccalc zlib-devel binutils-devel elfutils-libelf-devel
```

To install the driver, follow these steps:

1. Ensure the driver source code is available on your machine. The source code is available at the following location:
   ```text
   https://github.com/intel/fpga-partial-reconfig/tree/master/software/drivers
   ```
2. To compile all the necessary driver modules, run the following command:
   ```bash
   make DEVICE="a10"
   ```
   **Note:** To enable verbose messaging, use the option `VERBOSE=true` with the `make` command.

   Ensure that the following three kernel object files are present in the driver source directory after running this command:
   ```text
   • fpga-mgr-mod.ko
   • fpga-pcie-mod.ko
   ```
3. To copy the modules to the right location and update the module dependency database, run the following command:
   ```bash
   sudo make install
   ```
4. To deploy an instance of the driver for each Intel FPAG device, run the following command:
   ```bash
   sudo modprobe fpga-pcie-mod
   ```
5. To verify successful installation of the driver, run the following command:
   ```bash
   lspci -vvvd1172:
   ```
   Upon successful installation, the resulting output displays the following at the end:
   ```text
   Kernel driver in use: fpga-pcie
   Kernel modules: fpga_pcie_mod
   ```
   **Note:** The above command only works when the design is loaded onto the board and the computer has been power-cycled.

**Uninstalling the Linux Driver**

If you wish to uninstall the Linux driver, follow these steps:
1. Partial Reconfiguration over PCI Express* Reference Design for Intel® Arria® 10 Devices

1.2.4. Bringing Up the Reference Design

The reference design is available in the following location:

https://github.com/intel/fpga-partial-reconfig

To access the reference design, navigate to the ref_designs sub-folder. Copy the a10_pcie_devkit_cvp folder to the home directory in your Linux system.

To bring up the reference design on the board:
1. Plug-in the Intel Arria 10 GX FPGA development board to an available PCIe slot in your host machine.
2. Connect the host machine's ATX auxiliary power connector to the 12 V ATX input J4 of the development board.
3. Power-up the host machine.
4. Verify the micro-USB cable connection to the FPGA development board. Ensure that no other applications that use the JTAG chain are running.
5. Navigate to the a10_pcie_devkit_cvp/software/installation folder in your system.
6. To overwrite the existing factory image on the board with the reference design, execute the flash.pl script.
7. Pass the JTAG cable number of your connected device as an argument to the script (for example, perl flash.pl 1).

Running this script configures the device with the contents of the flash.pof file. This parallel object file comes directly from the a10_pcie_devkit_cvp.sof file present in the output_files directory. The flash.pof file acts as the base image for the reference design.

Note: Ensure successful compilation of the design before running this script.
8. Power-cycle the host machine.

1.3. Reference Design Components

The reference design contains the following design components.

1.3.1. BSP Top

This Platform Designer system contains all the subsystems of this reference design. The system comprises the following three main components:
• The top-level design
• The PCIe IP
• The DDR4 EMIF IP

The system connects to external pins through the `a10_pcie_ref_design.sv` wrapper.

### 1.3.1.1. PCI Express IP core

The Intel Arria 10 Hard IP for PCI Express IP core is Gen3x8 with a 256-bit interface, running at 250 MHz.

The following table provides information on the PCI Express IP parameters that the reference design uses that are different from the default settings:

<table>
<thead>
<tr>
<th>Setting</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Settings</td>
<td>Application interface type</td>
<td>Avalon-MM with DMA</td>
</tr>
<tr>
<td></td>
<td>Hard IP mode</td>
<td>Gen3:x8, Interface: 256-bit, 250 MHz</td>
</tr>
<tr>
<td></td>
<td>Port type</td>
<td>Native endpoint</td>
</tr>
<tr>
<td></td>
<td>RX buffer credit allocation for received</td>
<td>Low</td>
</tr>
<tr>
<td></td>
<td>requests vs completions</td>
<td></td>
</tr>
<tr>
<td>Avalon-MM Settings</td>
<td>Enable control register access (CRA) Avalon-MM</td>
<td>Disable</td>
</tr>
<tr>
<td>Base Address Registers - BAR2</td>
<td>Type</td>
<td>32-bit non-prefetchable memory</td>
</tr>
<tr>
<td>Base Address Registers - BAR4</td>
<td>Type</td>
<td>32-bit non-prefetchable memory</td>
</tr>
<tr>
<td>Device Identification Registers</td>
<td>Vendor ID</td>
<td>0x00001172</td>
</tr>
<tr>
<td></td>
<td>Device ID</td>
<td>0x00005052</td>
</tr>
<tr>
<td></td>
<td>Revision ID</td>
<td>0x00000001</td>
</tr>
<tr>
<td></td>
<td>Class code</td>
<td>0x00ea0001</td>
</tr>
<tr>
<td></td>
<td>Subsystem Vendor ID</td>
<td>0x00001172</td>
</tr>
<tr>
<td></td>
<td>Subsystem Device ID</td>
<td>0x00000001</td>
</tr>
<tr>
<td>PCI Express/PCI Capabilities - Device</td>
<td>Maximum payload size</td>
<td>256 Bytes</td>
</tr>
<tr>
<td>Configuration, Debug, and Extension Options</td>
<td>Enable Intel Arria 10 GX FPGA Development Kit Connection</td>
<td>Enable</td>
</tr>
<tr>
<td>PHY Characteristics</td>
<td>Requested equalization far-end TX preset</td>
<td>Preset 9</td>
</tr>
</tbody>
</table>

**Note:** Instantiate the PCI Express IP core as part of a Platform Designer system.

### 1.3.1.2. Intel Arria 10 DDR4 External Memory Interfaces IP Core

The `ddr4_emif` logic includes the Intel Arria 10 External Memory Interfaces IP core. This IP core interfaces to the DDR4 external memory, with a 64-bit interface that runs at 1066.0 MHz. Also, the IP core provides 2 GB of DDR4 SDRAM memory space. The EMIF Avalon-MM slave runs at 300 MHz.
The following table lists the Intel Arria 10 External Memory Interfaces IP parameters that are different from the Intel Arria 10 GX FPGA Development Kit with DDR4 HILO preset settings:

<table>
<thead>
<tr>
<th>Setting</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory - Topology</td>
<td>DQ width</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td>DQ pins per DQS group</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Number of DQS groups</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Alert# pin placement</td>
<td>I/O Lane with Address/Command Pins</td>
</tr>
<tr>
<td></td>
<td>Address/Command I/O lane of ALERT#</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>Pin index of ALERT#</td>
<td>0</td>
</tr>
</tbody>
</table>

1.3.1.3. Design Top

This component forms the core of the design, and includes the following:

- Reset logic
- PR region
- Partial Reconfiguration IP core
- Clock crossing and pipe-lining for Avalon-MM Transactions
- System description ROM
- PLL

1.3.1.3.1. Global Reset Logic

The PLL generates the main clock for this design. All logic, excluding the PCIe ip, pr ip, and ddr4 emif run using this 250 MHz clock. The PCIe core generates the global reset, along with the PLL reset signal. On power up, a countdown timer, tcd2um counts down using the internal 50 MHz oscillator, to a 830 μs delay. Until the timer reaches this delay, the PLL is held in reset, deasserting the locked signal. This action freezes the design. Because the PLL locked signal is ORed with the PCIe reset, the design also is held in reset. Once the timer reaches 830 μs, the design functions normally, and enters a known state.

1.3.1.3.2. PR Region Wrapper

The PR region wrapper contains the PR region controller, freeze bridges, and the personas. The PR region controller interacts with the driver over the Avalon-MM interface to initiate PR. The PR region controller acts as a bridge to communicate with the PR region for freeze and start requests initiation.

1.3.1.3.3. Intel Arria 10 Partial Reconfiguration Region Controller IP Core

Use the Intel Arria 10 Partial Reconfiguration Region Controller IP core to initiate a freeze request to the PR region. The PR region finalizes any actions, on freeze request acknowledgment. The freeze bridges also intercept the Avalon-MM interfaces to the PR region, and correctly responds to any transactions made to the PR region during
partial reconfiguration. Finally, on PR completion, the region controller issues a stop request, allowing the region to acknowledge, and act accordingly. The fpga-region-controller program provided with this reference design performs these functions.

The reference design configures the Partial Reconfiguration Region Controller IP core to operate as an internal host. The design connects this IP core to the PCI Express IP core, via an instance of the Avalon-MM interface. The PR IP core has a clock-to-data ratio of 1. Therefore, the PR IP core is not capable of handling encrypted or compressed PR data.

The following table lists the configuration fields of the Intel Arria 10 Hard IP for PCI Express IP core that are different from the preset settings:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable JTAG debug mode</td>
<td>Disable</td>
</tr>
<tr>
<td>Enable Avalon-MM slave interface</td>
<td>Enable</td>
</tr>
<tr>
<td>Input data width</td>
<td>32</td>
</tr>
</tbody>
</table>

### 1.3.1.3.4. Partial Reconfiguration Logic

The reference design provides the following personas:

<table>
<thead>
<tr>
<th>Table 5. Reference Design Personas</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Persona</strong></td>
</tr>
<tr>
<td>DDR4 access</td>
</tr>
<tr>
<td>Basic DSP</td>
</tr>
<tr>
<td>Basic arithmetic</td>
</tr>
<tr>
<td>Game of Life</td>
</tr>
</tbody>
</table>

Each persona has an 8-bit `persona_id` field in the `pr_data` register to indicate a unique identification number. A 32-bit control register and 16 I/O registers follow the 8-bit `persona_id`. The 16 I/O registers are 32-bit each, with 8 bits for device inputs, and 8 bits for device outputs. Each persona uses these registers in different ways. For more information, refer to the source code for each of the personas.

Additionally, the reference design provides a template to implement your custom persona. This template persona allows you modify the RTL, create a wrapper to interface with the register file, compile, and run your design.

### 1.4. Compiling the Reference Design

1. To compile the base revision of the reference design, run the following command from the project directory level:

   ```bash
   quartus_sh --flow compile a10_pcie_devkit_cvp -c a10_pcie_devkit_cvp
   ```

Send Feedback
All the implementation revisions, except the base revision contain the following QDB file partition assignment in their respective .qsf files:

```plaintext
set_instance_assignment -name QDB_FILE_PARTITION \
  output_files/a10_pcie_devkit_cvp_static.qdb -to |
```

This assignment imports the .qdb file representing the reference design static region logic into the subsequent PR persona implementation compile. Each implementation revision also contains an ENTITY_REBINDING assignment. This assignment links the hierarchy of the static region and the hierarchy of the PR persona. For example, a10_pcie_devkit_cvp_basic_arithmetic.qsf contains the following entity rebinding assignment:

```plaintext
set_instance_assignment -name ENTITY_REBINDING \
  basic_arithmetic_persona_top -to \
  u_top|design_core|pr_region_wrapper|pr_persona_wrapper|u_pr_logic
```

For more information, please refer to the Partial Reconfiguration Design Flow section in the Partial Reconfiguration User Guide.

2. To compile the PR implementation revisions that represent the PR personas, run the following commands:

```plaintext
quartus_sh --flow compile a10_pcie_devkit_cvp -c \
  a10_pcie_devkit_cvp_basic_arithmetic
quartus_sh --flow compile a10_pcie_devkit_cvp -c \
  a10_pcie_devkit_cvp_basic_dsp
quartus_sh --flow compile a10_pcie_devkit_cvp -c \
  a10_pcie_devkit_cvp_gol
quartus_sh --flow compile a10_pcie_devkit_cvp -c \
  a10_pcie_devkit_cvp_ddr4_access
```

### Related Information

- Partial Reconfiguration Design Flow
- AN 797: Partially Reconfiguring a Design on Intel Arria 10 GX FPGA Development Board

### 1.5. Testing the Reference Design

The reference design provides the following utilities for programming the FPGA board:

- `program-fpga-jtag`
- `fpga-configure`
- `fpga-region-controller`

The design also includes an `example_host_uio` application to communicate with the device, and demonstrate each of the personas.

#### 1.5.1. `program_fpga_jtag`

Use the `program_fpga_jtag` script to program the entire device (full-chip programming) without any requirement for reboot.

`program_fpga_jtag` performs the following functions:
• Uses the Intel Quartus Prime Programmer to program the device.
• Accepts an SRAM Object File (.sof) and configures the target device over a JTAG interface.
• Communicates with the driver to perform the following functions:
  ‒ Disable upstream AER (advanced error reporting)
  ‒ Save state
  ‒ Restore AER
  ‒ Restore state

<table>
<thead>
<tr>
<th>Table 6. program_fpga_jtag Command-Line Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option</td>
</tr>
<tr>
<td>---------------------------------------------</td>
</tr>
<tr>
<td>-f=, --file=[&lt;filename&gt;]</td>
</tr>
<tr>
<td>-c=, --cable=[&lt;cable number&gt;]</td>
</tr>
<tr>
<td>-i, --index</td>
</tr>
<tr>
<td>-h, --help</td>
</tr>
</tbody>
</table>

*Note:* Use the following command to obtain the device index:

```
/sbin/lspci -d 1172:
```

For example, consider that the command returns the following output:

```
03:00.0 Class ea00: Altera Corporation Device 5052 (rev 01)
```

The first value is the device index. Prepend 0000 to this value. In this case, your device index is **0000.03:00.0**.

1.5.2. *fpga*-configure

Use the *fpga*-configure utility to perform partial reconfiguration. The script accepts a .rbf file for a given persona. The script performs the following functions:

• Communicates with the driver to remove device sub-drivers, if any
• Communicates with the *fpga*-region-controller script to assert/de-assert freeze
• Writes the .rbf to the Partial Reconfiguration Controller IP core
• Re-deploys the sub-drivers, if any, that are required upon successful PR

To perform PR over PCIe, run the following command:

```
fpga-configure -p <path-to-rbf> <region_controller_addr>
```
### Table 8. example_host_uio Command-Line Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-s, --seed [seed]</td>
<td>Specifies the seed to use for number generation. Default value is 1.</td>
</tr>
<tr>
<td>-v, --verbose</td>
<td>Allows you to print additional information during execution. This option is disabled by default.</td>
</tr>
<tr>
<td>-n, --iterations</td>
<td>Allows you to specify the iterations for the test you wish to perform. Default value is 3.</td>
</tr>
<tr>
<td>-h, --help</td>
<td>Provides help for example_host_uio application.</td>
</tr>
</tbody>
</table>

**Note:** Running example_host_uio without any command-line arguments uses seed value of 1, 3 iterations.

### Signal Tap

The reference design supports signal tapping the PR regions, through hierarchical hubs. This feature facilitates the on-chip debugging of a specific persona. The static region contains the SLD agent, that communicates with an SLD host. You must instantiate the SLD host in the persona that you wish to signal tap. You must include the .stp file in the revision of a given persona. Do not include the signal tap file in the base revision, or the .qsf file of other personas, if the .stp file is specific to a persona.

Follow these guidelines when signal tapping the PR logic:

- Use pre-synthesis registers
- An instance cannot cross partition boundaries
- Do not trigger across partition boundaries

1.5.3.1. Compiling the Example Applications

The reference design software applications are available in the `software/util` directory. Each application has a respective sub-directory structure, with a corresponding Makefile.

To build the example application:
1. To compile the `example_host` module, type the following from the Linux shell:

```bash
  cd source/util
  make
```

This command generates the executable within the sub-directory. For example:

```bash
  ./example_host_uio -s 1 -n 100 -v
```

This command seeds the input generation with a value of 1, perform 100 iterations, and print more information on the current status.

1.5.3.2. Programming the Design Using Example Applications

The following steps describe programming your design using the provided scripts:

1. To program the DDR access persona’s `.sof` file after design compilation, type the following from the Linux shell:

   ```bash
   program-fpga-jtag -f=a10_pcie_devkit_cvp_ddr4_access.sof -c=1 -i=1
   ```

2. To verify the functionality of the design, type the following from the Linux shell:

   ```bash
   ./example_host_uio
   ```

3. To program the basic DSP persona’s `.rbf` file after design compilation, type the following from the Linux shell:

   ```bash
   fpga-configure -p a10_pcie_devkit_cvp_basic_dsp.pr_partition.rbf 10000
   ```

4. To verify the functionality of the design, type the following from the Linux shell:

   ```bash
   ./example_host_uio
   ```

5. To program the basic arithmetic persona’s `.rbf` file after design compilation, type the following from the Linux shell:

   ```bash
   fpga-configure -p a10_pcie_devkit_cvp_basic_arithmetic.pr_partition.rbf 10000
   ```

6. To verify the functionality of the design, type the following from the Linux shell:

   ```bash
   ./example_host_uio
   ```

7. To program the Game of Life persona’s `.rbf` file after design compilation, type the following from the Linux shell:

   ```bash
   fpga-configure -p a10_pcie_devkit_cvp_gol.pr_partition.rbf 10000
   ```
8. To verify the functionality of the design, type the following from the Linux shell:

```
./example_host_uio -v
```

### 1.6. Extending the Reference Design with Custom Persona

This reference design provides an example template to create your own personas for PR over PCIe. To extend the reference design with your custom persona:

1. Navigate to the `a10_pcie_devkit_cvp` folder:

   ```bash
   cd a10_pcie_devkit_cvp
   ```

2. Create a copy of the `pr_logic_impl_template.qsf.template` implementation revision file:

   ```bash
   cp pr_logic_impl_template.qsf.template <persona_impl_revision_name>.qsf
   ```

3. Create a folder and copy your persona-specific RTL to this folder:

   ```bash
   mkdir <persona_name>
   cp <custom_persona>.sv <persona_name>/
   ```

4. Your custom top-level entity must match the ports for the `custom_persona` module, defined in the `source/templates/pr_logic_template.sv` file. The following example shows interfacing your design with the Avalon-MM interface, controlled over PCIe register file:

   ```verilog
   module custom_persona #(parameter REG_FILE_IO_SIZE = 8)
   ( //clock
     input wire clk,
     //active low reset, defined by hardware
     input wire rst_n,
     //Persona identification register, used by host in host program
     output wire [31:0] persona_id,
     //Host control register, used for control signals.
     input wire [31:0] host_cntrl_register,
     // 8 registers for host -> PR logic communication
     input wire [31:0] host_pr [0:REG_FILE_IO_SIZE-1],
     // 8 Registers for PR logic -> host communication
     output wire [31:0] pr_host [0:REG_FILE_IO_SIZE-1]
   );
   ```

   Utilize any of the parallel I/O port (PIO) register files for customization. The `host_pr` register sends the data from the persona to the host machine. The `pr_host` register sends the data from the host machine to the persona.

5. In your top-level entity file, specify the persona ID as any 32-bit value:

   ```verilog
   assign persona_id = 32'h0000_aeed;
   ```

   **Note:** The example template uses only 8 bits, but you can specify any value, up to 32 bits.
6. Set the unused output ports of the `pr_host` register to 0:

```vhdl
generate
genvar i;
//Tying unused output ports to zero.
for (i = 2; i < REG_FILE_IO_SIZE; i = i + 1) begin
  assign pr_host [i] = 32'b0;
end
endgenerate
```

7. Modify your `persona_impl_revision_name.qsf` to include the following assignments:

```plaintext
set_global_assignment -name TOP_LEVEL_ENTITY a10_pcie_ref_design
set_global_assignment -name SYSTEMVERILOG_FILE \<persona_name>/\<custom_persona>.sv
set_global_assignment -name QSYS_FILE <persona_specific_qsys_file>
set_global_assignment -name IP_FILE <persona_specific_ip_file>
set_instance_assignment -name QDB_FILE_PARTITION \a10_pcie_devkit_cvp_static.qdb -to |
set_instance_assignment -name ENTITY_REBINDING \<custom_persona_top_level_entity> -to u_top\design_core\pr_region_wrapper\pr_persona_wrapper|u_pr_logic
```

8. Update the partial reconfiguration flow script to define your new PR implementation.

9. Update the `a10_pcie_devkit_cvp.qpf` project file to include your implementation revisions:

```plaintext
PROJECT_REVISION = "<persona_impl_revision_name>"
```

10. Compile the revision.

For complete information on adding a custom persona to a PR design, refer to Adding a New Persona to the Design section in the Partially Reconfiguring a Design on Intel Arria 10 GX FPGA Development Board application note.

**Related Information**

Adding a New Persona to the Design

### 1.7. Document Revision History for AN 784: Partial Reconfiguration over PCI Express Reference Design for Intel Arria 10 Devices

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2018.09.24       | 18.1.0                     | • Updated the Compiling the Reference Design to eliminate the need for manual export of finalized snapshot of the static region.  
                   |                             | • Other minor text edits |
| 2018.07.03       | 18.0.0                     | Updated the Compiling the Reference Design with the correct command for .qdb file export. |
| 2018.05.07       | 18.0.0                     | • Compilation flow change  
                   |                             | • Other minor text edits |

[continued...](#)
## Changes

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2017.11.06       | 17.1.0                     | • Updated the Hardware and Software Requirements section with additional reference design requirements  
|                  |                            | • Updated the Installing the Linux Driver section with detailed instructions on installing the open source Linux driver  
|                  |                            | • Version update  
|                  |                            | • Minor text edits                                                    |
| 2017.05.08       | 17.0.0                     | • Reference design flow updated  
|                  |                            | • New persona - Game of Life added                                    |
| 2016.10.31       | 16.1.0                     | Initial Release                                                        |
## A. Reference Design Files

### Table 9. Reference Design Files List

<table>
<thead>
<tr>
<th>Type</th>
<th>File/Folder</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IP files</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>source</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>static_region</strong></td>
<td>Contains the IP files for the Intel Arria 10 External Memory Interfaces IP core, Intel Arria 10 Hard IP for PCI Express IP core, and devkit pins.</td>
</tr>
<tr>
<td></td>
<td><strong>ip</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>bsp_top</strong></td>
<td></td>
</tr>
<tr>
<td><strong>source</strong></td>
<td><strong>static_region</strong></td>
<td>Contains the IP file for the Intel Arria 10 Partial Reconfiguration Controller IP core, system description ROM, calibration I/O, and all the interface components.</td>
</tr>
<tr>
<td></td>
<td><strong>ip</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>design_top</strong></td>
<td></td>
</tr>
<tr>
<td><strong>source</strong></td>
<td><strong>static_region</strong></td>
<td>Contains the freeze bridges, the region controller, and the JTAG SLD agent.</td>
</tr>
<tr>
<td></td>
<td><strong>ip</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>pr_subsystem</strong></td>
<td></td>
</tr>
<tr>
<td><strong>common</strong></td>
<td><strong>reg_file</strong></td>
<td>Contains all the IP files for the register file system, that is common across all personas.</td>
</tr>
<tr>
<td></td>
<td><strong>ip</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>reg_file</strong></td>
<td></td>
</tr>
<tr>
<td><strong>common</strong></td>
<td><strong>sld_jtag_host</strong></td>
<td>Contains the JTAG SLD host for the PR region signal tapping. These files are applicable to all the personas.</td>
</tr>
<tr>
<td></td>
<td><strong>ip</strong></td>
<td></td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Type</th>
<th>File/Folder</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>common</td>
<td>sld_jtag_agent</td>
<td>Contains the JTAG SLD agent for the PR region signal tapping. These files are applicable to the static region.</td>
</tr>
<tr>
<td>source</td>
<td>emif_interface</td>
<td>Contains the IP files for the EMIF logic inside the PR persona.</td>
</tr>
<tr>
<td>Platform Designer System Files</td>
<td>source</td>
<td>Contains the following three Platform Designer (Standard) subsystems: \n• bsp_top.qsys—top-level subsystem, containing the PCIe IP core and the External Memory Interfaces IP core. \n• design_top.qsys—static region, encompassing all the Avalon-MM interface logic, reset logic, and PR Region Controller IP core. \n• pr_subsystem.qsys—contains all the logic to communicate and interact with the PR region.</td>
</tr>
<tr>
<td>SystemVerilog design files</td>
<td>static_region</td>
<td>Contains the top-level wrapper. Also contains the SystemVerilog description for generic components in the three subsystems, and the PR region wrapper.</td>
</tr>
<tr>
<td>source</td>
<td>basic_dsp_persona</td>
<td>Contains all the source files for the basic DSP persona.</td>
</tr>
<tr>
<td>source</td>
<td>basic_arithmetic_persona</td>
<td>Contains all the source files for the basic arithmetic persona.</td>
</tr>
<tr>
<td>source</td>
<td>ddr4_access_persona</td>
<td>Contains all the source files for the DDR4 access persona.</td>
</tr>
<tr>
<td>source</td>
<td>gol_persona</td>
<td>Contains all the source files for the Game of Life persona.</td>
</tr>
<tr>
<td>source</td>
<td>templates</td>
<td>Example personas that use the template for persona configuration. These examples demonstrate integrating a custom persona RTL into the reference design.</td>
</tr>
<tr>
<td>Memory files</td>
<td>avalon_config.hex</td>
<td>Used for system description ROM.</td>
</tr>
</tbody>
</table>
### A. Reference Design Files

#### AN-784 | 2018.09.24

<table>
<thead>
<tr>
<th>Type</th>
<th>File/Folder</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synopsys Design Constraints Files</td>
<td>a10_pcie_devkit_cvp.sdc</td>
<td>Synthesis constraints for the design.</td>
</tr>
<tr>
<td></td>
<td>auxiliary.sdc</td>
<td>Provides exceptions.</td>
</tr>
<tr>
<td></td>
<td>jtag.sdc</td>
<td>Auto-generated constraints from <code>pcie_subsystem_alt_pr.ip</code> file.</td>
</tr>
<tr>
<td>Intel Quartus Prime Project File</td>
<td>a10_pcie_devkit_cvp.qpf</td>
<td>Contains all the revisions.</td>
</tr>
<tr>
<td>Intel Quartus Prime Settings Files</td>
<td>a10_pcie_devkit_cvp.qsf</td>
<td>Base revision settings file for DDR4 access persona.</td>
</tr>
<tr>
<td></td>
<td>a10_pcie_devkit_cvp_ddr4_access.qsf</td>
<td>Implementation revision settings file for DDR4 access persona.</td>
</tr>
<tr>
<td></td>
<td>a10_pcie_devkit_cvp_basic_dsp.qsf</td>
<td>Implementation revision settings file for basic DSP persona.</td>
</tr>
<tr>
<td></td>
<td>a10_pcie_devkit_cvp_basic_arithmetic.qsf</td>
<td>Implementation revision settings file for basic arithmetic persona.</td>
</tr>
<tr>
<td></td>
<td>a10_pcie_devkit_cvp_gol.qsf</td>
<td>Implementation revision settings file for Game of Life persona.</td>
</tr>
</tbody>
</table>