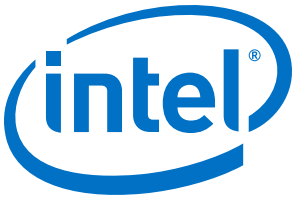

Interlaken IP Core Feature and Interface Differences Between Stratix 10, Arria 10, and Stratix V Devices

AN-782
2017.06.12

Contents

1 Interlaken IP Core Feature and Interface Differences..... 3

2 Document Revision History..... 5

1 Interlaken IP Core Feature and Interface Differences

Interlaken is a high-speed serial communication protocol for chip-to-chip packet transfers at rates from 25 Gbps to 300 Gbps. Intel® FPGA's Interlaken IP solution continues to scale with today's demand for more bandwidth and higher performance needs.

This application note summarizes the differences between Interlaken IP cores that target the Stratix® 10, Arria® 10, and Stratix V devices.

Table 1. Comparison of Interlaken IP Cores

Device Family	Stratix V		Arria 10		Stratix 10
IP Core Variant	**50G Interlaken IP core**	**100G Interlaken IP core**	**50G Interlaken IP core**	**100G Interlaken IP core**	**Interlaken IP core (2nd Generation)** [1]
Protocol Compliant	Interlaken Protocol Specification, Revision 1.2	Interlaken Protocol Specification, Revision 1.2	Interlaken Protocol Specification, Revision 1.2	Interlaken Protocol Specification, Revision 1.2	Interlaken Protocol Specification, Revision 1.2
Supported **Lane x Data Rate** (per lane) combinations	8x6.25 Gbps	24x6.25 Gbps 12x10.3125 Gbps 12x12.5 Gbps	8x6.25 Gbps	24x6.25 Gbps 12x10.3125 Gbps 12x12.5 Gbps	• In devices with L-tile transceivers: — 4x6.25 Gbps — 12x10.3125 Gbps — 12x12.5 Gbps • In devices with H-tile transceivers: — 6x25.28 Gbps — 12x25.28 Gbps
Meta-Frame	128 - 8192	128 - 8192	128 - 8192	128 - 8192	64 - 8192
Transceiver Reference Clock Frequency	Multiple	Multiple	Multiple	Multiple	Multiple
Advanced Error Reporting and Handling	Yes	Yes	Yes	Yes	Yes
M20K ECC Support	No	Yes	No	Yes	Yes

continued...

1 This IP core is only supported in the Quartus Prime Pro 17.1 Stratix 10 ES Editions. For more details, contact Intel FPGA.

Device Family	Stratix V		Arria 10		Stratix 10
IP Core Variant	50G Interlaken IP core	100G Interlaken IP core	50G Interlaken IP core	100G Interlaken IP core	Interlaken IP core (2nd Generation) [1]
Diagnostic Features	No	Yes	No	Yes	Yes
In-band Flow Control Functionality	Yes	Yes	Yes	Yes	Yes
Transceiver Native PHY ADME	No	No	Yes	Yes	Yes
Number of Calender Pages	1, 2, 4, 8, 16	1, 2, 4, 8, 16	1, 2, 4, 8, 16	1, 2, 4, 8, 16	1, 2, 4, 8, 16
Transfer Mode Selection	Interleaved Packet	Interleaved Packet	Interleaved Packet	Interleaved Packet	Interleaved Packet
Data Format	Single segment	Single segment Dual segment	Single segment	Single segment Dual segment	Single segment
Example Design Support	Simulation	Simulation	Simulation Synthesis	Simulation Synthesis	Simulation Synthesis
Resource Utilization - ALMS	9800 [2, 3]	17200 [2, 4]	9900 [3]	17500 [4]	20100 [4]
Resource Utilization - Logic Registers (Primary - P, Secondary - S) [5]	20700 (P) 1700 (S) [2, 3]	34200 (P) 2300 (S) [2, 4]	20600 (P) 1500 (S) [3]	34100 (P) 1800 (S) [4]	38000 (P) 9000 (S) [4]
Resource Utilization - M20K Blocks	17 [2, 3]	38 [2, 4]	17 [3]	38 [4]	44 [4]

Related Links

- Interlaken IP Solutions Webpage
- 50G Interlaken MegaCore Function User Guide
- 100G Interlaken MegaCore Function User Guide
- Interlaken IP Core (2nd Generation) User Guide

1 This IP core is only supported in the Quartus Prime Pro 17.1 Stratix 10 ES Editions. For more details, contact Intel FPGA.

2 For Stratix V GX devices.

3 IP core variant: 8x6.25

4 IP core variant:12x10.3125

5 Primary registers are the core logic registers; Secondary registers are the implementation, routing and timing closure optimization registers.

2 Document Revision History

Table 2. Document Revision History

Date	Changes
2017.06.12	• Added support for 6x25.28 Gbps and 12x25.28 Gbps configurations. • Updated the resource utilization for Stratix 10 variation.
2016.10.31	Initial release