



AN 775: I/O Timing Information Generation Guidelines



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1. AN775: I/O Timing Information Generation Guidelines

This Application Note demonstrates techniques to generate I/O timing information for any given device using the Quartus® Prime software.

I/O timing information is crucial for early analysis during PCB board design stages. Generate timing parameters to help you adjust the timing budget of your design, considering I/O standards and pin placement. The relevant I/O timing information parameters are: input setup time t_{su} , input hold time t_h , and clock to output delay t_{co} .

Generating I/O timing information includes the following steps:

1. Create a simple D flipflop (DFF) design project that targets the device for analysis.
2. Assign the I/O standard and pin location constraints.
3. Run compilation and timing analysis.
4. Determine t_{su} , t_h , and t_{co} value.

This document provides both GUI and script-based generation examples.

1.1. I/O Timing Parameters

The following are timing parameters relevant for analysis:

Table 1. I/O Timing Parameter Description

Timing Parameter	Description
Input setup time (t_{su})	Data delay from input pin to input register, plus the micro setup time of the input register, minus the clock delay from input pin to input register
Input hold time (t_h)	Clock delay from input pin to input register, minus data delay from input pin to input register, plus micro hold time of the input register
Clock to output delay (t_{co})	Delay from clock pin to I/O output register, plus register clock to output delay, plus delay from output register to output pin

1.2. Setup Requirements

This demonstration requires the current version of the Quartus Prime software. The script-based technique is only available on Linux platforms.

Note: This document assumes basic familiarity with the Quartus Prime software, the Pin Planner, and the TimeQuest Timing Analyzer.

Related Information

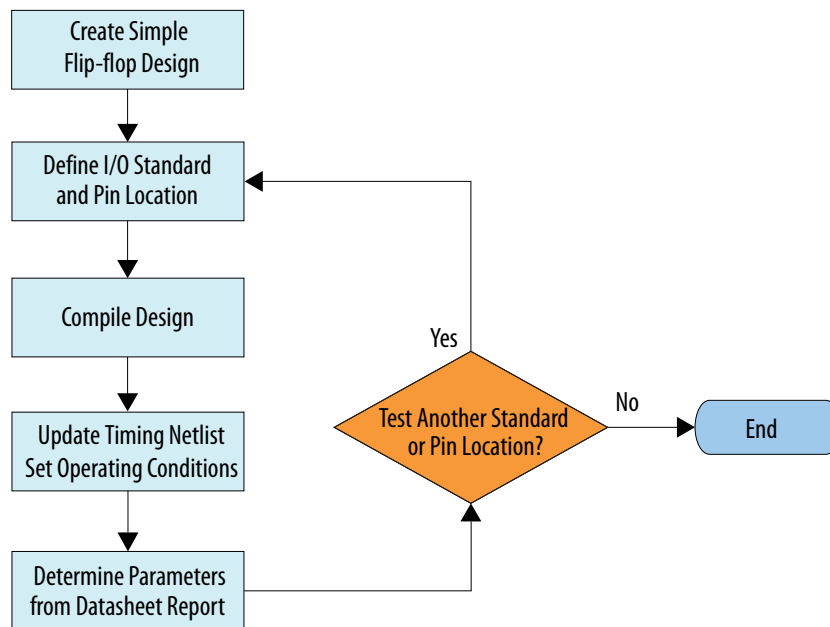
- [Managing Device I/O Pins](#)
- [The TimeQuest Timing Analyzer](#)

- TimeQuest Timing Analyzer Cookbook

1.3. I/O Timing Information Generation Flow

The following diagram shows the I/O timing information generation flow:

Figure 1. I/O Timing Information Generation Flow

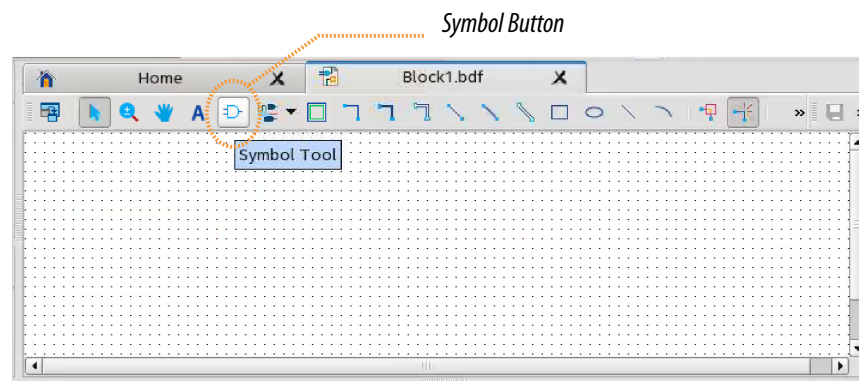


1.3.1. Create and Synthesize a Simple Flip-flop Design

Create the elements to compute timing parameters:

1. Open or create a new Quartus Prime project.
2. Click **Assignments** ► **Device** and specify the target device.
3. Click **New** and create a **BlockDiagram/Schematic File**.
4. To add components to the schematic, click on the **Symbol Tool**.

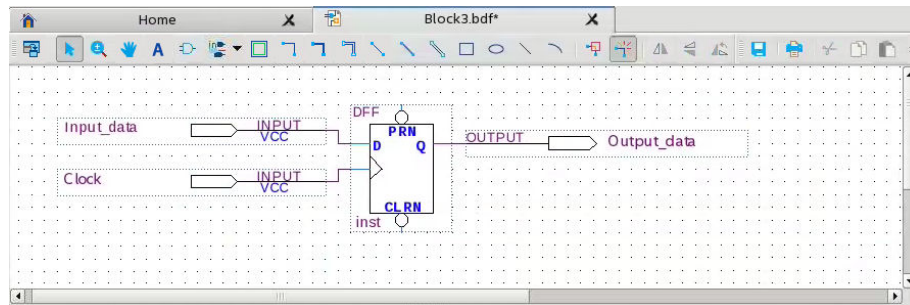
Figure 2. Symbol Button on Schematic Editor





- Under **Name**, type DFF, and click **OK**. Click in the Block Editor to insert a DFF symbol.
- Add input, clock, and output pins. Connect pins to the DFF.

Figure 3. DFF with Pin Connections



- Click **Processing > Start > Start Analysis and Synthesis**.

Related Information

[To Work with Block and Symbol Editor Toolbar Buttons](#)

1.3.2. Define I/O Standard and Pin Location

The specific pin location and I/O standard you assign impacts timing parameter values. Follow these steps to assign the constraints:

- Click **Assignments > Pin Planner**.
- Assign pin location and I/O standard constraints according to your design specifications.

Figure 4. Pin Locations and I/O Standards Assignments in Pin Planner

Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard	eserve	Current Strength	Slew Rate	>if
Clock	Input	PIN_AV16	3A	PIN_AV16	1.8 V		12mA (default)		
Input_data	Input	PIN_AN29	2F	PIN_AN29	1.8-V ..lass I		8mA (default)		
Output_data	Output	PIN_J14	3G	PIN_J14	1.8-V ..lass I		8mA (default)	1 (default)	
<<new node>>									

- To compile the design, click **Processing > Start Compilation**. The Compiler generates all timing information during processing.

Related Information

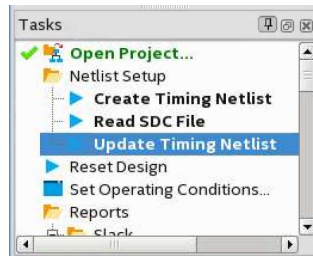
- [I/O Standards Definition](#)
- [Managing Device I/O Pins](#)

1.3.3. Update Timing Netlist and Set Operating Conditions

Follow these steps to update the timing netlist and set operating conditions following full compilation:

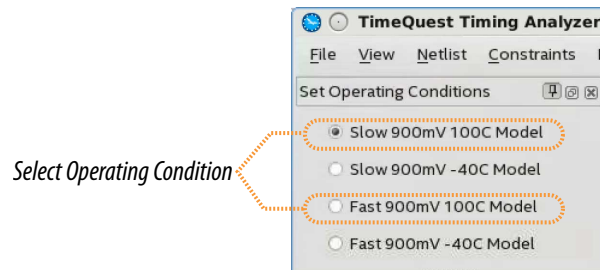
1. Click **Tools** ► **TimeQuest Timing Analyzer**.
2. In the **Task** pane, double-click **Update Timing Netlist**. The timing netlist updates with full compilation timing information that accounts for constraints.

Figure 5. Task Pane in TimeQuest Timing Analyzer



3. Under **Set Operating Conditions**, select either **Slow 900 mV 100C Model** or **Fast 900mV 100C Model**.

Figure 6. Set Operating Conditions in TimeQuest Timing Analyzer

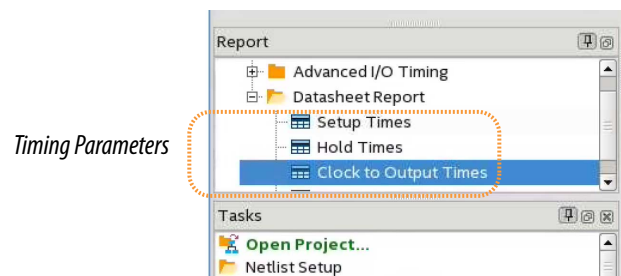


1.3.4. Determine I/O Timing Information from Datasheet Report

View the Compiler timing reports to determine the timing parameters.

1. Click **Report** ► **Datasheet** ► **Report Datasheet**.
2. Click **OK**.

Figure 7. Datasheet Report on TimeQuest Timing Analyzer



The Report pane displays the **Setup Times**, **Hold Times**, and **Clock to Output Times** reports.

3. Click each report to view the **Rise** and **Fall** parameter values.
4. For a conservative approach, select the maximum absolute value.



Example 1. Determining I/O Timing Parameters from Datasheet Report

In the following example **Setup Times** report, the fall time is greater than the Rise time, therefore $t_{su} = t_{fall}$.

Figure 8. Setup Time Report

Setup Times						
	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	Input_data	Clock	2.513	2.592	Rise	Clock

In the following example **Hold Times** report, the absolute value of the fall time is greater than the absolute value of the rise time, therefore $t_h = t_{fall}$.

Figure 9. Hold Time Report

Hold Times						
	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	Input_data	Clock	-1.428	1.482	Rise	Clock

In the following example **Clock to Output Time** report, the absolute value of the fall time is greater than the absolute value of the rise time, therefore $t_{co} = t_{fall}$.

Figure 10. Clock to Output Time Report

Clock to Output Times						
	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	Output_data	Clock	12.198	13.025	Rise	Clock

1.4. Scripting I/O Timing Information Generation

Alternatively, you can create and execute a tcl script to generate I/O timing information. This scripted approach generates tabular I/O timing parameter data for several I/O standards. Download example scripts for a selection of devices from the [Intel® FPGA Wiki page](#).

Note: This method is only available on Linux platforms.

Follow these steps to generate I/O Timing information for an Arria® 10 device reflecting multiple I/O standards:

1. In an internet browser, type `http://www.alterawiki.com/wiki/Device_I/O_Timing_Information_Generation` in the address field.
2. Click the **Arria 10 IO Timing Extraction Script** link, then click `A10_vversion.tgz` to download the file.
3. Extract the contents of the file in your computer. Example: `tar -zxvf A10_v1p2.tgz`. The `a10` folder appears.
4. Change directory to `a10`.



The a10 directory contains one or more subfolders with names corresponding to device types, such as a10_ax_r4_f40. This is the script for the Arria 10 GX device with 66 transceiver count, package type F40.

5. Change directory to a10/a10_ax_r4_f40/.
6. To run the script, type `quartus_sta -tR a10.tcl`.
Wait for completion. The script execution may take 8 hours or more, because each change on I/O standard or pin location requires design recompilation.

After the script completes, locate the `.csv` file in the current directory. This file contains I/O timing information for all supported I/O standards for the device. Open this file in a text editor to view the parameters.

Related Information

- [Command Line Scripting](#)
- `::quartus::sta`
Tcl package containing the set of functions for obtaining information from the TimeQuest Timing Analyzer.

1.5. Document Revision History

Table 2. Document Revision History

Date	Version	Changes
2016.10.31	16.1.0	Initial release of the document.