AN 754: MIPI D-PHY Solution with Passive Resistor Networks in Intel® Low-Cost FPGAs

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Introduction to MIPI D-PHY

The Mobile Industry Processor Interface (MIPI) is an industry consortium specifying high-speed serial interface solutions to interconnect between components inside a mobile device. The group specifies both protocols and physical layer standards for a variety of applications. The D-PHY is a popular MIPI physical layer standard for Camera Serial Interface (CSI-2) and Display Serial Interface (DSI) protocols. You can use the CSI-2 interface with D-PHY for the Camera (Imager) to Host interface, as a streaming video interface between devices, and in applications outside of mobile devices.

Overview on MIPI Operation

The D-PHY provides a synchronous connection between a master and slave. The minimum PHY configuration consists of a clock and one or more data signals. The D-PHY uses two wires per data lane and two wires for the clock lane. The lane can operate in a high-speed (HS) signaling mode for fast-data traffic and low-power (LP) signaling mode for control purpose.

The maximum data rate that can be supported in high-speed signaling is determined by the performance of the transmitter, receiver, and interconnect implementations. In practice, the typical implementation has a bit rate of approximately 500-800 Mbps per lane in high-speed mode for passive D-PHY. However, for some D-PHY applications, the bit rate can go up to 1.5 Gbps per lane. The maximum data rate in low-power mode is 10 Mbps.

The three possible implementations for connecting MIPI / D-PHY compliant device to Intel FPGAs are as follows:

- Use of an external D-PHY ASSP (for example Meticom MC2000x and MC2090x devices) as an active level shifter
- Use passive resistor network to create the compatible D-PHY with FPGA general-purpose I/O (GPIO)
- Use FPGA transceiver I/O to achieve higher data rate

This application note discusses the implementation using passive resistor network to achieve the lowest cost implementation.

The D-PHY can support bidirectional data transmission or unidirectional data transmission. CSI-2 protocol only requires unidirectional data transmission. Thus this implementation of a MIPI D-PHY compatible solution for Intel's low cost FPGAs only supports unidirectional data transmission.

- Receiving interface—FPGA I/O receives the high-speed or low-power signaling from a MIPI D-PHY transmitter (TX) device such as camera sensor or imager
- Transmitting interface—FPGA I/O transmits the high-speed or low-power signaling to a MIPI D-PHY receiver (RX) device such as a host or display

The high-speed differential signaling and low-power single-ended serial signals have different electrical characteristics. This application note covers the recommendation of the I/O standard for the FPGA I/O to emulate a MIPI D-PHY RX or TX, and provide an electrically compatibility between FPGA I/O and the MIPI interface. The single-ended mode uses LVCMOS or HSTL I/O standard for low-power mode, and differential I/O standard (LVDS) for high-speed mode. Resistors are used to connect, isolate, terminate, and level set to construct the compatible D-PHY.

Functional Description: FPGA Receiving Interface and FPGA Transmitting Interface

MIPI D-PHY IP incorporated in the FPGA is able to receive and transmit serial data which consists of one clock and one or more data lanes. The data lanes can switch between the high-speed and low-power signaling through a passive resistor network in unidirectional mode as shown in the following figures. This may be a spate IP block or integrated into the MIPI CSI-2 protocol controllers depending on the IP source or third-party IP partner. The lane control and interface logic are essential to the D-PHY functionality that needs to be built inside the FPGA logic.

Figure 1. FPGA Unidirectional Receiver Implementation Block Diagram

This figure shows high-speed and low-power modes in a single lane and common resistor configuration.

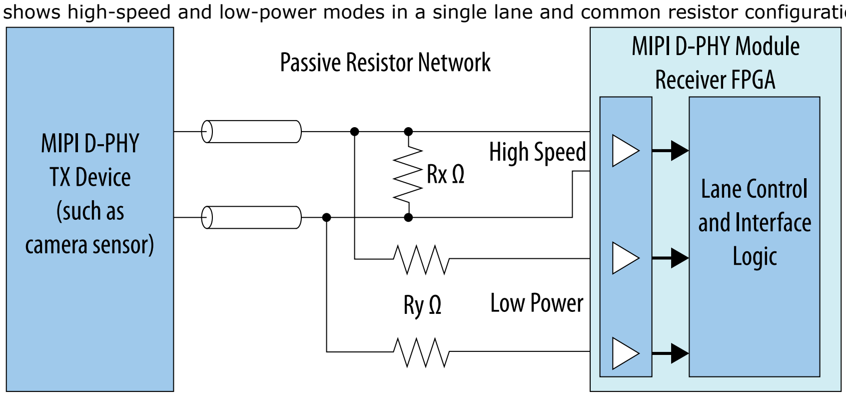
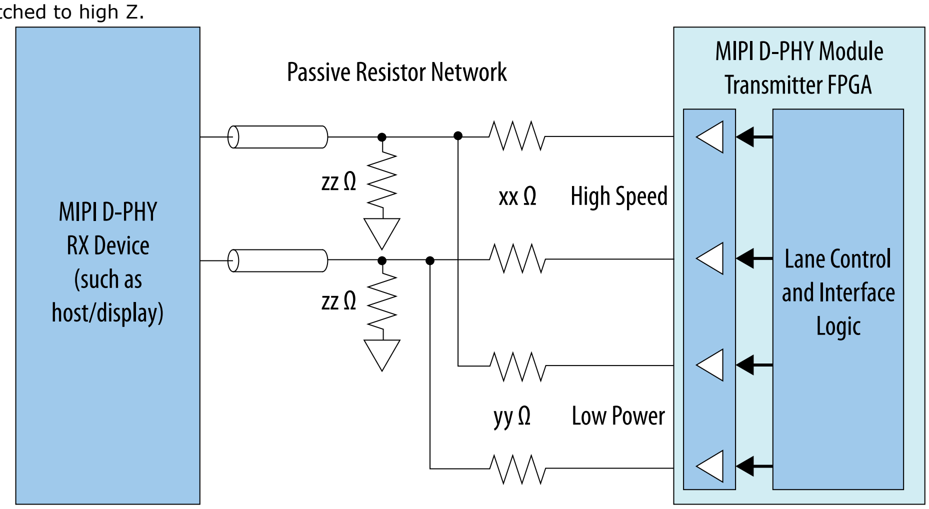


Figure 2. FPGA Unidirectional Transmitter Implementation Block Diagram

This figure shows high-speed and low-power modes in a single lane and common resistor configuration.

When the interface is in high-speed mode, the MIPI D-PHY RX device presents a 100 Ω differential termination. When the common-mode of the lines indicates that the interface is in low-power mode, the 100 Ω termination is switched to high Z.



Related Information

MIPI CSI-2 Controller Core
Provides more information about MIPI CSI-2 Controller Core

I/O Standards for MIPI D-PHY Implementation

Table 1. I/O Standards for MIPI D-PHY Implementation

This table lists the I/O standards supported for the FPGA I/O buffer for the MIPI D-PHY implementation in high-speed or low-power RX or TX mode. The recommendation has selected such that the following I/Os can co-exist in an I/O bank depending on the FPGA device.

- High-speed
- Low-power
- High-speed and low-power

Device	FPGA I/O Buffer Mode	Signaling Mode	I/O Standard	I/O Voltage Supply (V)	
				Input	Output
Cyclone® IV, Cyclone V, Intel® Cyclone 10 LP, Intel MAX® 10	RX	High-speed	LVDS (1)	2.5 (2)	—
		Low-power	HSTL-12 (1), 1.2 V LVCMOS	2.5 (2), 1.2	—
	TX	High-speed	Differential HSTL-18 (3)	—	1.8
		Low-power	1.8 V LVCMOS (3), 2.5 V LVCMOS	—	1.8, 2.5

MIPI D-PHY Specifications

MIPI D-PHY Specifications for Receiver

Table 2. High-Speed MIPI D-PHY Receiver DC Specifications

This table shows the MIPI D-PHY receiver high-speed signal DC specifications as stipulated in the MIPI D-PHY specifications from the MIPI Alliance.

Parameter	Description	Minimum	Typical	Maximum	Unit
$V_{CMRX(DC)}$	Common-mode voltage high-speed receive mode	70	—	330	mV
V_{IDTH}	Differential input high threshold	—	—	70	mV
V_{IDTL}	Differential input low threshold	–70	—	—	mV
V_{IHHS}	Single-ended input high voltage	—	—	460	mV
V_{ILHS}	Single-ended input low voltage	–40	—	—	mV
$V_{TERM-EN}$	Single-ended threshold for high-speed termination enable	—	—	450	mV
Z_{ID}	Differential input impedance	80	100	125	Ω

(1) The LVDS can co-exist in the same I/O bank as HSTL-12 when the FPGA is configured as input buffer in Cyclone V devices.

(2) Input buffer for LVDS and HSTL-12 I/O standards are powered by V_{CCPD} in Cyclone V devices.

(3) The Differential HSTL-18 can co-exist in the same I/O bank as 1.8 V LVCMOS when the FPGA is configured as output buffer in Cyclone IV, Cyclone V, Intel Cyclone 10 LP, and Intel MAX 10 devices.

Table 3. Low-Power MIPI D-PHY Receiver DC Specifications

This table shows the MIPI D-PHY receiver low-power signal DC specifications as stipulated in the MIPI D-PHY specifications from the MIPI Alliance.

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{IH}	Logic 1 input voltage	880	—	—	mV
V_{IL}	Logic 0 input voltage, not in ultra low power (ULP) state	—	—	550	mV

MIPI D-PHY Specifications for Transmitter

Table 4. High-Speed MIPI D-PHY Transmitter DC Specifications

This table shows the MIPI D-PHY transmitter high-speed signal DC specifications as stipulated in the MIPI D-PHY specifications from the MIPI Alliance.

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{CMTX}	High-speed transmit static common-mode voltage (4)	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0 (5)	—	—	5	mV
$\|V_{OD}\|$	High-speed transmit differential voltage (4)	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0 (5)	—	—	10	mV
V_{OHHS}	High-speed output high voltage (4)	—	—	360	mV
Z_{OS}	Single-ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch	—	—	10	%

Table 5. Low-Power MIPI D-PHY Transmitter DC Specifications

This table shows the MIPI D-PHY transmitter low-power signal DC specifications as stipulated in the MIPI D-PHY specifications from the MIPI Alliance.

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V
V_{OL}	Thevenin output low level	–50	—	50	mV

(4) When driving into load impedance within the Z_{ID} range.

(5) Recommended to minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ to minimize radiation and optimize signal integrity.

FPGA I/O Standard Specifications

FPGA I/O Standard Specifications for MIPI Receiver

The DC specifications for 1.2 V LVCMOS, HSTL-12, and LVDS I/O standards are as stipulated in the device datasheets for the respective devices. When an FPGA functions as a MIPI D-PHY receiver, the transmitted high-speed and low-power signals from the MIPI D-PHY transmitter are expected to meet these FPGA I/O standards specifications with passive resistor network.

Table 6. 1.2 V LVCMOS I/O Standard DC Specifications

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)	
	Min	Typ	Max	Min	Max	Min	Max
1.2 V	1.14	1.2	1.26	−0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3

Table 7. Single-Ended HSTL-12 I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V_{CCIO} (6)	0.50 × V_{CCIO} (6)	0.52 × V_{CCIO} (6)	—	0.50 × V_{CCIO}	—
				0.47 × V_{CCIO} (7)	0.50 × V_{CCIO} (7)	0.53 × V_{CCIO} (7)			

Table 8. Single-Ended HSTL-12 I/O Standard Signal Specifications

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)	
	Min	Max	Min	Max	Min	Max	Min	Max
HSTL-12 Class I, II	−0.15	V_{REF} − 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	−0.24	V_{REF} − 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24

Table 9. LVDS I/O Standard DC Specifications

I/O Standard	V_{CCIO} (V)			V_{ID} (V)		V_{ICM} (V)		
	Min	Typ	Max	Min	Max	Min	Condition	Max
LVDS	2.375	2.5	2.625	100	—	0.05	D_{MAX} ≤ 500 Mbps	1.8
						0.55	500 Mbps ≤ D_{MAX} ≤ 700 Mbps	1.8
						1.05	D_{MAX} > 700 Mbps	1.55

(6) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.

(7) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

FPGA I/O Standard Specifications for MIPI Transmitter

The DC specifications for Differential HSTL-18, 1.8 V LVCMOS, and 2.5 V LVCMOS I/O standards are as stipulated in the device datasheets for the respective devices. When an FPGA functions as a MIPI D-PHY transmitter, the transmitted high-speed and low-power signals from the FPGA I/O are expected to meet the high-speed and low-power MIPI D-PHY receiver specifications with passive resistor network.

Table 10. Differential HSTL-18, 1.8 V LVCMOS, and 2.5 V LVCMOS I/O Standards DC Specifications

I/O Standard	V_{CCIO} (V)			V_{OL} (V)	V_{OH} (V)
	Min	Typ	Max	Max	Min
HSTL-18[8] Class I, II	1.71	1.8	1.89	0.4	V_{CCIO} – 0.4
1.8 V LVCMOS	1.71	1.8	1.89	0.45	V_{CCIO} – 0.45
2.5 V LVCMOS	2.375	2.5	2.625	0.4	2

Related Information

MIPI D-PHY Specifications for Receiver on page 6

IBIS Simulation

IBIS simulation using HyperLynx is performed to show the link simulation between the MIPI D-PHY, transmission line, passive resistor network, and FPGA I/O for Cyclone IV, Cyclone V, Intel Cyclone 10 LP, and Intel Intel MAX 10 devices. The simulation demonstrates the following signaling modes with the passive resistor networks setups:

- Input and output differential and common-mode voltage levels for high-speed signaling
- Single-ended input and output high and low voltage levels for low-power signaling

During normal operation, either high-speed or low-power signaling can drive a lane. The states for high-speed lane are Differential-0 and Differential-1. The two single-ended lines in low-power lane states can drive a different or same state depending on the mode of operation. The low-power lane can drive four possible states: LP00, LP11, LP01 and LP10.

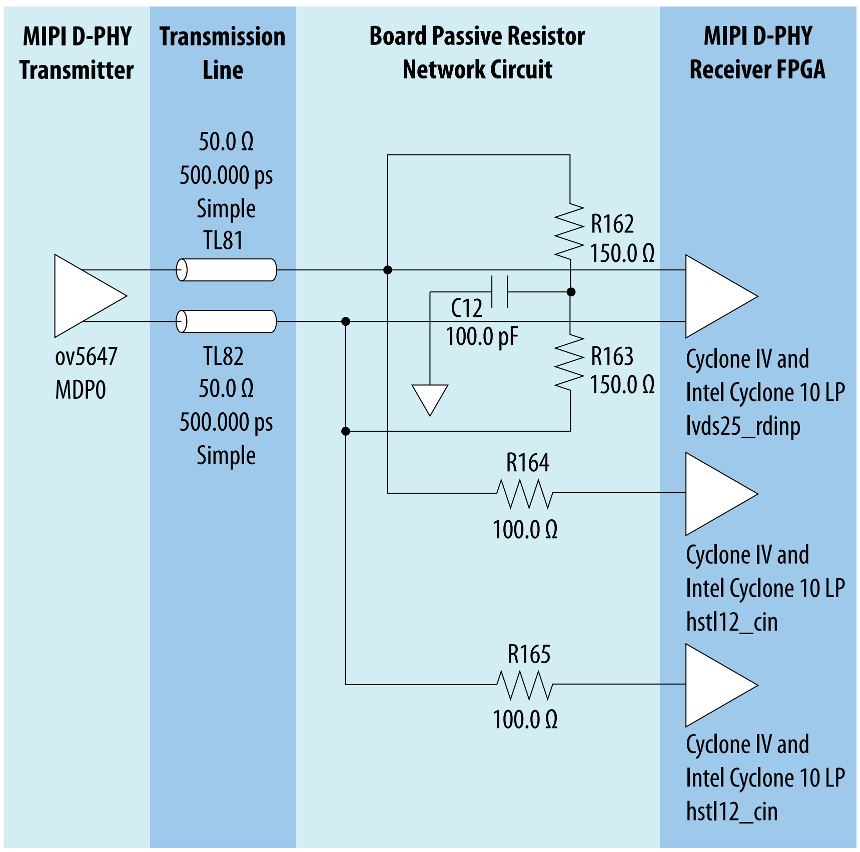
The high-speed mode is simulated at 840 Mbps for Cyclone IV, Cyclone V, and Intel Cyclone 10 LP devices, and 720 Mbps for Intel MAX 10 device. The low-power mode is simulated at 10 Mbps for Cyclone IV, Cyclone V, Intel Cyclone 10 LP, and Intel MAX 10 devices. The simulation uses simple transmission line that assumed to have the characteristics impedance of 50 Ω with 500 ps transmission delay.

[8] Differential HSTL-18 is a pseudo differential I/O standard consists of two single-ended HSTL-18 output buffers. One single-ended output buffer is the P channel and another single-ended output buffer is the N channel (inversion of P channel). The output differential signal (V_{OD}) is the difference of V_{OH}–V_{OL}. The output common mode voltage (V_{OCM}) is the signal crossing point for P and N channels.

FPGA As Receiver: HS-RX and LP-RX Modes Simulation

In the HS-RX and LP-RX mode simulation, the FPGA acts as a receiver to receive the MIPI D-PHY high-speed and low-power signals from MIPI D-PHY TX device in a single lane. The differential termination is fixed at 300 Ω across the LVDS pair in a single lane. The termination is set high to avoid the complexity of switching in and out of the high-speed mode termination. The termination supports the required signal quality at the targeted data rates although the termination does not match the characteristics impedance of the transmission line. The 300 Ω load between the lines minimizes loading in the low-power mode and in the LP01 or LP10 state. The two fixed series termination resistors are used for the low-power signals.

Figure 3. FPGA As Receiver HS-RX and LP-RX Modes IBIS Simulation Circuit



FPGA As Receiver: Simulation Results

The simulated waveforms for the Cyclone IV, Cyclone V, Intel Cyclone 10 LP, and Intel MAX 10 devices are based on the recommended setup. The I/O standards used in the FPGA I/O pins are compliant to the following voltage levels transmitted from the MIPI D-PHY TX device under typical conditions:

- High-speed signals—Output differential (V_{OD}) and common mode (V_{OCM}) voltage levels
- Low-power single-ended signals—Output voltage high (V_{OH}) and output voltage low(V_{OL}) signals

FPGA As Receiver: Simulation Results Using Cyclone IV and Intel Cyclone 10 LP Devices

Figure 4. HS-RX Mode Eye Diagram Measured At Cyclone IV and Intel Cyclone 10 LP FPGA Receiver Die At 840 Mbps

True (P) and Inverted (N) signals are plotted in purple and green. The P and N signals are overlapped. Differential signal (P-N) is plotted in yellow.

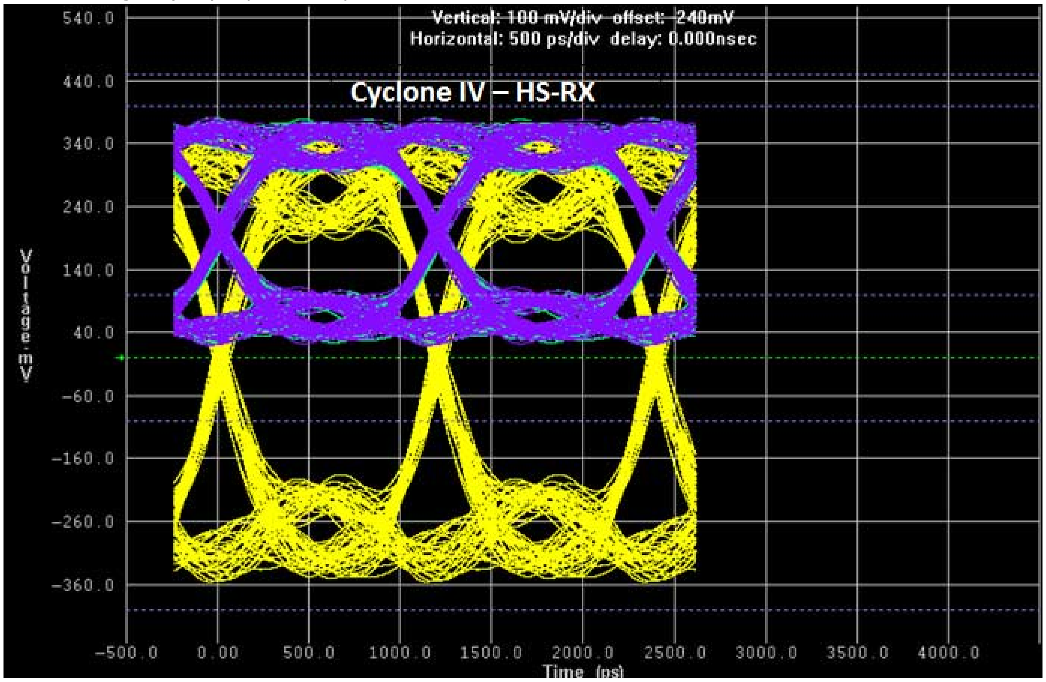


Figure 5. LP-RX Mode Waveform Measured At Cyclone IV and Intel Cyclone 10 LP FPGA Receiver Die for LP11 and LP00 States at 10 Mbps

DP signal is shown in blue and DN signal is shown in pink. The DN signal (pink) overlaps with the DP signal (blue) because both signals are driven on the same state (LP11, LP00).

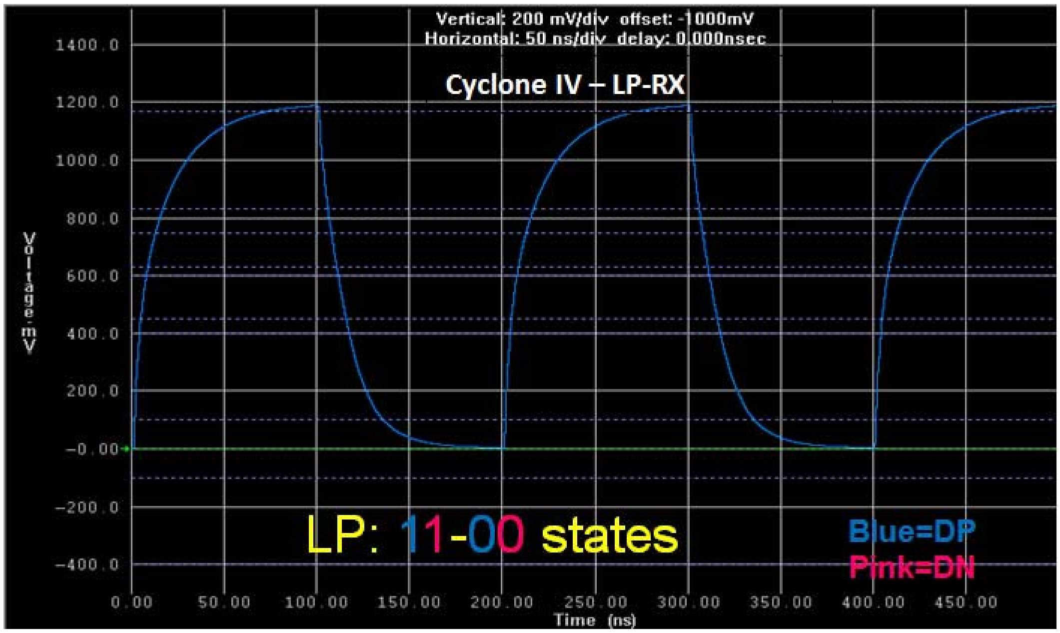
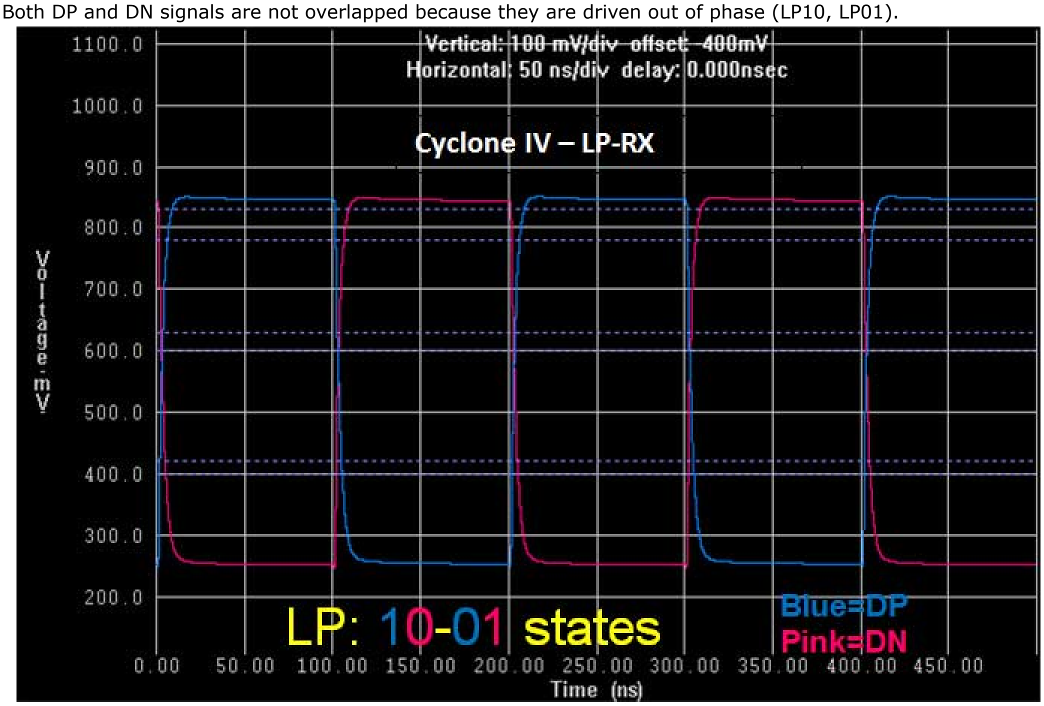


Figure 6. LP-RX Mode Waveform Measured At Cyclone IV and Intel Cyclone 10 LP FPGA Receiver Die for LP10 and LP01 States at 10 Mbps

Both DP and DN signals are not overlapped because they are driven out of phase (LP10, LP01).



FPGA As Receiver: Simulation Results Using Cyclone V Devices

Figure 7. HS-RX Mode Eye Diagram Measured At Cyclone V FPGA Receiver Die At 840 Mbps

True (P) and Inverted (N) signals are plotted in purple and green. The P and N signals are overlapped. Differential signal (P-N) is plotted in yellow.

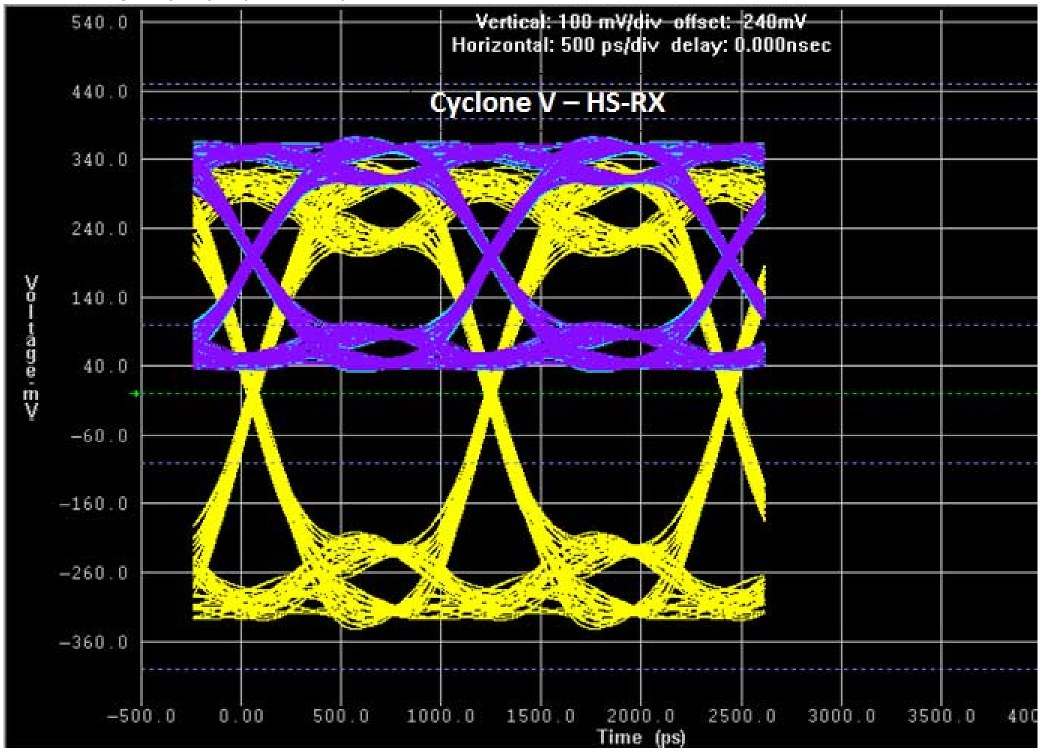


Figure 8. LP-RX Mode Waveform Measured At Cyclone V FPGA Receiver Die for LP11 and LP00 States at 10 Mbps

DP signal is shown in green and DN signal is shown in red. The DN signal (red) overlaps with the DP signal (green) because both signals are driven on the same state (LP11, LP00).

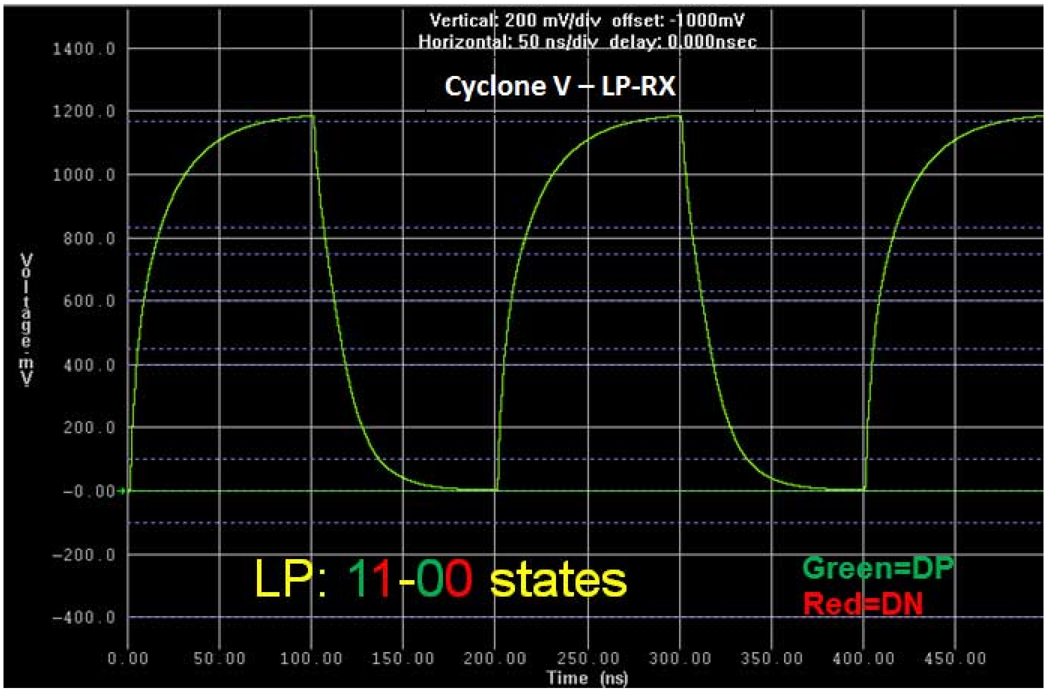
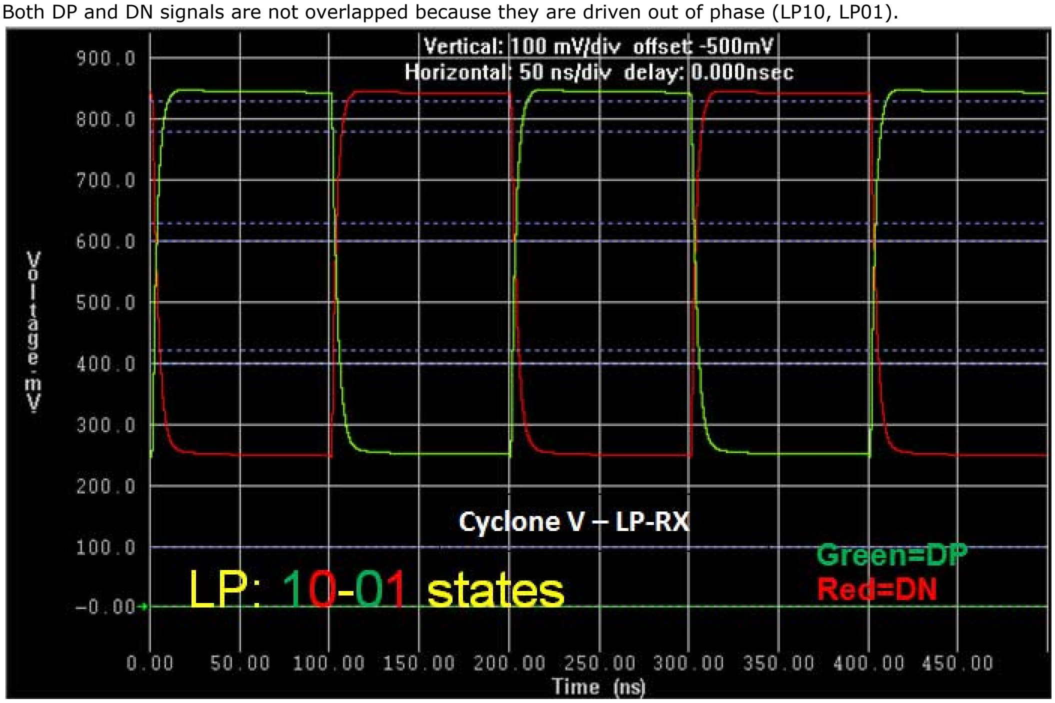


Figure 9. LP-RX Mode Waveform Measured At Cyclone V FPGA Receiver Die for LP10 and LP01 States at 10 Mbps

Both DP and DN signals are not overlapped because they are driven out of phase (LP10, LP01).



FPGA As Receiver: Simulation Results Using Intel MAX 10 Devices

Figure 10. HS-RX Mode Eye Diagram Measured At Intel MAX 10 FPGA Receiver Die At 720 Mbps

True (P) and Inverted (N) signals are plotted in yellow and pink. The P and N signals are overlapped. Differential signal (P-N) is plotted in blue.

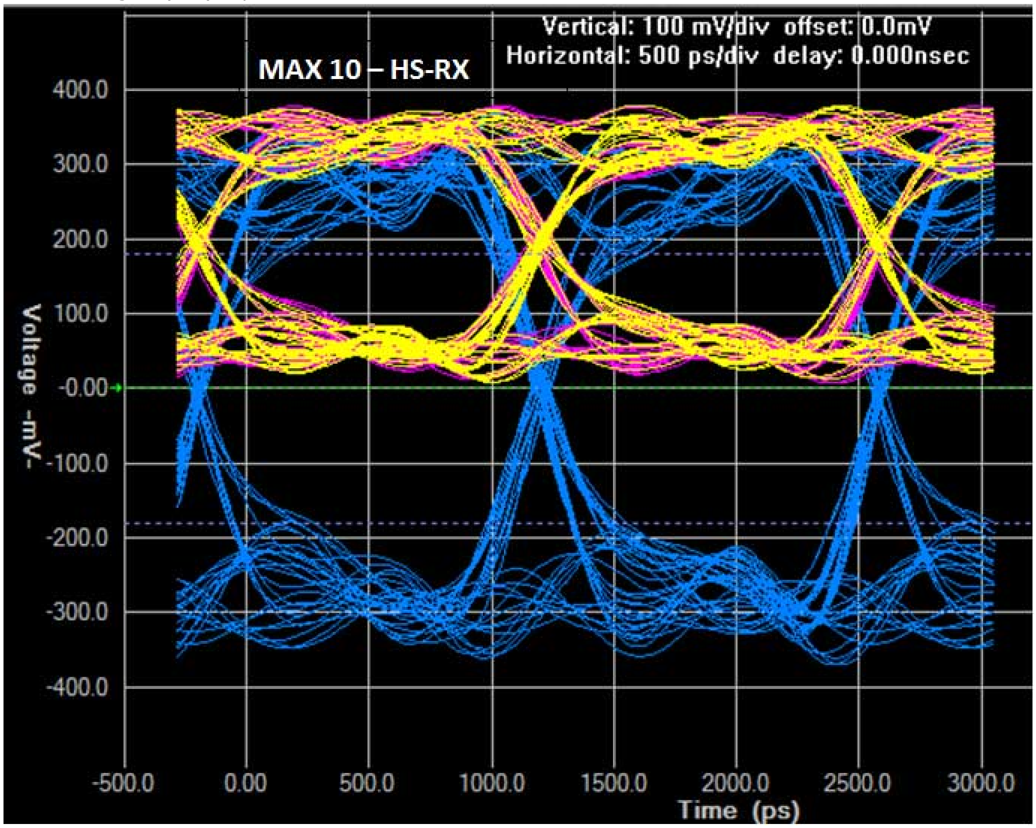


Figure 11. LP-RX Mode Waveform Measured At Intel MAX 10 FPGA Receiver Die for LP11 and LP00 States at 10 Mbps

DP signal is shown in blue and DN signal is shown in red. The DN signal (red) overlaps with the DP signal (blue) because both signals are driven on the same state (LP11, LP00).

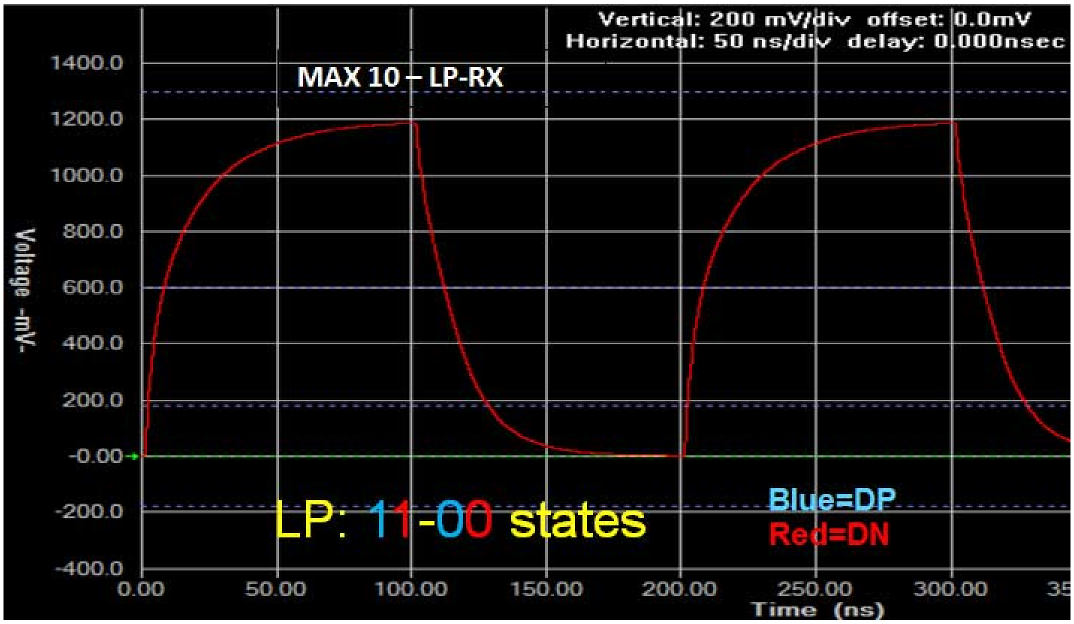
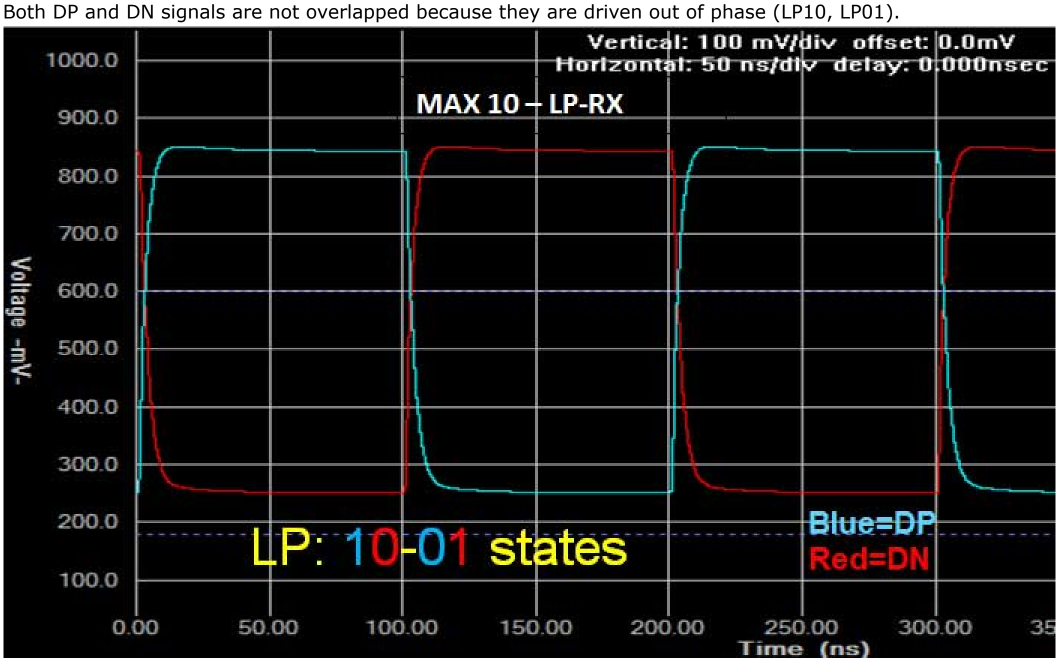


Figure 12. LP-RX Mode Waveform Measured At Intel MAX 10 FPGA Receiver Die for LP10 and LP01 States at 10 Mbps

Both DP and DN signals are not overlapped because they are driven out of phase (LP10, LP01).



FPGA As Transmitter: HS-TX and LP-TX Modes Simulation

In the HS-TX and LP-TX mode simulation, the FPGA acts as a MIPI D-PHY TX device. The MIPI D-PHY RX device is represented by the package parasitic components with a worst case capacitive load of 3.0 pF.

When the interface is in high-speed mode, the MIPI D-PHY RX device presents a 100 Ω differential termination in this simulation (as shown in the FPGA As Transmitter HS-TX Mode IBIS Simulation Circuit diagram). When the common-mode of the lines indicates that the interface is in low-power mode, the 100 Ω termination is switched to high Z, which is not shown in the LP-TX mode IBIS simulation circuit (as shown in the FPGA As Transmitter LP-TX Mode IBIS Simulation Circuit diagram). In this simulation, the MIPI D-PHY high-speed receiver is turned off during the low-power mode operation, thus the input differential termination is removed.

The IBIS simulation uses the buffers in different modes as follows:

- High-speed mode
  - A differential buffer is used to transmit signals.
  - Two single-ended buffers are configured as input mode to act as tri-stated outputs.
- Low-power mode
  - A differential buffer is configured as input mode to act as tri-stated output.
  - Two single-ended buffers are used to transmit signals.

Figure 13. FPGA As Transmitter HS-TX Mode IBIS Simulation Circuit

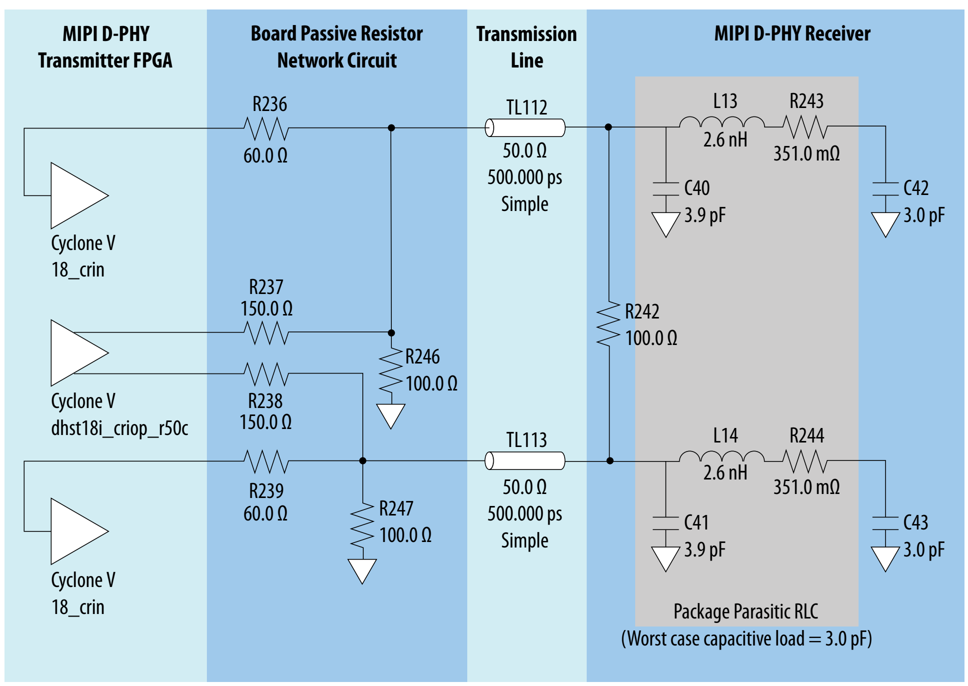
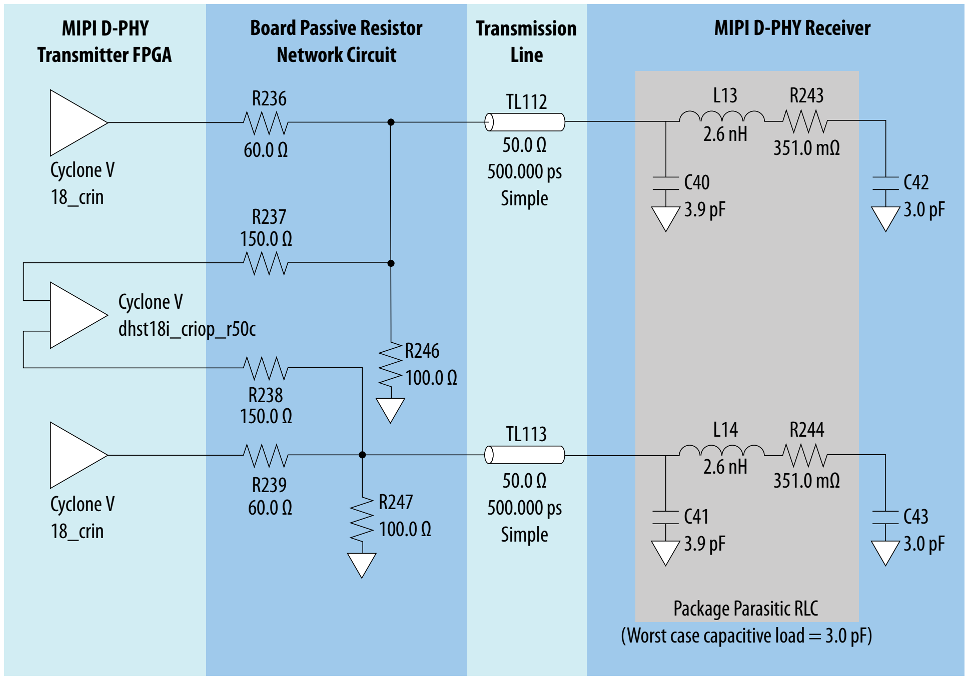


Figure 14. FPGA As Transmitter LP-TX Mode IBIS Simulation Circuit



FPGA As Transmitter: Simulation Results

The simulated waveforms for the Cyclone IV, Cyclone V, Intel Cyclone 10 LP, and Intel MAX 10 devices are based on the recommended setup.

The I/O standards used in the FPGA I/O pins are compliant to the following voltage levels as defined for high-speed or low-power MIPI D-PHY RX device under typical conditions:

- High-speed signals—Input differential (V_{ID}) and common mode (V_{ICM}) voltage levels
- Low-power single-ended signals—Input voltage high (V_{IH}) and input voltage low (V_{IL}) signals

The signal quality for high-speed signal is better with less jitter compared to the high-speed signal when FPGA acts as the receiving interface. The 100 Ω differential termination resistor at the load provides good impedance matching to the characteristic impedance of the transmission line.

FPGA As Transmitter: Simulation Results Using Cyclone IV and Intel Cyclone 10 LP Devices

Figure 15. Cyclone IV and Intel Cyclone 10 LP HS-TX Mode Eye Diagram Measured At MIPI D-PHY Receiver Die At 840 Mbps

True (P) and Inverted (N) signals are plotted in purple and blue. Differential signal (P-N) is plotted in green.

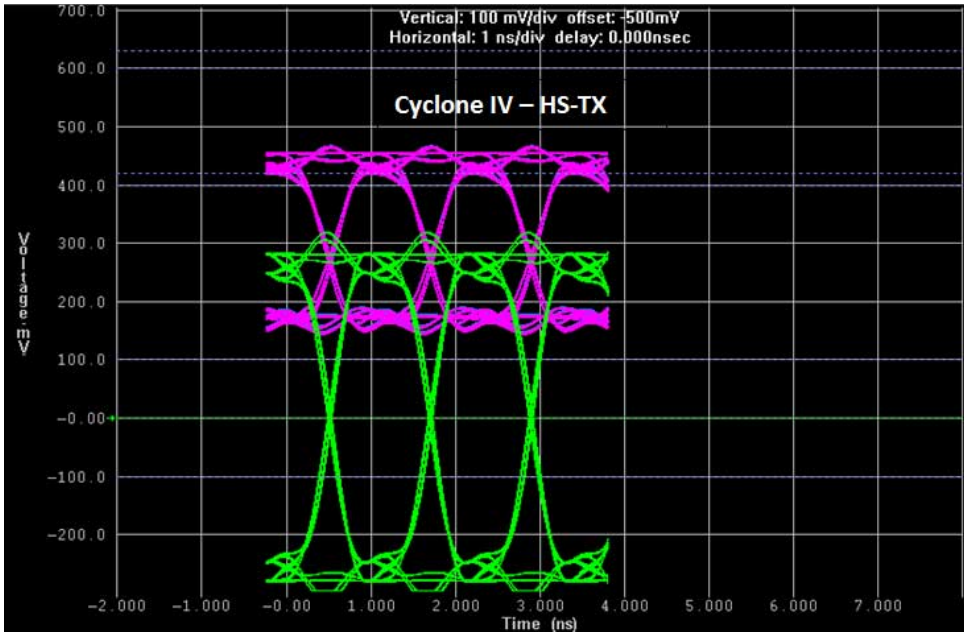


Figure 16. Cyclone IV and Intel Cyclone 10 LP LP-TX Mode Waveform Measured At MIPI D-PHY Receiver Die for LP11 and LP00 States at 10 Mbps

DP signal is shown in pink and DN signal is shown in yellow. The DN signal (yellow) overlaps with the DP signal (pink) because both signals are driven on the same state (LP11, LP00).

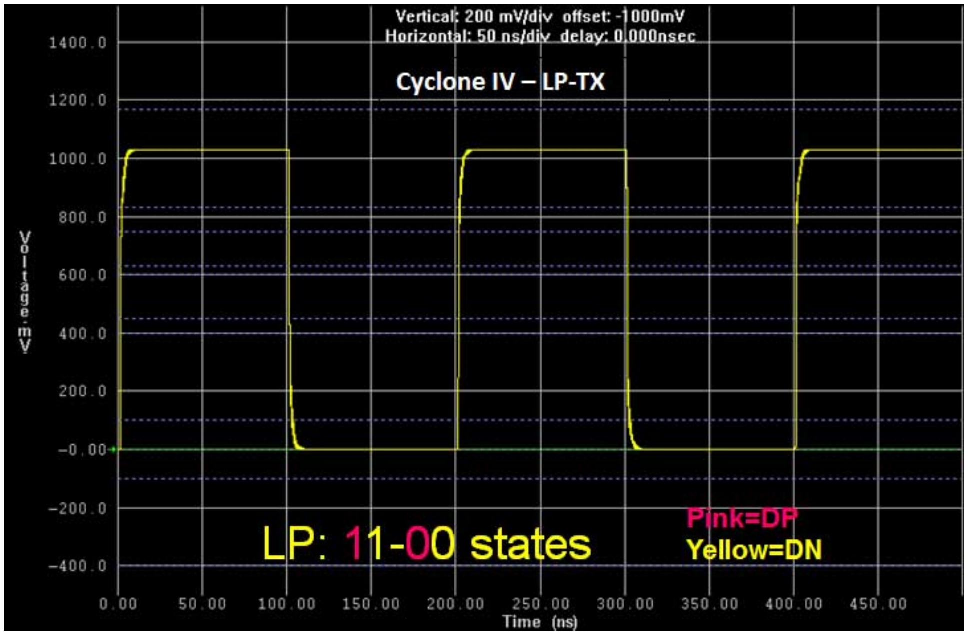
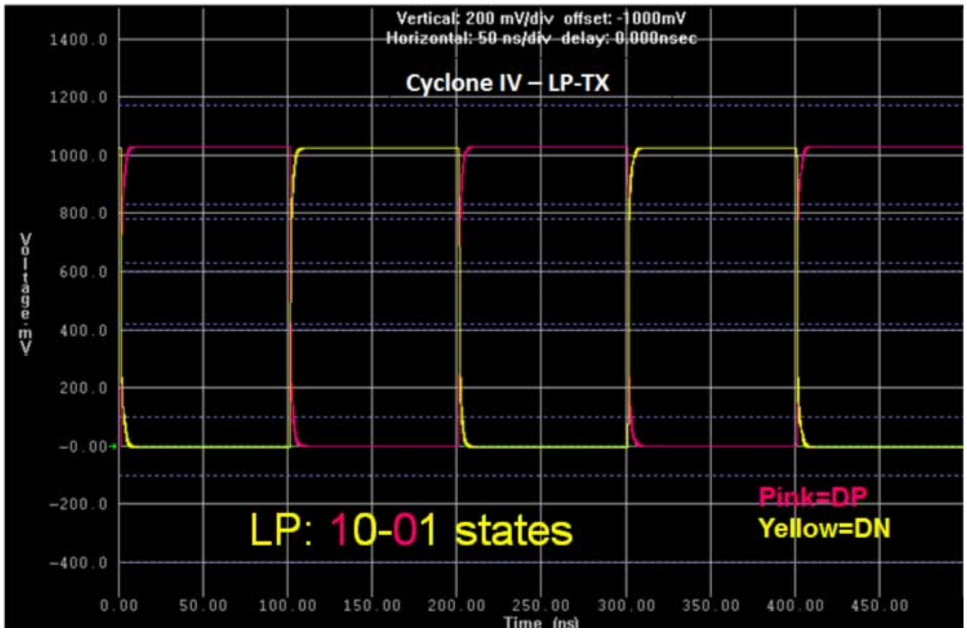


Figure 17. Cyclone IV and Intel Cyclone 10 LP LP-TX Mode Waveform Measured At MIPI D-PHY Receiver Die for LP10 and LP01 States at 10 Mbps

Both DP and DN signals are not overlapped because they are driven out of phase (LP10, LP01).



FPGA As Transmitter: Simulation Results Using Cyclone V Devices

Figure 18. Cyclone V HS-TX Mode Eye Diagram Measured At MIPI D-PHY Receiver Die At 840 Mbps

True (P) and Inverted (N) signals are plotted in green and orange. Differential signal (P-N) is plotted in red.

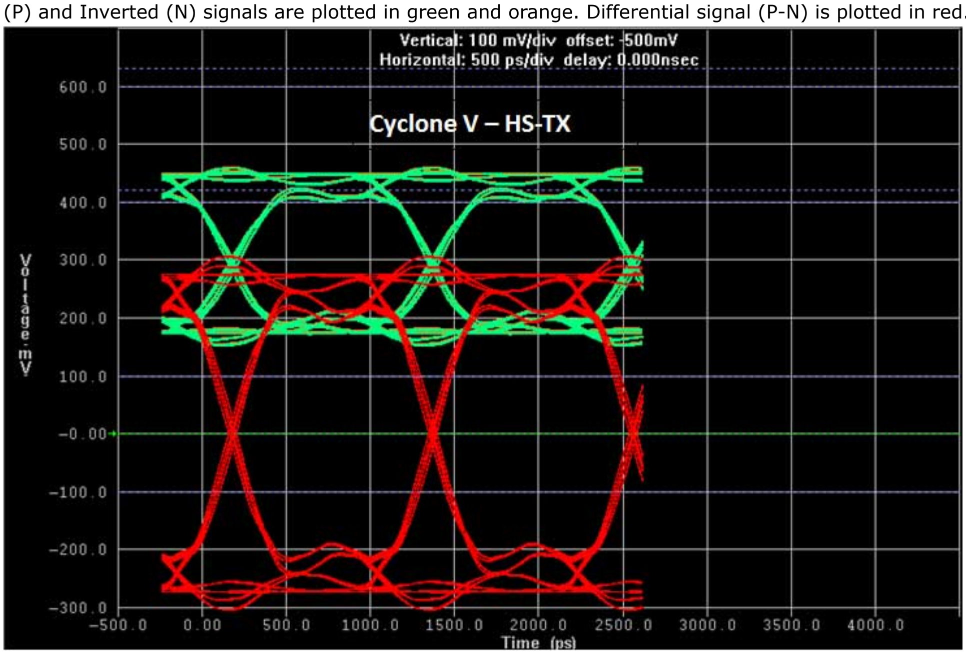


Figure 19. Cyclone V LP-TX Mode Waveform Measured At MIPI D-PHY Receiver Die for LP11 and LP00 States at 10 Mbps

DP signal is shown in yellow and DN signal is shown in blue. The DN signal (blue) overlaps with the DP signal (yellow) because both signals are driven on the same state (LP11, LP00).

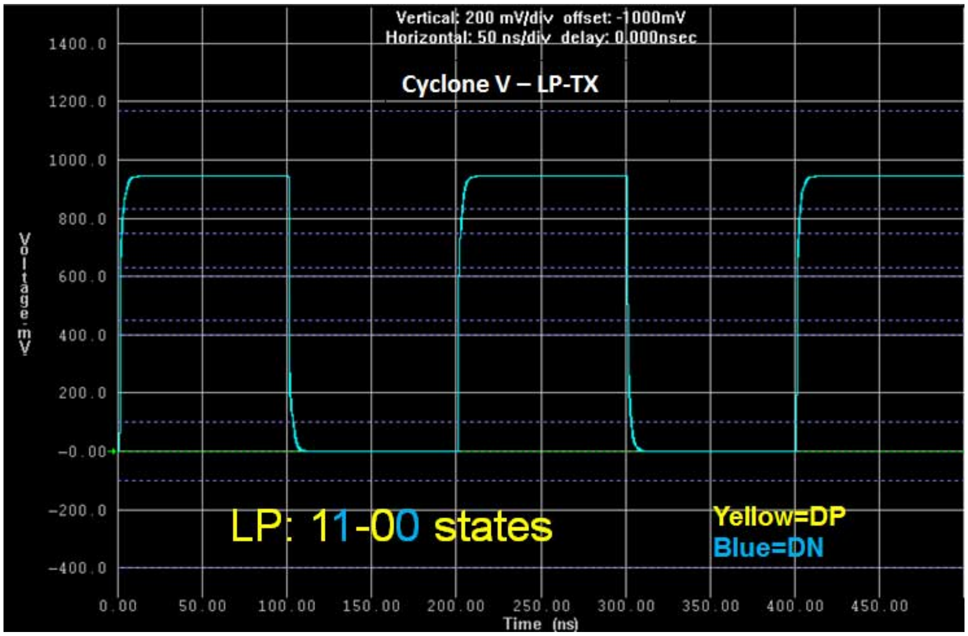
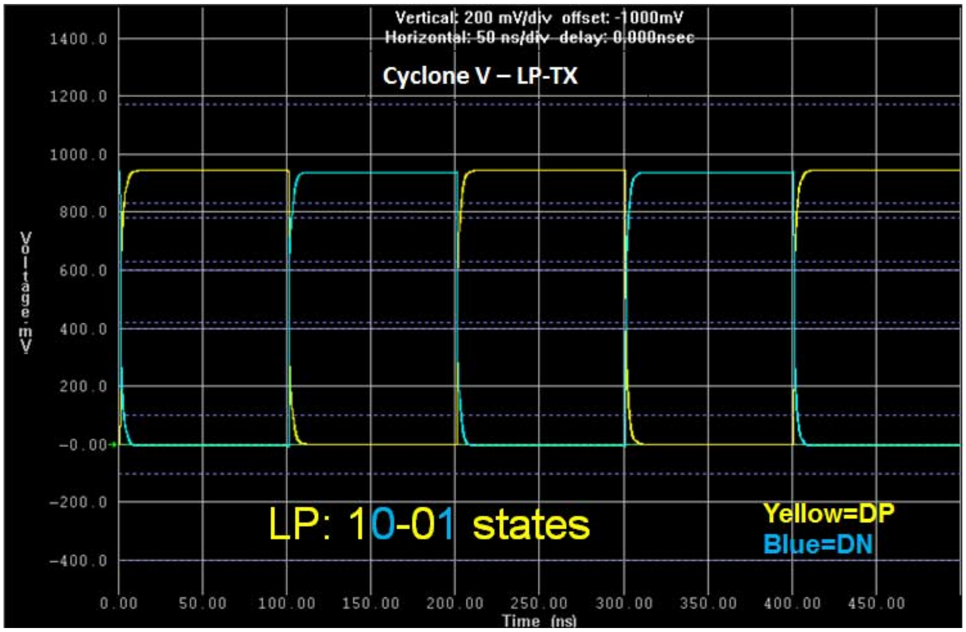


Figure 20. Cyclone V LP-TX Mode Waveform Measured At MIPI D-PHY Receiver Die for LP10 and LP01 States at 10 Mbps

Both DP and DN signals are not overlapped because they are driven out of phase (LP10, LP01).



FPGA As Transmitter: Simulation Results Using Intel MAX 10 Devices

Figure 21. Intel MAX 10 HS-TX Mode Eye Diagram Measured At MIPI D-PHY Receiver Die At 720 Mbps

True (P) and Inverted (N) signals are plotted in yellow and pink. Differential signal (P-N) is plotted in blue.

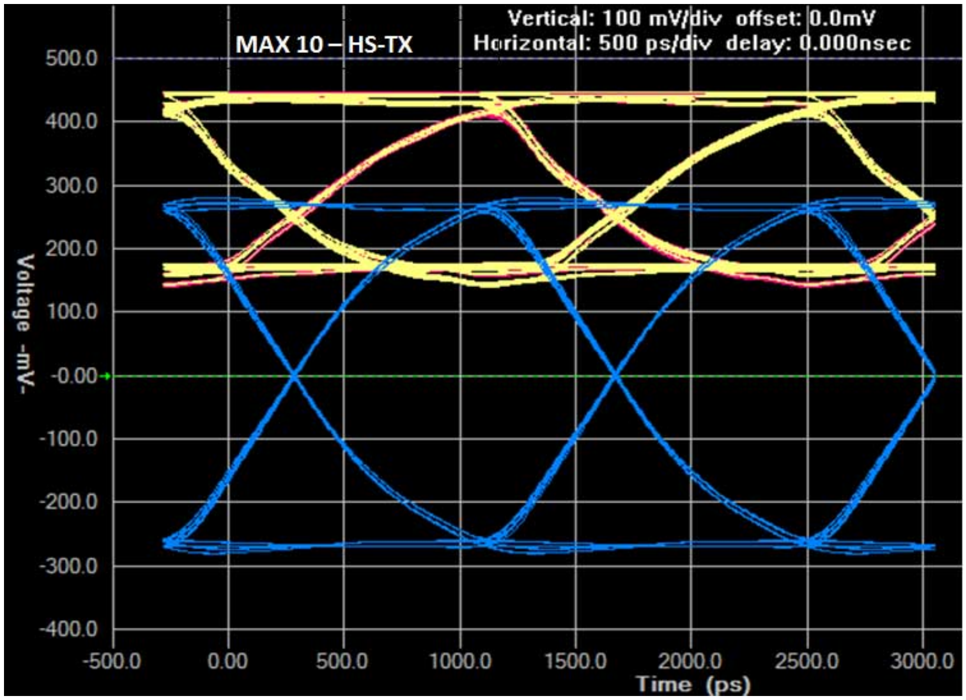


Figure 22. Intel MAX 10 LP-TX Mode Waveform Measured At MIPI D-PHY Receiver Die for LP11 and LP00 States at 10 Mbps

DP signal is shown in red and DN signal is shown in blue. The DN signal (blue) overlaps with the DP signal (red) because both signals are driven on the same state (LP11, LP00).

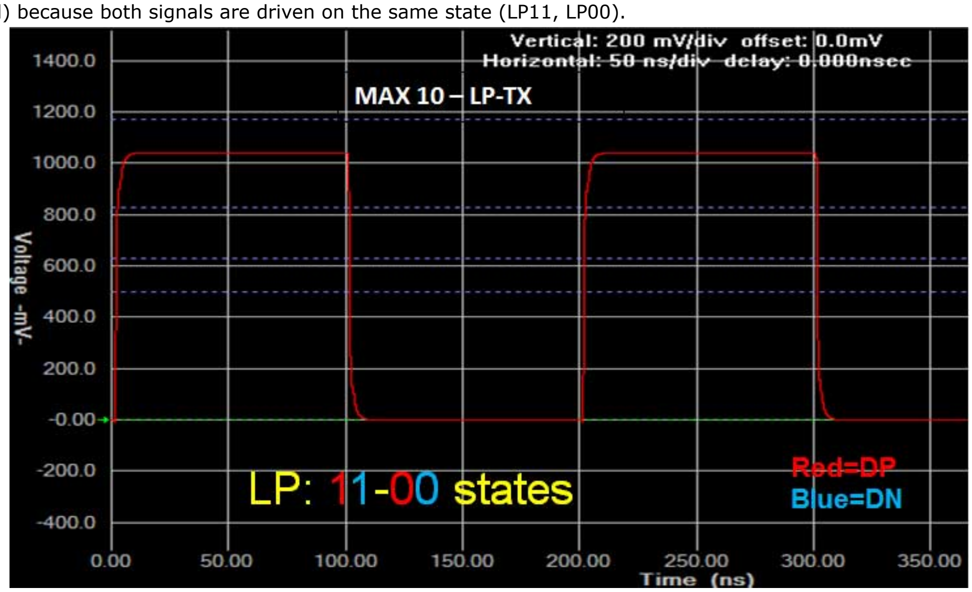
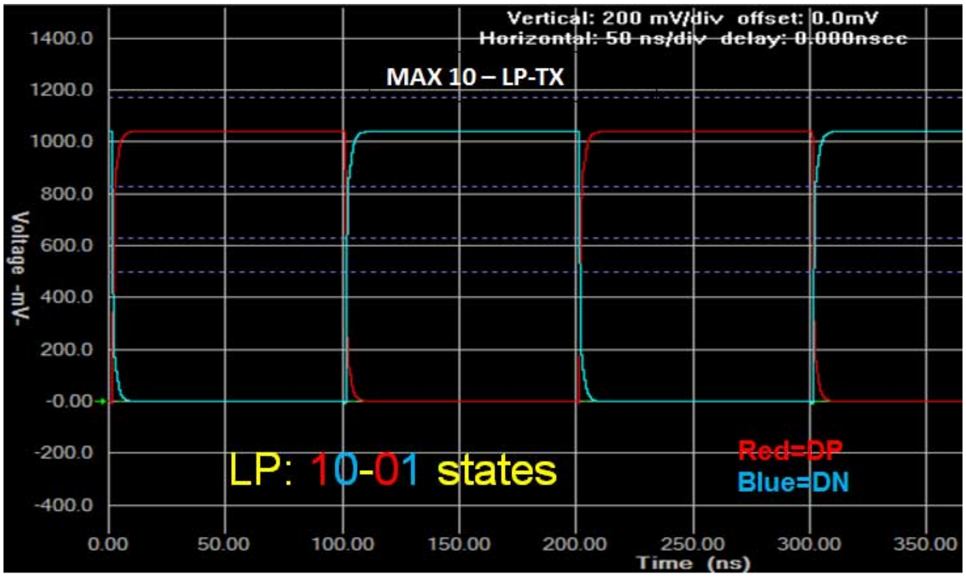


Figure 23. Intel MAX 10 LP-TX Mode Waveform Measured At MIPI D-PHY Receiver Die for LP10 and LP01 States at 10 Mbps

Both DP and DN signals are not overlapped because they are driven out of phase (LP10, LP01).



PCB Design Guidelines

The interconnect between the MIPI TX and RX devices must be designed with caution. The interconnect includes PCB traces, connectors (if any), and cable media (typically flex-foils).

Signal quality guidelines are as follows:

- Match the electrical length of all pairs as close as possible to maximize data valid margins.
- Place the passive components as close as possible to the FPGA. Avoid any stub when placing the passive resistors on the high-speed signal trace. Minimize the stub length from the low-power signal trace to high-speed signal trace.
- Use the on chip termination feature on FPGA I/O whenever possible.
- The reference characteristics impedance level per line is 100 Ω for differential and 50 Ω for single-ended. Control the impedance of the trace on the PCB to avoid impedance mismatch between the driver output impedance and input impedance of the receiver over the operating frequency.
- Keep the traces matched in lengths and as short as possible. The flight time for signals across the interconnect should not exceed 2 ns.
- Ensure equal length for all high-speed differential traces. The differential channel is also used for low-power single-ended signaling. Intel recommends applying only very loosely coupled differential transmission lines.

- If probe points are required, ensure they are in line with the trace and not creating a transmission line stub.
- Do not place noisy signals (example: voltage regulator module, clock generator) over or near MIPI signals.
- Use the I/O standards supported for the FPGA I/O as listed in the I/O standards for MIPI D-PHY Implementation table.

Related Information

- I/O Standards for MIPI D-PHY Implementation on page 6
- I/O Features in Cyclone IV Devices Chapter, Cyclone IV Device Handbook Volume 1
  Provides the I/O banks locations in Cyclone IV devices.
- I/O Features in Cyclone V Devices Chapter, Cyclone V Device Handbook Volume 1: Device Interfaces and Integration
  Provides the I/O banks locations in Cyclone V Devices. All the I/O banks in the Cyclone V devices can accommodate both the single-ended and differential I/Os, except the HPS row and column I/O banks.
- I/O and High Speed I/O in Intel Cyclone 10 LP Devices Chapter, Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook
  Provides the I/O banks locations in Intel Cyclone 10 LP devices.
- Intel MAX 10 I/O Banks Locations, Intel MAX 10 General Purpose I/O User Guide
  Provides the I/O banks locations in Intel MAX 10 devices.
- Support Resources: Board Design
  Provides more information about the general board design guidelines.
- IBIS Models for Intel Devices

Conclusion

The passive resistor network in this application illustrates and validates the IBIS simulations. You can use the passive resistor network to build a FPGA I/O based compatible MIPI D-PHY for receiving or transmitting both high-speed and low-power signals using various FPGA GPIO connected. The passive resistor network is capable to enable an electrically compatible connection between Intel FPGA I/O to a MIPI D-PHY TX or RX device via MIPI D-PHY interface.

Table 11. Passive Resistor Values Used in the IBIS Simulations

Refer to the FPGA Unidirectional Receiver Implementation Block Diagram and FPGA Unidirectional Transmitter Implementation Block Diagram for the simulation block diagrams.

FPGA Implementation	Passive Resistor Value (Ω)				
	R_x	R_y	xx	yy	zz
FPGA unidirectional receiver implementation	300	100	—	—	—
FPGA unidirectional transmitter implementation	—	—	150	60	100

Table 12. Maximum Achievable Data Rate Using Intel FPGA GPIO

The maximum achievable data rate depends on the device speed grade.

Device	Supported Data Rate (Mbps)
Cyclone IV, Cyclone V, Intel Cyclone 10 LP	840
Intel MAX 10	720

Intel recommends performing HSPICE/IBIS simulations to verify the signal quality based on your specific system setup and PCB info at the desired operating frequency.

Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulation based on your specific design, system setup, and PCB info to determine the maximum achievable frequency.

The MIPI D-PHY passive solution with different approaches (I/O, passive network, and FPGA devices) are validated using multiple demo boards. You can use the following demo boards as reference:

- Intel 10M50 Evaluation Kit, EK-10M50F484 (available March 2016 onwards)
- Internal HSMC Passive D-PHY lab validation board for use with Cyclone V Development Kits
- Arrow DECA Intel MAX 10 Evaluation Kit

For more information about the demo boards, contact your local Intel sales representatives.

Related Information

I/O Standards for MIPI D-PHY Implementation on page 6

Document Revision History for AN 754: MIPI D-PHY Solution with Passive Resistor Networks in Intel Low-Cost FPGAs

Document Version	Changes
2018.06.15	• Changed Cyclone IV GX to Cyclone IV in the *I/O Standards for MIPI D-PHY Implementation* table. • Removed the note about MIPI D-PHY solution that can also use others I/O standards that are powered with different V_{CCIO} in the *Conclusion* section. • Added support for Intel Cyclone 10 LP devices.

Date	Version	Changes
November 2017	2017.11.20	Updated links.
May 2017	2017.05.08	Rebranded as Intel.
December 2015	2015.12.23	Initial release.