



# AN 711: Power Reduction Features in Intel<sup>®</sup> Arria<sup>®</sup> 10 Devices



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## AN 711: Power Reduction Features in Intel® Arria® 10 Devices

The Intel® Arria® 10 family features the most sophisticated power reduction capabilities of any FPGA available.

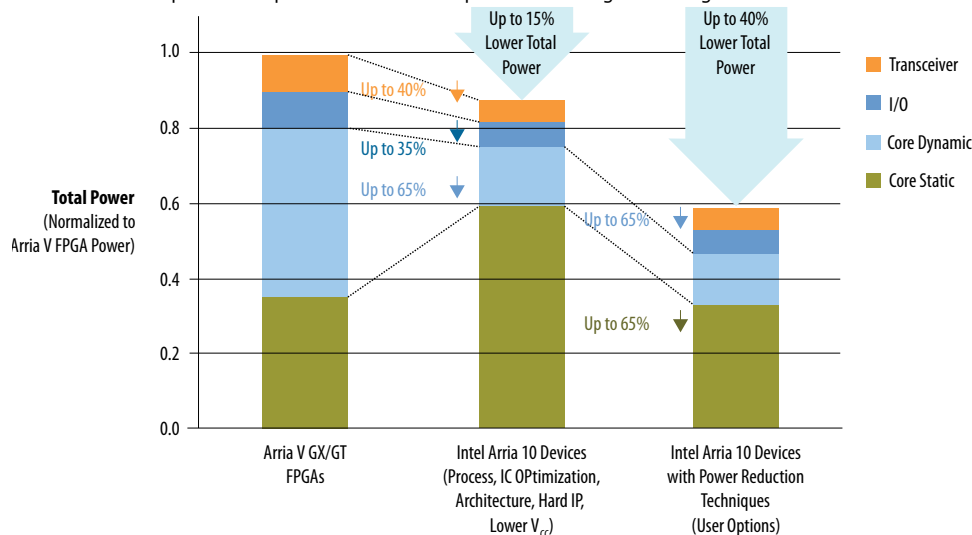
The Intel Arria 10 family is designed to provide higher performance than the fastest FPGAs of the prior generation, and offers significant power advantages. Additionally, Smart Voltage ID (SmartVID) allows further reduction in both static and dynamic power consumption.

### Power Reduction and Performance

The Intel Arria 10 family operates at higher performance levels than prior generation 28-nm FPGAs. With 20-nm design rules, you can achieve significant power savings compared to 28-nm FPGAs. You can achieve even more power savings by applying additional power reduction techniques on the core voltage.

**Figure 1. Power Consumption Comparison**

Potential reduction in power compared to the lowest-power mid-range 28-nm generation FPGAs.



Smaller geometries and changes to the basic architecture provide the initial power savings of up to 15% over prior generation Arria V devices. Any static power increases are offset by reductions in dynamic power for an overall total power reduction. You can achieve up to 40% additional power savings through static power binning, and by controlling the core voltage. You can control the core voltage through SmartVID.

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## Intel Arria 10 Power Reduction Techniques

Intel Arria 10 devices implement several power reduction techniques.

**Table 1. Strategies for Reducing Power Consumption**

Power Reduction Technique	Description
Low Static Power Device Grades	Provides flexibility to Intel devices that have been tested for static power. These devices have the -L suffix.
Programmable Power Technology	Enables lower power transistors for non-performance-critical paths to reduce static power. This is achieved during compilation of the FPGA design in Intel Quartus® Prime.
SmartVID	Enables the device to run at lower than default $V_{CC}$ while retaining the same performance level, reducing static and dynamic power. This requires devices screened for proper operation. These devices have the -V suffix.

### SmartVID

During manufacturing testing, Intel determines the optimum operating conditions for the core performance. A set of voltage values corresponding to those conditions are then programmed into nonvolatile registers in the device. The contents of these registers, and information about the silicon temperature, control the output of the voltage regulators, minimizing power consumption.

SmartVID has a large number of very small voltage reduction steps. Using SmartVID, the Intel Arria 10 device operates at the lowest possible voltage for a given speed grade. This enables power savings without sacrificing performance. SmartVID is offered as device-specific features. If you want to use either of these features, ensure that you order the correct product corresponding to the feature. For more information, refer to the "Intel Arria 10 Device Variants and Packages" section of the *Intel Arria 10 Device Overview*.

Intel Arria 10 SmartVID devices power up at default voltage (0.9 V). After the power-up sequence and device configuration, lower voltage is applied. This reduces  $V_{CC}$  SmartVID voltage to a value between 0.9 V and 0.85 V. When the junction temperature of the device is below 0° C, the voltage is increased to the original value.

#### Related Information

[Intel Arria 10 Device Overview](#)

### SmartVID General Configuration

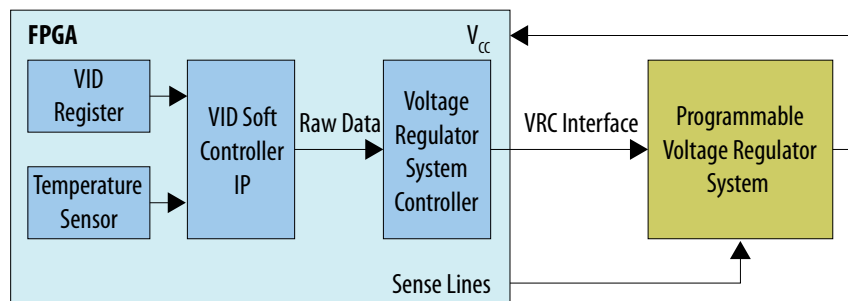
The system is comprised of four main sections.



**Table 2. SmartVID Blocks and Descriptions**

Section	Description
VID Register	Provides status input for the SmartVID Controller IP.
Temperature Sensor	
VID Soft Controller	One component of the SmartVID Controller IP that provides data to the voltage regulator controller.
Voltage Regulator System Controller	Voltage regulator is a generic term to designate any sort of voltage conversion system: DC-to-DC converters, switching regulators, and linear regulators. The system controller requests an external programmable voltage regulator system to provide the correct voltage to the $V_{CC}$ input of the FPGA. This helps to limit power consumption. The controller can have several different topologies, which are explained below.

**Figure 2. General Configuration for the SmartVID Controller IP**



## System Topology Options

The VID register, temperature sensor, and VID soft controller are unchangeable. Intel provides the VID soft controller as a SmartVID Controller IP to customers. The remainder of the system may have many different solutions.

The voltage regulator controller interface can be implemented as:

- A parallel output to drive a digitally adjustable voltage regulator directly
- A multi-wire serial interface such as I2C, SMBus\*, PMBus\*, or similar interface hereafter referred to as PMBus
- A one-wire pulse width modulated (PWM) output to be used with a circuit to adjust the output of an adjustable voltage regulator

Intel provides reference designs for some of these functions. Contact your sales representative to find out what is available at this time.

**Table 3. Reference Design Availability Schedule**

Voltage Regulator Controller	Availability <sup>(1)</sup>
Parallel	Intel Quartus Prime software version 15.0
PMBus	Intel Quartus Prime software version 15.1
Single-wire interface (one-wire PWM)	Intel Quartus Prime software version 16.0

(1) These software releases are available on [www.altera.com](http://www.altera.com).



The Voltage Regulator System can be implemented as:

- A parallel input digital voltage converter, such as the EC7401QI PWM controller from Intel Enpirion® portfolio.
- A multi-wire serial voltage converter that supports the PMBus standard such as the Intel Enpirion Digital PowerSoC family. Example solutions include the EM2260, EM2140, EM2130, and EM2120.
- An adjustable voltage regulator with an analog circuit that converts the PWM signal to some means that controls the regulator output, allowing the use of standard analog voltage regulator controllers.

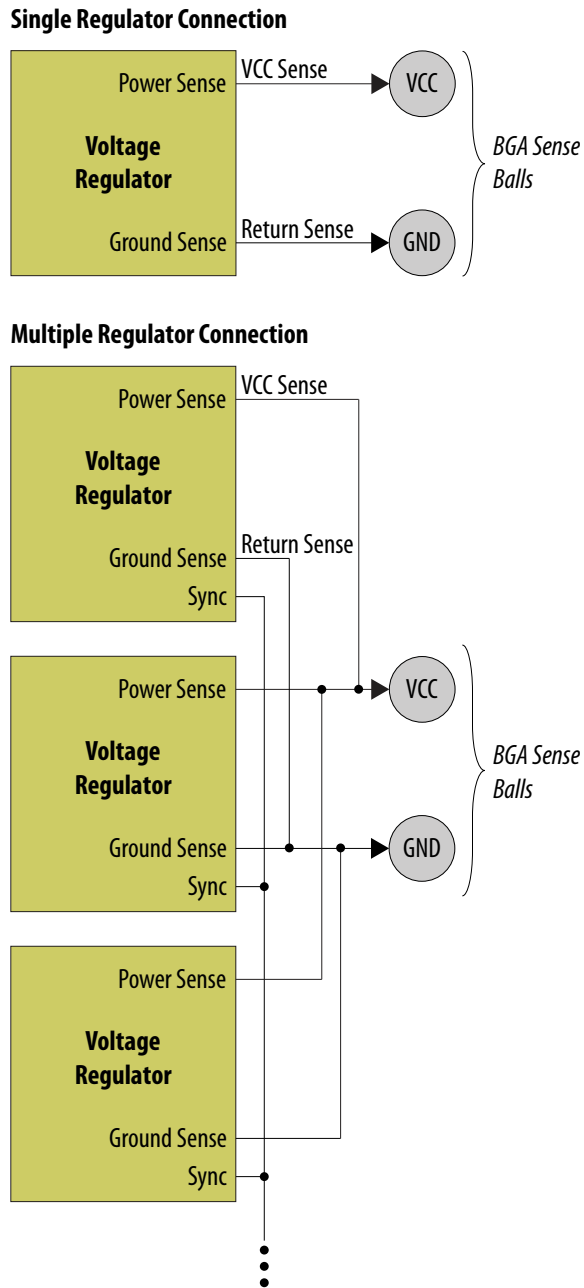
## Power Sense Lines

Sense lines from the die power rail to the ball accurately account for the voltage drop in the package at high currents. The power supply uses the sense lines as the feedback reference to avoid having the wrong voltage level under load. You must use the power sense lines in this fashion when using the SmartVID features.

The power sense lines are dedicated pins on the FPGA. Refer to the *Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines* for details.



Figure 3. Power Sense Lines with Single and Multiple Regulator Configurations



**Related Information**

*Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines*



## SmartVID Topologies

All SmartVID systems start with the SmartVID soft controller. This controller reads data from a fuse register containing data obtained during production tests. This data is used with the temperature reading for the FPGA to create a value for the optimal voltage level.

## SmartVID Controller IP Core

**Note:** To avoid problems during board bring-up and testing, do not read the fuse register during any reset sequence of the SmartVID soft controller. Doing so interrupts the normal operation of the JTAG chain of the device.

The `vidctl_vid_code` port is the VID output code, which represents the 6-bit VID code. This value is also stored in the control and status register (CSR) and can be accessed via the Avalon® Memory-Mapped interface.

When interfacing between the IP and your system, you should read the output when `vidctl_vid_code_avail` is asserted. This means that a new valid VID code is ready to be read. After the VID code is read, assert `vidctl_vid_ack` to let the SmartVID Controller IP Core know that the VID code is taken and a new value can be computed.

The first VID code output will be the default value, which is 0.9 V. How often the value will change depends on the temperature. If the temperature change causes the value to be updated, the VID code reduces to the targeted VID value with the decrement of `VID_STEP` per update. Likewise, it increases from the targeted VID value to 0.9 V with the increment of `VID_STEP` per update. VID code is only updated after you acknowledge that the current value is being read by asserting the `vidctl_vid_ack` input port.

For the SmartVID supported voltage range, refer to the *Intel Arria 10 Device Datasheet*.

There are many other ports on the SmartVID controller that need to be connected and used to configure the core. Please refer to the *SmartVID Controller IP Core User Guide* for more details.

### Related Information

- [SmartVID Controller IP Core User Guide](#)
- [Intel Arria 10 Device Datasheet](#)

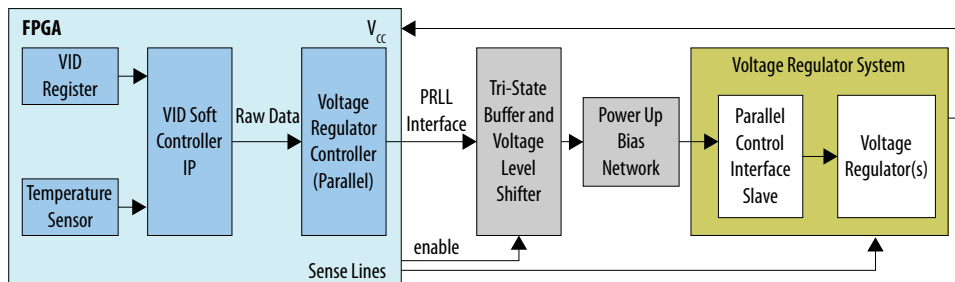
## Parallel Control System

**Note:** Currently, the parallel control system is being implemented on some Intel FPGA development boards. Contact your sales and service representative for availability.





Figure 4. Parallel Control System



The parallel output configuration uses an on-FPGA VID soft controller and parallel voltage regulator controller system. Together they create a value necessary to drive the correct data to the voltage regulator. The regulator decodes the parallel data and adjusts the voltage level to the FPGA. At power up, the bias network, which consists of weak pull-up and pull-down resistors, establishes the code for the default  $V_{CC}$  voltage for the FPGA. When the SmartVID Controller IP takes control and is done with initializations, it outputs the voltage code. It then enables the tri-state buffer, taking control of the  $V_{CC}$  level. Intel recommends that the enable signal originate from a specific pin (RZQ\_2A) on the FPGA. Refer to the *Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines* for more information about pin assignments.

**Related Information**

*Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines*

**Intel Quartus Prime Parallel Control System Instantiation**

Intel will provide a reference design for a parallel control system with the release of the Intel Arria 10 PCIe\* development kit. Contact your sales representative about the availability of intellectual property for this interface.

Figure 5. Parallel Interface Example Diagram

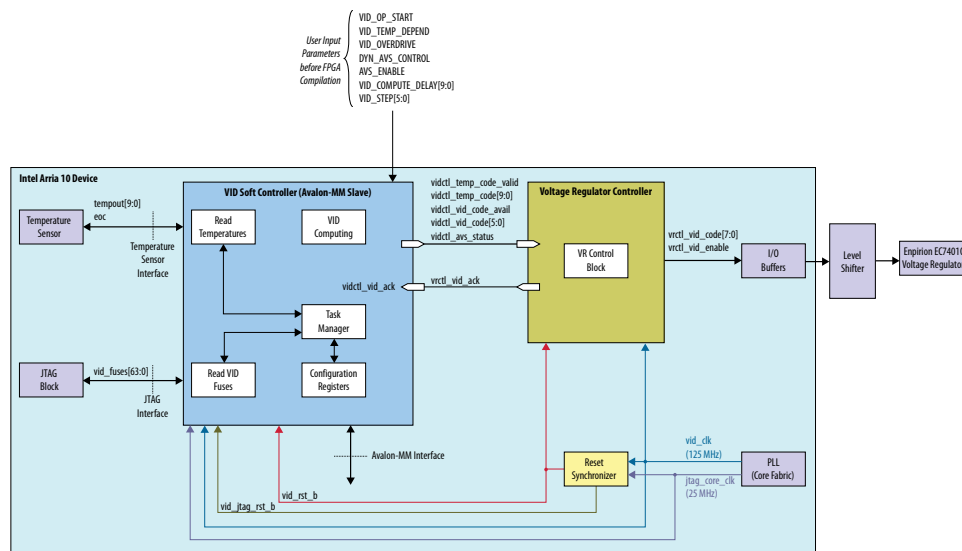
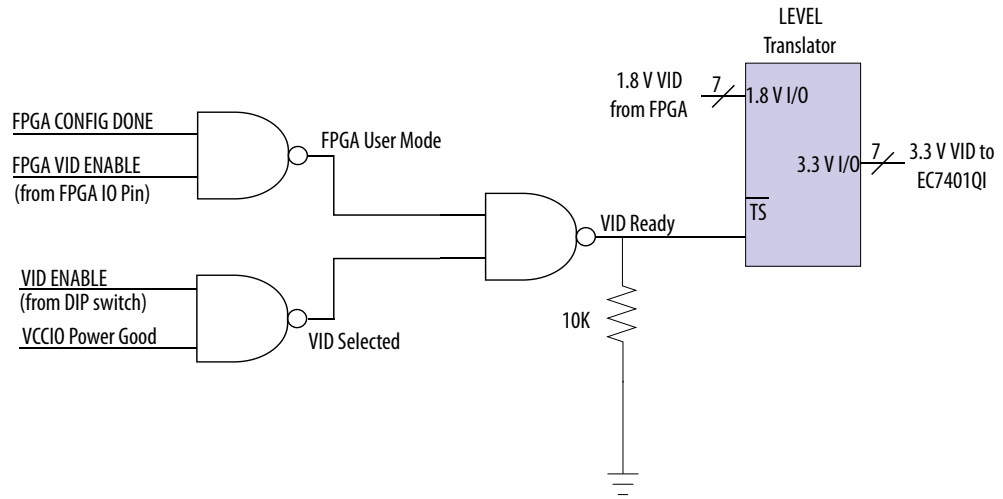


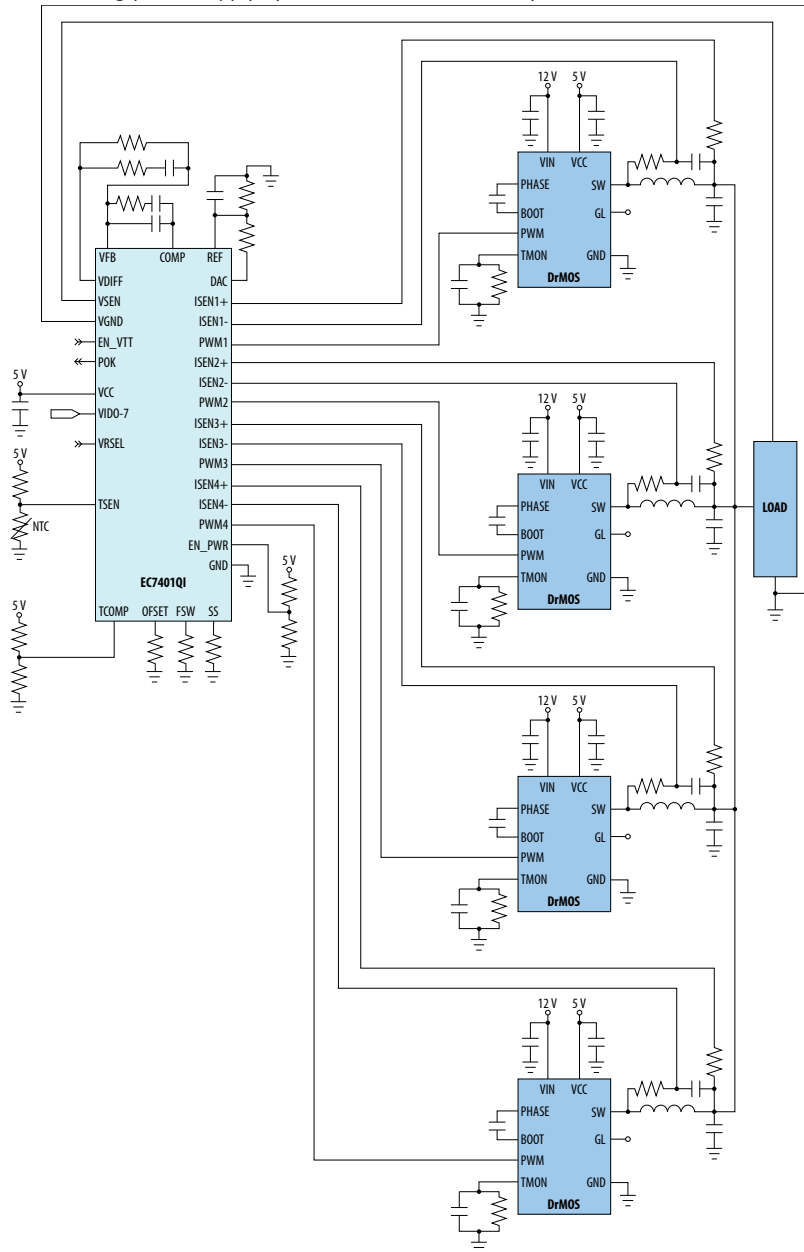
Figure 6. Level Shifter Block Diagram





**Figure 7. System Implementation using the EC7401QI Controller**

The EC7401QI controller connects easily to the Parallel SmartVID FPGA circuit. This provides an easy way to get a guaranteed working power supply system with SmartVID ability.



Using the EC7401QI 4-phase PWM controller with Parallel VID interface is one example solution for implementing the SmartVID capability of the Intel Arria 10 family. The EC7401QI drives up to four high current powertrain devices. The EC7401QI supports a wide range of Intel Arria 10 core power requirements. This solution easily enables system power reduction by leveraging the SmartVID capability via an Intel Arria 10 family parallel VID interface.



## Parallel SmartVID Regulator Implementation Guidelines

Parallel SmartVID regulator implementation with Intel Arria 10 devices requires the following characteristics:

- The boot voltage must be in default value (0.9 V) before VID is applied.
- The regulator must accept parallel VID logic signals with a maximum logic voltage of 1.8 V. If you need a higher voltage for the signals to the regulator, then a level shifter may be inserted between the FPGA and the regulator if necessary.
- The 8-bit parallel VID code must be similar to the lowest 6 bits of the Intel VRM 11 8-bit VID code. The exception is that the voltage least significant bit (LSB) step size is 5 mV instead of 6.25 mV. The range of adjustment must include 0.83 V to 0.95 V. The Parallel VID code only uses even codes (10 mV steps); thus the LSB can be omitted. The VID code will change by no more than 10 mV per step. See [Table 5](#) on page 22.
- The regulator must accept a VID update rate of 10 ms. Additionally, the voltage must reach within the tolerance envelope ( $\pm 5$  mV of the new VID value) within 10 ms of the last transition on the VID signals.
- If you require multiple parallel regulators to achieve the output current target, then the group of regulators must behave in the same way as a single regulator with respect to the VID functions.
- The regulator(s) must meet the static and ripple ( $\pm 30$  mV) and dynamic ( $\pm 5\%$ ) power tolerances during all phases of power delivery after the boot voltage is reached. Refer to the specifications described in the *Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines*.

### Related Information

[Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines](#)

## PMBus Control System

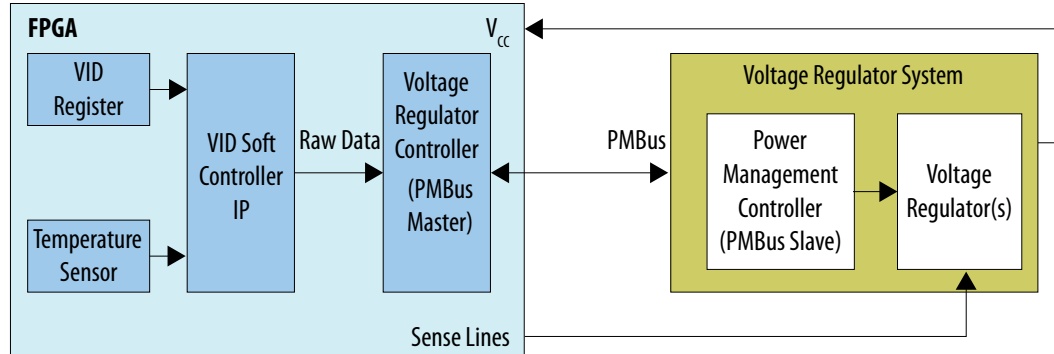
**Note:** Currently, the PMBus control system is being implemented on some Intel FPGA development boards. Contact your sales and service representative for availability.

In a PMBus system, the Intel Arria 10 device acts as either a PMBus master or a PMBus slave, according to your design choice. The following figure illustrates the simplest PMBus system for SmartVID support. In this case, the Intel Arria 10 device acts as a PMBus master and communicates the SmartVID information to the voltage regulator system directly through the PMBus.



**Figure 8. Data Flow for the PMBus Interface**

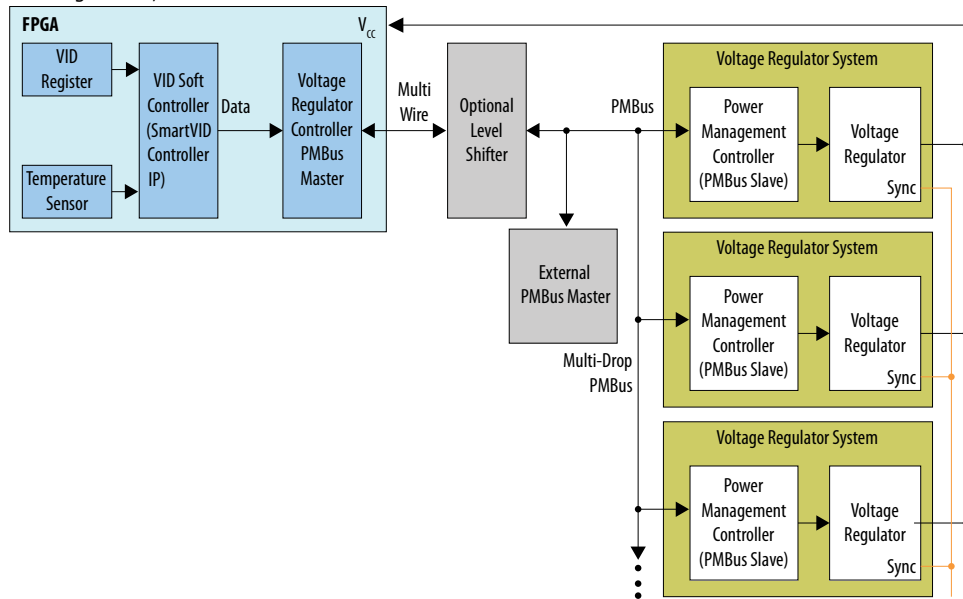
In this configuration, the only devices on the PMBus are the Intel Arria 10 device and the voltage regulator system. The voltage regulator system provides the core voltage for the Intel Arria 10 device.



In other PMBus systems, you may choose to have an external PMBus master separate from the Intel Arria 10 device. In this case, the Intel Arria 10 device may act as either a PMBus slave, or as a PMBus master in multi-master mode.

**Figure 9. PMBus System with Multiple Regulators**

In this configuration, the Intel Arria 10 device acts as a PMBus master in multi-master mode.



In this system, the VID soft controller feeds data to a PMBus Master interface on the FPGA. Other devices on the PMBus may require level shifters to translate the FPGA IO voltage to other voltage levels. PMBus systems can contain more than one regulator.

## PMBus System Implementation

PMBus interface support is planned for release with Intel Quartus Prime software version 15.1. Contact your sales representative concerning the availability of PMBus interface support ahead of Intel Quartus Prime software version 15.1.

None of the pins on the FPGA are tied to any specific function for the PMBus interface.



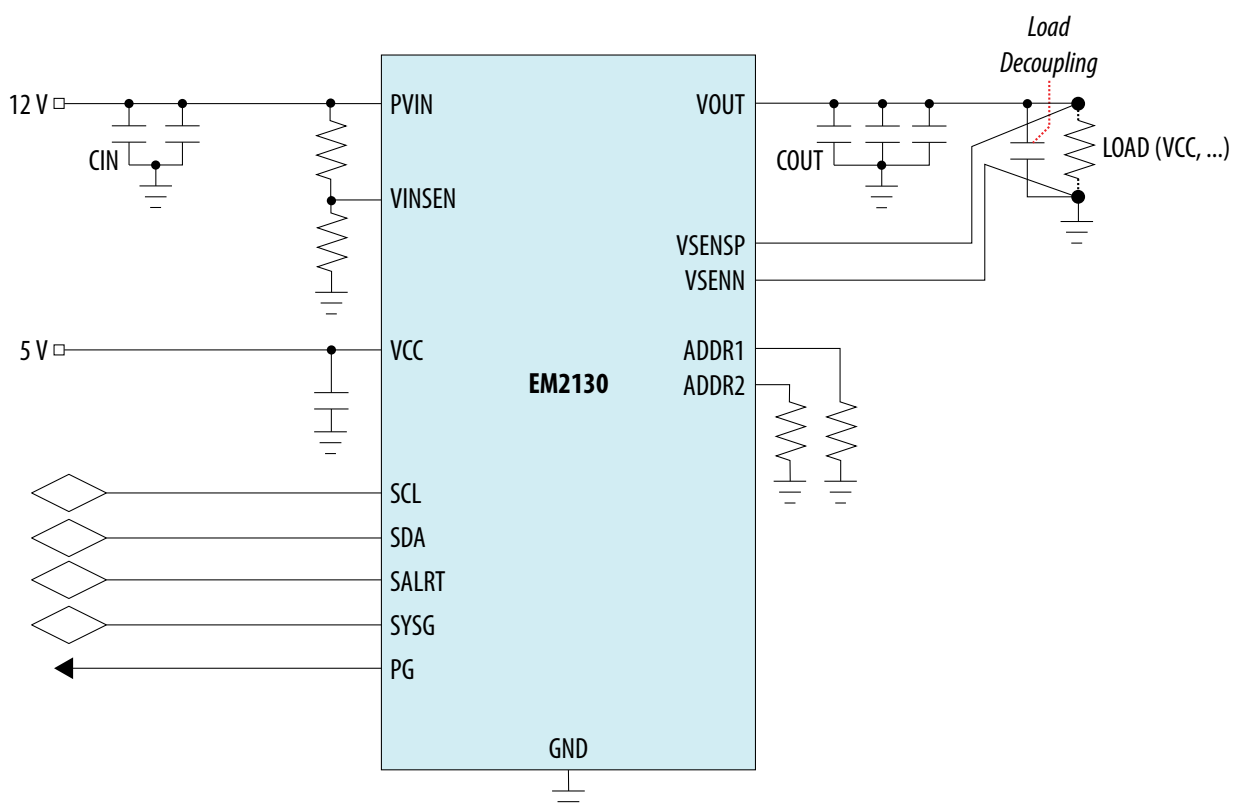
## **PMBus Voltage Regulators**

Voltage converter systems that include the PMBus interface can help you implement the SmartVID capability of the Intel Arria 10 family.

Intel recommends using an Intel Enpirion Digital Power Solution, such as the EM2260, EM2140, EM2130, or EM2120 devices, for new Intel Arria 10 designs. These devices are highly integrated, high current power modules with PMBus-compliant interfaces. This family of devices provides a single-chip solution for the programmable voltage regulator system needed to implement SmartVID and reduce system power. This maximizes power density while simplifying design.



Figure 10. EM2130 30A Digital PowerSoC





## Related Information

EM2120, EM2130, EM2140 Intel Enpirion Digital PowerSoCs

## PMBus VID Implementation Guidelines

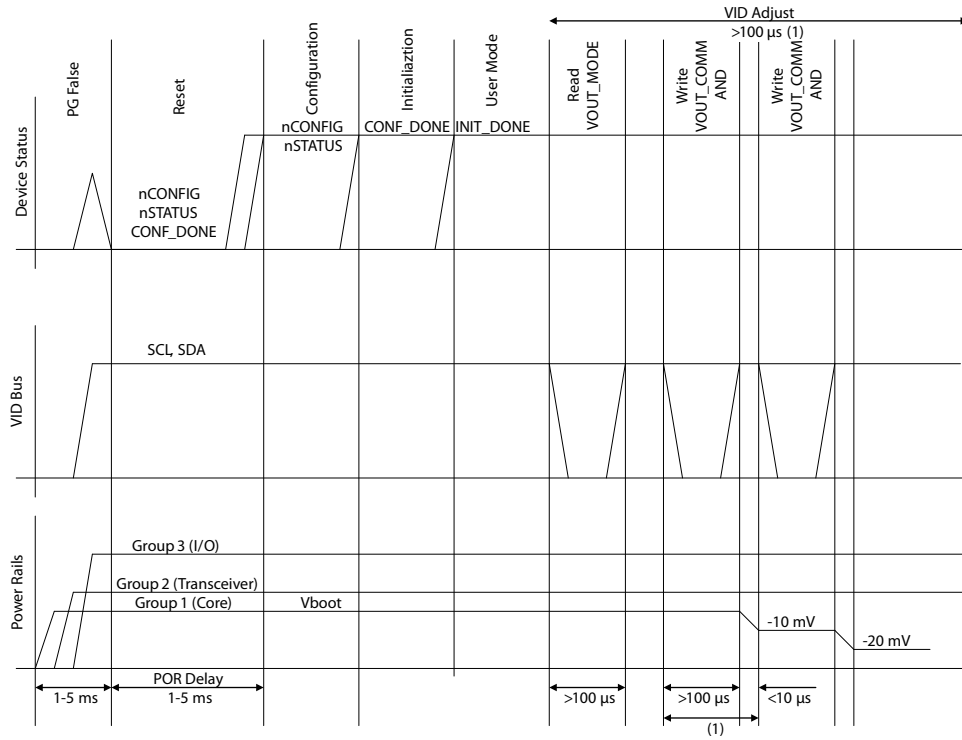
PMBus VID implementation with Intel Arria 10 devices requires the following characteristics:

- The regulator must support a default boot voltage prior to the issuing any VID commands.
- The regulator must support PMBus logic voltages no higher than 1.8 V (nominal). If the regulator logic levels are greater than 1.8 V, then some form of voltage level shifter is required for at least SCL and SDA signals.
- The regulator must support the PMBus Slave role with clock rates up to 400 kHz.
- The regulator must support the PMBus `VOUT_MODE(0x20, R)` command. The PMBus Master uses the `VOUT_MODE` command to interrogate the regulator to discover the data format for the `VOUT_COMMAND` values. The PMBus Master can be the FPGA or a system power manager.
- The regulator must support the PMBus `VOUT_COMMAND(0x21, R/W)` command. The PMBus Master uses the `VOUT_COMMAND` instruction in the data format retrieved from `VOUT_MODE` to write VID values to the regulator. The PMBus Master can be the FPGA or a system power manager. The VID voltage will change by no more than 10 mV per step.
- If you require multiple parallel regulators to achieve the output current target, then the group of regulators must behave as a single regulator with respect to the VID functions. This implies having distinct addresses for each of the regulators, and for the regulators to respond to `VOUT_COMMAND` using the SMBus Group Command Protocol. The SMBus Group Command Protocol writes to each address using repeated starts, with all devices simultaneously executing the command on the last STOP symbol.
- The regulator must accept a VID update rate of 10 ms, and the voltage must reach within the  $\pm 30$  mV tolerance envelope within 10 ms of the last STOP symbol for transmitting `VOUT_COMMAND`. Voltage change for 10 mv should be between 20  $\mu$ s and 45  $\mu$ s for each step.
- The regulator(s) must meet the static and ripple and dynamic power tolerances listed in the *Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines* during all phases of power delivery after the boot voltage is reached.





Figure 11. Boot Sequence for Intel Arria 10 Devices Using PMBus SmartVID



Note:  
 1. VID writes chosen to occur no faster than 10 ms to allow VID computation time.

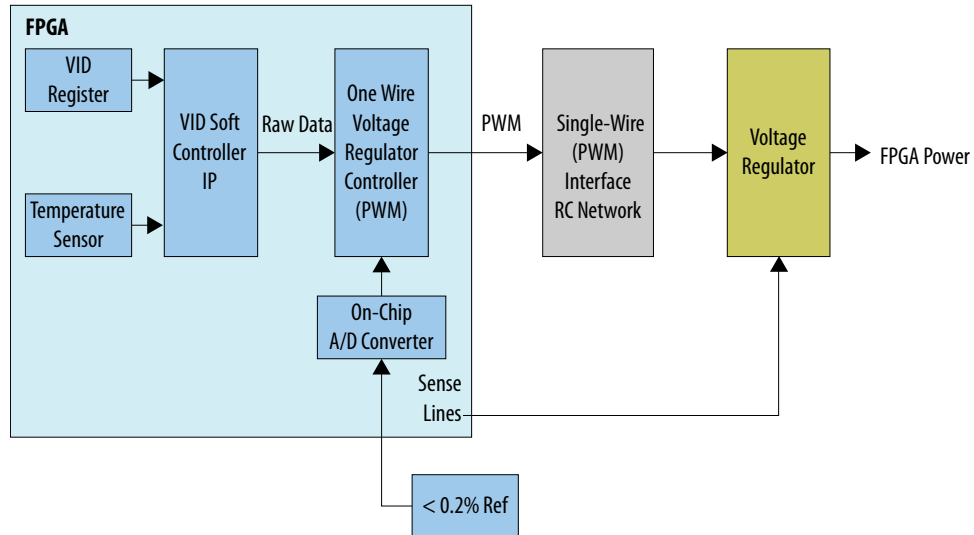
### Related Information

[Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines](#)

## Single-Wire Interface PWM Control System

**Figure 12. Data Flow for the Single-Wire Interface**

This topology shows the flow of data for a single-wire interface, pulse width modulation (PWM)-based control system.



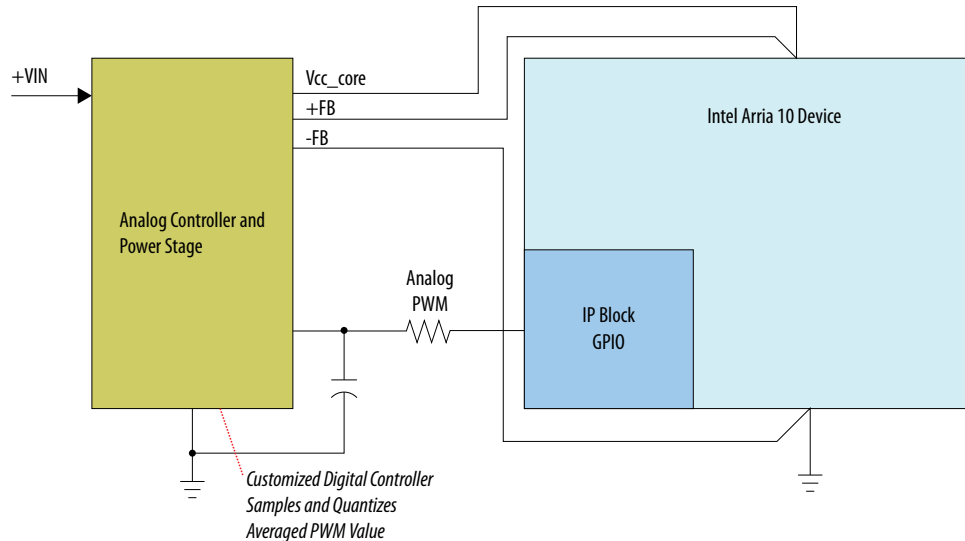
The single-wire interface control system uses the PWM of a single signal. An analog process translates that signal into a current that is added to the voltage feedback node of the power supply module. Voltage sense lines and an accurate voltage reference provide the analog-to-digital converter on the FPGA with the resulting voltage level.

## Single-Wire Interface PWM System Implementation

The single-wire interface is scheduled for release with Intel Quartus Prime software version 16.0. Please contact your sales representative for availability of single-wire interface support ahead of Intel Quartus Prime software version 16.0.



**Figure 13. Single-Wire Interface PWM System Implementation Example**



PWM VID feature has the following implementation requirements:

- General purpose I/O (GPIO) VDD must be held to 1.8 V+/-1% (tighter than pin connection guideline requirements).
- Slew rates of GPIO edges must be held to < 2 ns.
- GPIO output driver configuration must be push-pull with  $R_{ds} < 25 \Omega$  for both p-channel field effect transistor (pFET) and negative channel field effect transistor (nFET), such as 1.8 V SSTL Class II driver.
- Resistor insertion network must be scaled for suitable insertion values for the 10 mV/LSB VID steps.
- Resistor insertion network impedance must be high enough that 25- $\Omega$  driver resistance results in < 1% voltage error (about 30 k $\Omega$ ).
- Slew rate of the VID changes must be limited to a maximum of 10 mV/20  $\mu$ s by the regulator settings or the time constant of the resistor VID insertion network.
- The sense line current of the regulator(s) must not cause a voltage setting error of more than 1 mV with the VID resistor insertion network.
- An external reference for the voltage ADC must be used which has an accuracy over all causes of  $\pm 0.2\%$  as shown in Figure 12 on page 18.

## SmartVID Power Savings Estimation

The Intel Arria 10 device family Early Power Estimator (EPE) includes options for analyzing the possible power savings using SmartVID.

**Table 4. Important Parameter Settings for SmartVID Power Estimation**

Parameter	Value	Description
Temperature Grade	-2V	These are the only valid options to enable SmartVID.

*continued...*



Parameter	Value	Description
	-3V	
<b>Power Characteristics</b>	<b>Maximum</b>	This is the only option that shows the benefit of the static power reduction features for SmartVID. <i>Note:</i> The SmartVID Power Reduction field shows the power savings resulting from using SmartVID.

Figure 14. Example Early Power Estimator for Intel Arria 10 Devices

**PowerPlay Early Power Estimator**  
Arria® 10  
Version 14.1, Build 03.03

Visit the Online Power Management Resource Center

Input Parameters		Thermal Power (W)	
Family	Arria 10	Logic	3.967
Device	10AX066	RAM	0.867
Device Grade	Industrial -2L	DSP	0.399
Package	F34	Clock	1.131
Transceiver Grade	H2	PLL	0.085
Power Characteristics	Typical	I/O	3.608
V <sub>CC</sub> Voltage (mV)	900	XCVR	4.556
SmartVoltage ID	On	HPS	0.000
Power Model Status	PRELIMINARY	P <sub>STATIC</sub>	4.441
Junction Temp, T <sub>J</sub> (°C)	Auto Compute	<b>TOTAL (W)</b>	<b>19.234</b>
Ambient Temp, T <sub>A</sub> (°C)	25	SmartVID Power Savings	-7.58E-02
Cooling Solution	23 mm heat sink with 400 LFPm airflow	<b>TOTAL After SmartVID (W)</b>	<b>19.158</b>
θ <sub>JA</sub> Junction-Ambient	1.5	<b>Thermal Analysis</b>	
Board Thermal Model	N/A	Junction Temp, T <sub>J</sub> (°C)	50.0
θ <sub>JB</sub> Junction-Board	0.0	Maximum Allowed T <sub>A</sub> (°C)	93.4
Board Temp, T <sub>B</sub> (°C)	0		

Buttons: Reset, Import CSV, Export CSV, ViewReport, Manage Power Rail Configuration, Manage Power Regulators

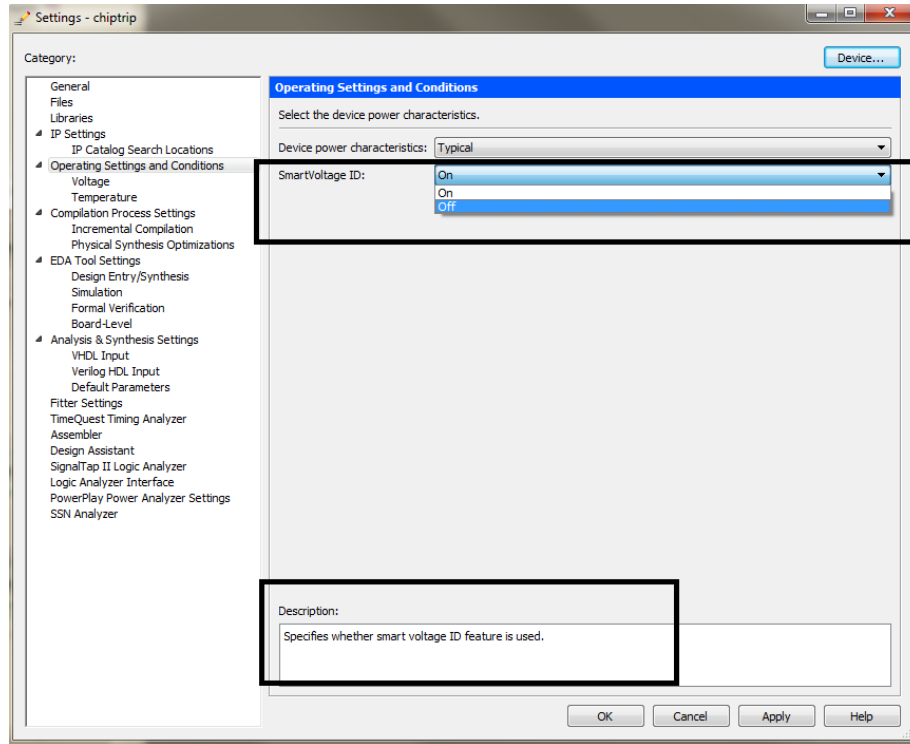
## Enabling SmartVID in the Intel Quartus Prime Software

If you want to use SmartVID in your Intel Arria 10 design, you must activate the feature within your Intel Quartus Prime project.

1. In the Intel Quartus Prime software, click **Assignments > Settings**.
2. In the **Category** pane, select **Operating Settings and Conditions**.
3. In the **SmartVoltage ID:** field, select **On** from the pull-down menu.
4. Click **OK**.



Figure 15. Intel Quartus Prime Setup for SmartVID



## VID Design for Intel Arria 10 FPGAs

Intel Arria 10 FPGAs can inform its core  $V_{CC}$  Voltage Regulator Module (VRM) of its required voltage and have the VRM re-adjust its output voltage automatically to match. The Intel Arria 10 FPGA supports this Voltage ID (or VID) feature in three forms—parallel VID, serial VID, and PWM VID.

### Parallel VID

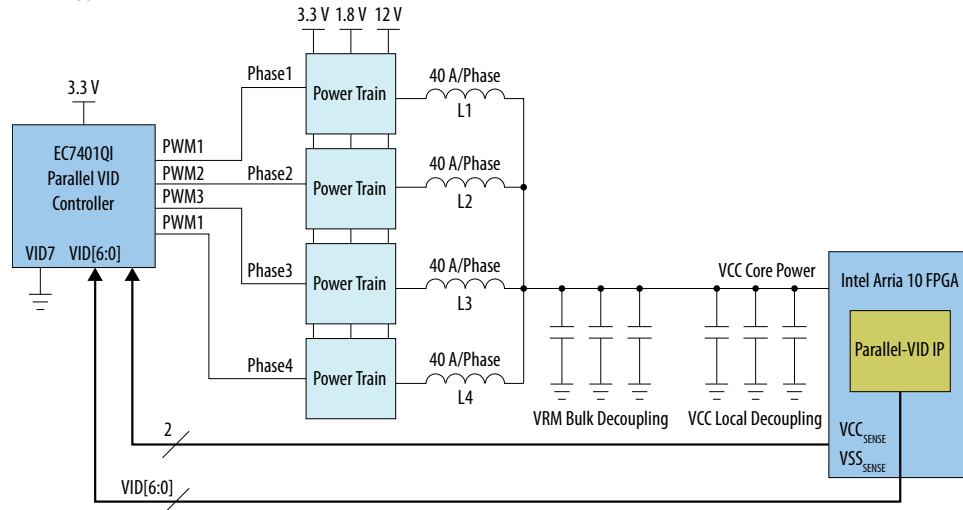
In parallel VID, the VRM is initially set to output a default voltage required by the FPGA device at power-on. Once the FPGA device is successfully powered on and configured, the FPGA outputs an 7-bit VID code ( $VID[6:0]$ ) to the VRM. In a system using a VRM that uses 8 bits, the LSB is grounded. This informs the VRM that a voltage change is requested. Based on this unique code, the VRM re-adjusts (raises or lowers) its output voltage automatically to meet the new voltage required by the FPGA. This reduces the  $V_{CC}$  core power by the square of the voltage multiplied by the current.

An implementation of this feature requires both hardware and software (IP) support. For the hardware portion, the selected VRM for the  $V_{CC}$  core must support a parallel VID interface capable of supporting the VID voltage levels required by the Intel Arria 10 FPGA. Additionally, because the  $V_{CC}$  core can sink over 100 A of current, you must account for the DC IR drop of the PCB  $V_{CC}$  plane and device package. This compensation requires the VRM to support remote sensing. One solution that supports

both VID and remote sensing is the EC7401QI 4-phase pulse-width modulation (PWM) controller with a 40A powertrain. This solution directly powers the V<sub>CC</sub> core power of the Intel Arria 10 FPGA while supporting its VID requirements.

**Figure 16. Parallel VID Block Diagram**

Parallel VID implementation using the EC7401QI + 4x powertrain delivering up to 160 A (40 A per phase) of V<sub>CC</sub> core current demanded by high-end FPGA applications.



**Table 5. Output Voltage Versus VID Codes**

VID codes and respective output voltages from the EC7401QI controller.

Voltage (V)	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Notes
0.830	0	1	0	1	1	1	0	0	
0.835	0	1	0	1	1	0	1	1	
0.840	0	1	0	1	1	0	1	0	
0.845	0	1	0	1	1	0	0	1	
0.850	0	1	0	1	1	0	0	0	
0.855	0	1	0	1	0	1	1	1	
0.860	0	1	0	1	0	1	1	0	
0.865	0	1	0	1	0	1	0	1	
0.870	0	1	0	1	0	1	0	0	
0.875	0	1	0	1	0	0	1	1	
0.880	0	1	0	1	0	0	1	0	
0.885	0	1	0	1	0	0	0	1	
0.890	0	1	0	1	0	0	0	0	
0.895	0	1	0	0	1	1	1	1	
0.900	0	1	0	0	1	1	1	0	Intel Arria 10 default voltage
0.905	0	1	0	0	1	1	0	1	

*continued...*

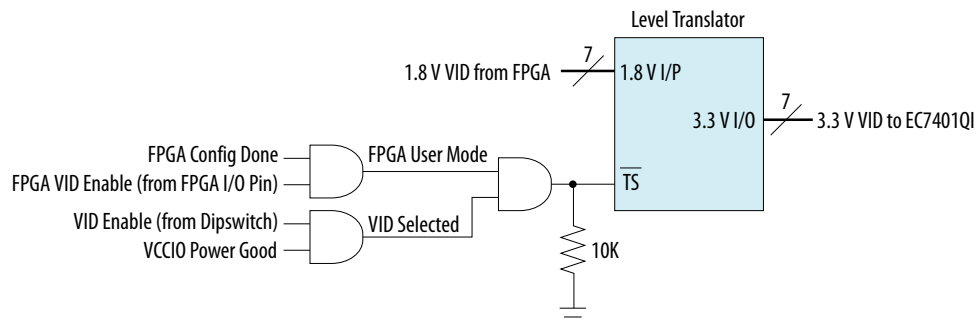


Voltage (V)	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Notes
0.910	0	1	0	0	1	1	0	0	
0.915	0	1	0	0	1	0	1	1	
0.920	0	1	0	0	1	0	1	0	
0.925	0	1	0	0	1	0	0	1	
0.930	0	1	0	0	1	0	0	0	
0.935	0	1	0	0	0	1	1	1	
0.940	0	1	0	0	0	1	1	0	
0.945	0	1	0	0	0	1	0	1	
0.950	0	1	0	0	0	1	0	0	

After power-on but before programming the FPGA, the EC7401QI design must be strapped to set the default voltage to 0.900 V at the device. Connecting the EC7401QI device's differential remote sense lines (VSEN and RGND) to the VCCLsense and VSSsense of the Intel Arria 10 device manages the power plane and package DC IR drop compensation. Once the device is programmed, the VID IP instantiated within the FPGA reads the fuse bits burned into the FPGA. It then sends out the parallel VID codes to override the 0.900 V default voltage set by the strapping resistors. Because the VID signals coming from the FPGA use 1.8 V IO standards, level translators interface these signals to the 3.3 V IO standard of the EC7401QI. In addition to the level translators, Intel also uses additional signals to generate a VID\_READY signal to the level translator. This ensures that any spurious glitches on the VID I/O pins are avoided during the time between configuration and USER mode. The following signals are ANDed together to generate a VID\_READY signal that enables the level translator:

- FPGA CONFIG DONE
- FPGA VID ENABLE (from an FPGA I/O pin)
- VID ENABLE (from an on-board DIP switch)
- VCCIO Power Good

Figure 17. VID READY Generation



**Related Information**

[EC7401QI: 4-Phase PWM Controller with 8-Bit DAC Code](#)

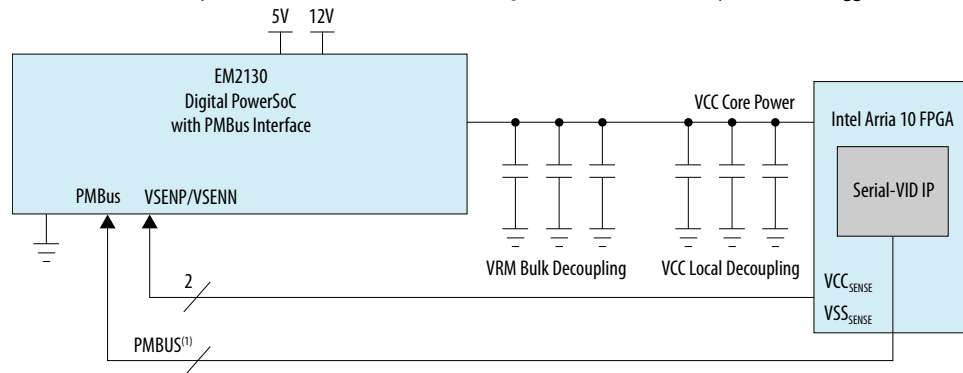
## PMBus SmartVID

In PMBus SmartVID, the VRM is initially set to output a default voltage (0.9 V) required by the FPGA device at power-on. Once the FPGA device is successfully powered-on and configured, the FPGA uses PMBus to inform the VRM that a voltage change is requested. Based on the new configuration, the VRM re-adjusts (raises or lowers) its output voltage automatically to meet the new voltage required by the FPGA. In turn, the Intel Arria 10 device's  $V_{CC}$  core power can be reduced by the square of the voltage multiplied by the current.

Implementing this feature requires both hardware and software (IP) support. For the hardware portion, the selected VRM for the  $V_{CC}$  core must support the PMBus interface and remote sensing. One solution that supports both the PMBus and remote sensing is the Intel Enpirion EM2130xQI Digital PowerSoC DC-DC step-down converter with PMBus interface.. This solution is designed to directly power the  $V_{CC}$  core power of the Intel Arria 10 SoC FPGA while supporting its VID requirements. The following figure shows the block diagram of the PMBus implementation using the EM2130xQI solution to deliver up to 30A of  $V_{CC}$  core current. This solution is also footprint scalable with the Intel Enpirion EM2120xQI and EM2140xQI solutions, which can deliver up to 20A and 40A  $V_{CC}$  core current respectively.

**Figure 18. PMBus SmartVID Block Diagram**

This PMBus SmartVID implementation uses the EM2130xQI solution to deliver up to 30A of  $V_{CC}$  core current.



Note:

1. A level shifter may be required if the PMBus power converter requires voltage levels higher than 1.8 V logic from the FPGA.

### Related Information

- [EM2130xQI: 30A PowerSoC DC-DC Step-Down Converter](#)
- [EM2120, EM2130, EM2140 Intel Enpirion Digital PowerSoCs](#)





## VID Design Guidelines

Intel recommends that you follow these guidelines to ensure VID system robustness.

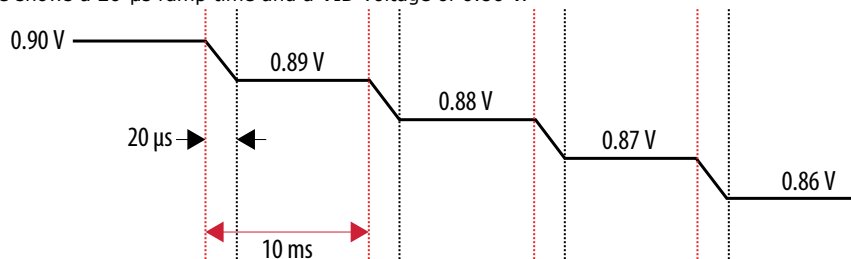
- Power regulator ramp time for 10-mV changes:
  - Minimum = 20  $\mu$ s
  - Maximum = 45  $\mu$ s

*Note:* The maximum ramp time is bounded by the configuration via protocol (CvP) requirement. This is only required if it is linked to  $T_{RISE}$  of  $VCC_{core}$ .

- 10 ms interval for every 10 mV step changes on top of the ramp time requirement above.

**Figure 19. Power Regulator Behavior Based on Ramp Time and 10-ms Interval**

This example shows a 20- $\mu$ s ramp time and a VID voltage of 0.86 V.



**Table 6. Operating Recommendations for VID Device Based on Temperature Grade**

Device Temperature Grade	Implementation Scheme
Extended temperature (0° C to 100° C)	<ul style="list-style-type: none"> <li>– User mode temperature dependency control scheme: Disabled</li> <li>– VID voltage changes immediately following user mode and before any user activity begins.</li> </ul>
Industrial temperature (-40° C to 100° C)	<ul style="list-style-type: none"> <li>– User mode temperature dependency control scheme: Enabled</li> </ul>

## Document Revision History for AN 711: Power Reduction Features in Intel Arria 10 Devices

Document Version	Changes
2018.07.12	<ul style="list-style-type: none"> <li>• Updated the EC7401 device name to EC7401QI.</li> <li>• Updated the voltage regulator system implementation in the <i>System Topology Options</i> section.</li> <li>• Updated the supported Intel Enpirion devices in the <i>PMBus Voltage Regulators</i> and <i>PMBus SmartVID</i> sections.</li> <li>• Removed support for the ET4040QI Powertrain.</li> <li>• Removed support for the ED8101P0xQI Controller.</li> <li>• Updated the <i>Level Shifter Block Diagram</i> figure.</li> <li>• Updated the <i>System Implementation using the EC7401QI Controller</i> figure.</li> <li>• Updated the <i>Single-Wire Interface PWM System Implementation Example</i> figure.</li> <li>• Updated the <i>Parallel VID Block Diagram</i> figure.</li> <li>• Updated the <i>VID Ready Generation</i> figure.</li> <li>• Updated the <i>PMBus SmartVID Block Diagram</i> figure.</li> </ul>



Document Version	Changes
	<ul style="list-style-type: none"> <li>Removed the <i>ED8101P0xQI Controller with PMBus</i> figure.</li> <li>Removed the <i>PWR to V<sub>CC</sub> Controller</i> figure.</li> <li>Removed the <i>PWR to Enpirion Power Train Phase 1 and 2</i> figure.</li> <li>Removed the <i>PWR to Enpirion Power Train Phase 3 and 4</i> figure.</li> <li>Removed the <i>12 V to 9 V Converter (Controller)</i> figure.</li> <li>Removed the <i>12V to 9V Converter (40-A MOSFET)</i> figure.</li> </ul>

Date	Version	Changes
May 2017	2017.05.08	<ul style="list-style-type: none"> <li>Updated to reflect current product availability.</li> <li>Rebranded as Intel.</li> </ul>
October 2016	2016.10.31	<ul style="list-style-type: none"> <li>Changed instances of Quartus II to Quartus Prime.</li> <li>Updated the V<sub>CC</sub> SmartVID voltage value.</li> <li>Updated the EM1130 device to the EM2130 device.</li> <li>Updated the EM2130 PowerSoC figure.</li> <li>Removed support for the V<sub>CC</sub> PowerManager feature.</li> </ul>
December 2015	2015.12.16	<p>Made the following changes:</p> <ul style="list-style-type: none"> <li>Removed a parameter from the "Operating Recommendations for VID Device Based on Temperature Grade" table.</li> <li>Changed the operating guidelines in the "Operating Recommendations for the V<sub>CC</sub> PowerManager Device Based on Temperature Grade" table.</li> </ul>
June 2015	2015.06.25	<p>Made the following changes:</p> <ul style="list-style-type: none"> <li>Changed the temperature parameter in the "VCC PowerManager and SmartVID" section.</li> <li>Changed the "Power Sense Lines with Single and Multiple Regulator Configurations" figure.</li> <li>Global: replaced "MegaCore function" with "Controller IP."</li> <li>Changed the availabilities in the "Reference Design Availability Schedule" table.</li> <li>Added the "Parallel SmartVID Regulator Implementation Guidelines" section.</li> <li>Added the "PMBus VID Implementation Guidelines" section.</li> <li>Changed the software release availability in the "Single-Wire Interface PWM System Implementation" section.</li> <li>Added the "VID Design for Arria 10 FPGAs" section.</li> <li>Added the "Parallel VID" section.</li> <li>Added the "VID and mV Design Guidelines" section.</li> </ul>
April 2015	2015.04.08	<p>Made the following changes:</p> <ul style="list-style-type: none"> <li>Added voltage information to the "VCC PowerManager and SmartVID" section.</li> <li>Changed the availability for Parallel and PMBus systems in the "Reference Design Availability Schedule" table.</li> <li>Added the "SmartVID Controller IP Core" section.</li> <li>Replaced the "Example PowerPlay Early Power Estimator for Arria 10 Devices" figure.</li> </ul>
October 2014	2014.10.24	Initial release.