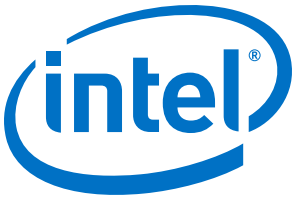

# AN 692: Power Sequencing Considerations for Intel® Cyclone® 10 GX, Intel® Arria® 10, and Intel® Stratix® 10 Devices

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# Contents

# 1. References

**Table 1. Related Links**

| Title | Link |
|---|---|
| Errata Sheets | https://www.intel.com/content/www/us/en/programmable/documentation/lit-es.html |
| Intel® Stratix® 10 Power Management User Guide | Intel Stratix 10 Power Management User Guide |
| Intel Stratix 10 Device Family Pin Connection Guidelines | Intel Stratix 10 Device Family Pin Connection Guidelines |
| Intel Stratix 10 Device Datasheet | Intel Stratix 10 Device Datasheet |
| Intel Arria® 10 GX, GT, and SX Pin Connection Guidelines | Intel Arria 10 GX, GT, and SX Pin Connection Guidelines |
| Intel Arria 10 Device Datasheet | Intel Arria 10 Device Datasheet |
| Intel Cyclone® 10 GX Device Family Pin Connection Guidelines | Intel Cyclone 10 GX Device Family Pin Connection Guidelines |
| Intel Cyclone 10 GX Device Datasheet | Intel Cyclone 10 GX Device Datasheet |
| Quad-Comparator Circuit Provides Power-Down Sequencing At Low Cost | How2Power Today, Josh Mandelcorn |

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# 2. Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices

The Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices require a specific power-up and power-down sequence. This document describes several power management options and discusses proper I/O management during device power-up and power-down. Design your power supply solution to properly control the complete power sequence.

The requirements in this document must be followed to prevent unnecessary current draw to the FPGA device. Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices do not support 'Hot-Socketing' except under the conditions stated in the table below. The tables below also show what the unpowered pins can tolerate during power-up and power-down sequences.

**Table 2. Pin Tolerance – Power-Up/Power-Down**

'√' is Acceptable; '-' is Not Applicable.

| | Power-Up | | | | Power-Down | | | |
|---|---|---|---|---|---|---|---|---|
| **Pin Type** | **Tristate** | **Drive to GND** | **Drive to VCCIO** | **Driven with < 1.0 Vp-p** | **Tristate** | **Drive to GND** | **Drive to VCCIO** | **Driven with < 1.0 Vp-p** |
| 3VIO banks | √ | - | - | - | √ | √ | - | - |
| LVDS I/O banks | √ | √ | √(1) | - | √ | √ | √(1) | - |
| Differential Transceiver pins | √ | √ | - | √(2) | √ | √ | - | √(2) |

**Related Information**

- LVDS I/O Pin Guidance for Unpowered FPGA on page 23
- Transceiver Pin Guidance for Unpowered FPGA on page 23

(1) The maximum current allowed through any LVDS I/O bank pin when the device is unpowered or during power up/down conditions = 10 mA (refer to "LVDS I/O Pin Guidance for Unpowered FPGA Pins").

(2) This applies to Intel Stratix 10 L-tile/H-tile only (refer to "Transceiver Pin Guidance for Unpowered FPGA Transceiver Pins").

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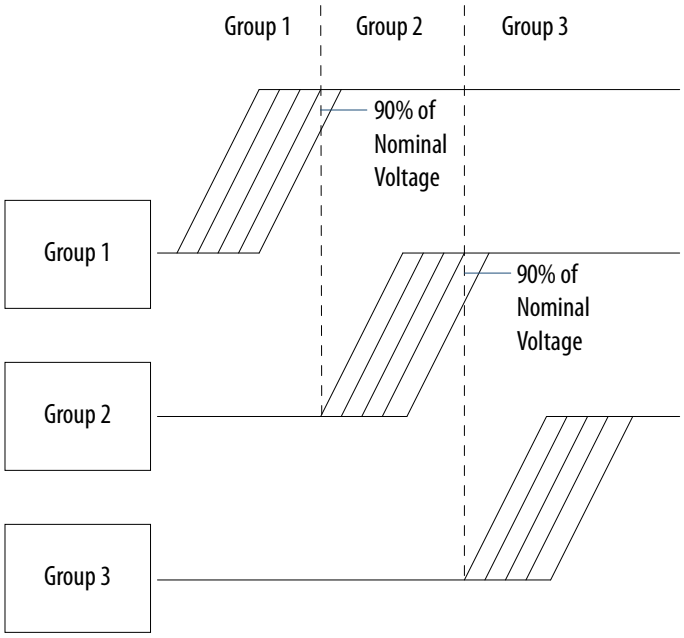
## 2.1. Power-Up Sequence Requirements for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices

The power rails in Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices are each divided into three groups. Refer to the *Intel Cyclone 10 GX Device Family Pin Connection Guidelines*, *Intel Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines*, *Intel Stratix 10 Device Family Pin Connection Guidelines*, and the *Intel Stratix 10 Power Management User Guide* for additional details.

The diagram below illustrates the voltage groups of the Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices and their required power-up sequence.

**Figure 1. Power-Up Sequence for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices**




*Note:* $V_{CCBAT}$ is not in any of the groups below. $V_{CCBAT}$ does not have any sequence requirements. $V_{CCBAT}$ holds the contents of the security keys.

**Table 3. Voltage Rails**

| Devices | Intel Cyclone 10 GX | Intel Arria 10 | Intel Stratix 10 GX<br>Intel Stratix 10 SX<br>Intel Stratix 10 MX (H-Tile Only) | Intel Stratix 10 MX (H-Tile and E-Tile)<br>Intel Stratix 10 TX |
|---|---|---|---|---|
| Group 1 | $V_{CC}$<br>$V_{CCP}$<br>$V_{CCERAM}$<br>$V_{CCR\_GXB}$<br>$V_{CCT\_GXB}$ | $V_{CC}$<br>$V_{CCP}$<br>$V_{CCERAM}$<br>$V_{CCR\_GXB}$<br>$V_{CCT\_GXB}$<br>$V_{CCL\_HPS}$ | $V_{CC}$<br>$V_{CCP}$<br>$V_{CCERAM}$<br>$V_{CCR\_GXB}$<br>$V_{CCT\_GXB}$<br>$V_{CCL\_HPS}$<br>$V_{CCPLLDIG\_SDM}$<br>$V_{CCPLLDIG\_HPS}$ | $V_{CC}$<br>$V_{CCP}$<br>$V_{CCERAM}$<br>$V_{CCR\_GXB}$<br>$V_{CCT\_GXB}$<br>$V_{CCL\_HPS}$<br>$V_{CCPLLDIG\_SDM}$<br>$V_{CCPLLDIG\_HPS}$ |

***continued...***

| Devices | Intel Cyclone 10 GX | Intel Arria 10 | Intel Stratix 10 GX<br>Intel Stratix 10 SX<br>Intel Stratix 10 MX (H-Tile Only) | Intel Stratix 10 MX (H-Tile and E-Tile)<br>Intel Stratix 10 TX |
|---|---|---|---|---|
| | | | | $V_{CCRT\_GXE}$<br>$V_{CCRTPLL\_GXE}$ |
| Group 2 | $V_{CCPT}$<br>$V_{CCH\_GXB}$<br>$V_{CCA\_PLL}$ | $V_{CCPT}$<br>$V_{CCH\_GXB}$<br>$V_{CCA\_PLL}$<br>$V_{CCPLL\_HPS}$<br>$V_{CCIOREF\_HPS}$ | $V_{CCPT}$<br>$V_{CCH\_GXB}$<br>$V_{CCA\_PLL}$<br>$V_{CCPLL\_HPS}$<br>$V_{CCPLL\_SDM}$<br>$V_{CCADC}$<br>$V_{CCM\_WORD}$(3) | $V_{CCPT}$<br>$V_{CCH\_GXB}$<br>$V_{CCA\_PLL}$<br>$V_{CCPLL\_HPS}$<br>$V_{CCPLL\_SDM}$<br>$V_{CCADC}$<br>$V_{CCM\_WORD}$(3)<br>$V_{CCH\_GXE}$<br>$V_{CCCLK\_GXE}$ |
| Group 3 | $V_{CCPGM}$<br>$V_{CCIO}$ | $V_{CCPGM}$<br>$V_{CCIO}$<br>$V_{CCIO\_HPS}$ | $V_{CCIO}$<br>$V_{CCIO3V}$<br>$V_{CCIO\_SDM}$<br>$V_{CCIO\_HPS}$<br>$V_{CCFUSEWR\_SDM}$<br>$V_{CCIO\_UIB}$(3) | $V_{CCIO}$<br>$V_{CCIO3V}$<br>$V_{CCIO\_SDM}$<br>$V_{CCIO\_HPS}$<br>$V_{CCFUSEWR\_SDM}$<br>$V_{CCIO\_UIB}$(3) |

All power rails in Group 1 must ramp up (in any order) to a minimum of 90% of their respective nominal voltage before the power rails from Group 2 can start ramping up.

The power rails within Group 2 can ramp up in any order after the last power rail in Group 1 ramps to the minimum threshold of 90% of its nominal voltage. All power rails in Group 2 must ramp to a minimum threshold of 90% of their nominal value before the Group 3 power rails can start ramping up.

The power rails within Group 3 can ramp up in any order after the last power rail in Group 2 ramps up to a minimum threshold of 90% of their full value.

For Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices, you can combine and ramp up Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as Group 2 power rail $V_{CCPT}$. Exception: E-tile devices must maintain voltage rail groupings for power-up sequencing as stated in the table above. $V_{CCCLK\_GXE}$ must power up before $V_{CCIO\_SDM}$.

*Note:* Ensure that the newly combined power rails do not cause any driving of unpowered GPIO or transceiver pins.

All power rails must ramp up monotonically. The power-up sequence should meet either the standard or the fast Power On Reset (POR) delay time. The POR delay time depends on the POR delay setting you use.

(3) Applies to Intel Stratix 10 MX devices only

**Table 4. POR Delay Specification**

| Device | POR Delay | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Intel Stratix 10 | AS (Normal mode), AVST ×8, AVST ×16, AVST ×32, SD/MMC | 12 | 20 | ms |
| Intel Stratix 10 | AS (Fast mode) | 2 | 6.5 | ms |
| Intel Cyclone 10 GX<br>Intel Arria 10 | Standard | 100 | 300 | ms |
| Intel Cyclone 10 GX<br>Intel Arria 10 | Fast | 4 | 12(4) | ms |

For configuration via protocol (CvP), the total TRAMP must be less than 10 ms from the first power supply ramp-up to the last power supply ramp-up. Select a fast POR delay setting to allow sufficient time for the PCI Express* (PCIe) link initialization and configuration. The power-up sequence must meet either the standard or fast POR delay time depending on the POR delay setting you use.

### Related Information

- Intel Cyclone 10 GX Device Family Pin Connection Guidelines
- Intel Arria 10 GX, GT, and SX Pin Connection Guidelines
- Intel Stratix 10 Device Family Pin Connection Guidelines
- Intel Stratix 10 Power Management User Guide

## 2.2. Power-Down Sequence Recommendations and Requirements for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices

Intel's FPGAs need to follow certain requirements during a power-down sequence. The power-down sequence can be a controlled power-down event via an on/off switch or an uncontrolled event as with a power supply collapse. In either case, you must follow a specific power-down sequence. Below are three power-down sequence specifications. They are either Recommended Power-Down Ramp, Required Power-Down Ramp, or Required Voltage Differential. To comply with Intel's FPGA Power-Down requirements, the Recommended option is best.

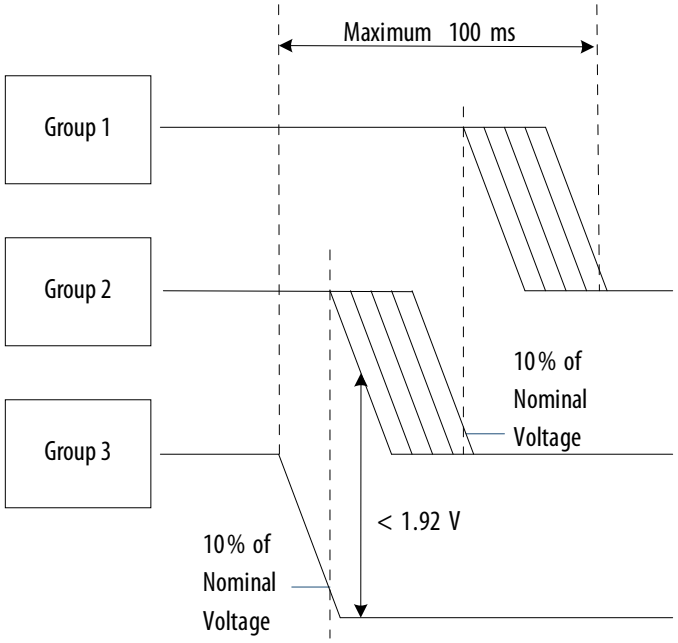
*Note:* If you cannot follow the Recommended specification, you must follow the Required specification. The Required specification includes both the Power-Down Ramp and the Voltage Differential specifications.

### Recommended Power-Down Ramp Specification

This is the best option to minimize power supply currents.

(4) PCIe* hard IP to initialize after POR trip.

**Figure 2. Recommended Power-Down Ramp Specification**




- Power down all power rails fully within 100 ms.
- Power down power supplies within the same Group in any order.
- Before Group 2 supplies power down, power down all Group 3 supplies within 10% of GND.
- Before Group 1 supplies power down, power down all Group 2 supplies within 10% of GND.
- The maximum voltage differential between any Group 3 supply and any Group 2 supply is 1.92 V.

For Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices, you can combine and ramp down Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as the Group 2 power rails.

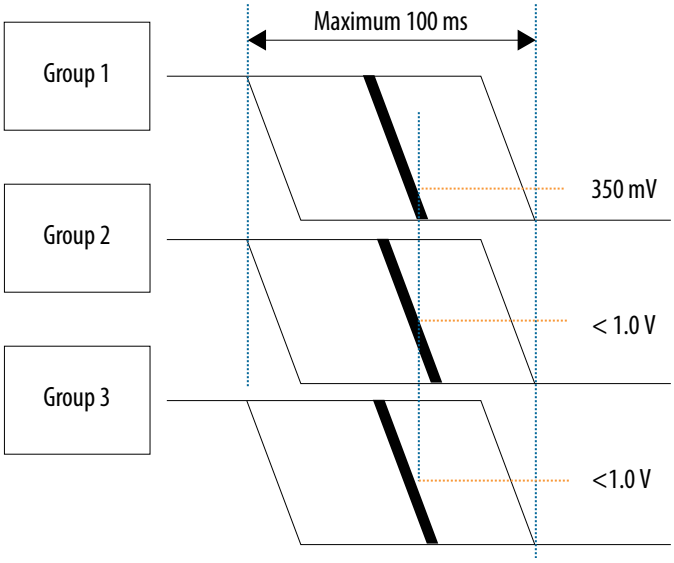
- Ensure that the newly combined power rails do not cause any driving of unpowered GPIO or transceiver pins.
- Ensure that the newly combined power rails do not violate any power-down sequencing specification due to device (third party) leakage; maintain the Required Voltage Differential Specification.

During the power-up/down sequence, the device output pins are tri-stated. To ensure long term reliability of the device, Intel recommends that you do not drive the input pins during this time.

### Required Power-Down Ramp Specification

In cases where power supply is collapsing or if the recommended specification cannot be met, the following PDS sequence is required.

**Figure 3. Required Power-Down Ramp Specification**



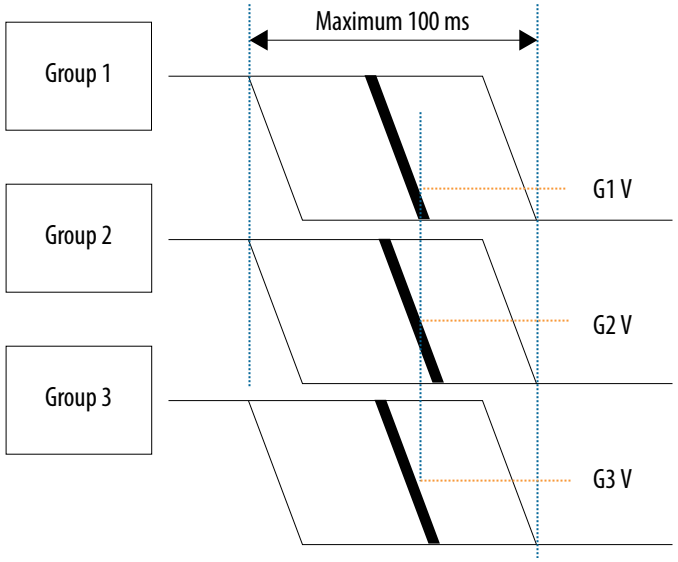

- Power down all power rails fully within 100 ms.
- As soon as possible, disable all power supplies.
  - Tri-state Group 1 supplies, and do not drive them actively to GND.
  - If possible, drive or terminate Group 2 and Group 3 supplies to GND.
- Ensure no alternative sourcing of any power supply exists during the power-down sequence; reduce all supplies monotonically and with a consistent RC typical decay.
- By the time any Group 1 supply goes under 0.35 V, all Group 2 and Group 3 supplies must be under 1.0 V.

### Required Voltage Differential Specification

To not excessively overstress device transistors during power-down, there is an additional voltage requirement between any two power supplies between different power groups during power-down:

$\Delta V < \Delta V_{nom} + 500$ mV

**Figure 4. Required Voltage Differential Specification**




- Power down all power rails fully within 100 ms.
- For example, if Group 1 Voltage = 0.9 V, Group 2 Voltage = 1.8 V, and Group 3 Voltage = 3.0 V, then:

| | | |
|---|---|---|
| $G3V_{nom}$ = 3.0 V<br>$G2V_{nom}$ = 1.8 V | $G2V_{nom}$ = 1.8 V<br>$G1V_{nom}$ = 0.9 V | $G3V_{nom}$ = 3.0 V<br>$G1V_{nom}$ = 0.9 V |
| $(G3V - G2V)_{nom}$ = 1.2 V | $(G2V - G1V)_{nom}$ = 0.9 V | $(G3V - G1V)_{nom}$ = 2.1 V |
| (G3V – G2V) <= 1.2 V + .5 V | (G2V – G1V) <= 0.9 V + .5 V | (G3V – G1V) <= 2.1 V + .5 V |
| (G3V – G2V) <= 1.7 V | (G2V – G1V) <= 1.4 V | (G3V – G1V) <= 2.6 V |

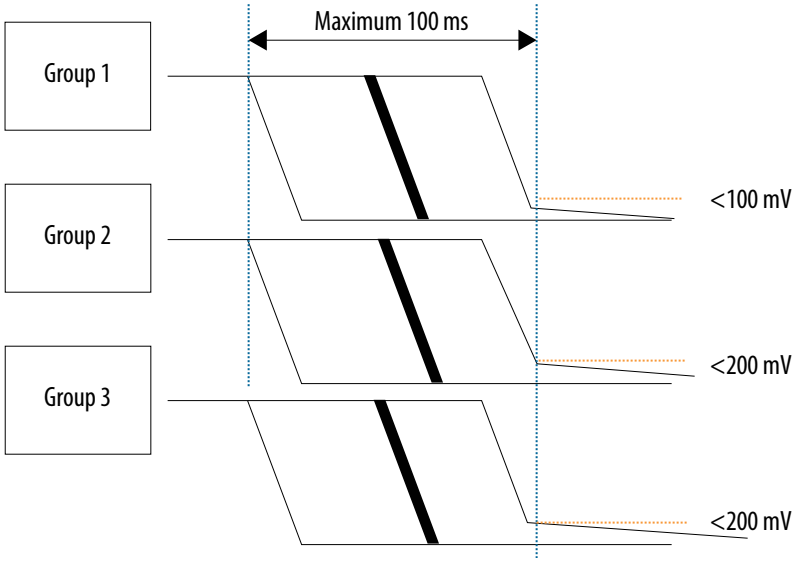
- To meet this voltage differential requirement, ramp down all power supplies as soon as possible according to the Required Power-Down Ramp Specification.

*Note:* Not following the required power sequence can result in unpredictable device operation and internal high current paths.

### Relaxed Power-Down Duration Specification

For supplies powered down with no active discharge, voltage reduction to GND slows down as supply approaches 0 V. In this case, the 100 ms power requirement is relaxed.

**Figure 5. Relaxed Power-Down Duration Specification**




- Ensure all Group 1 supplies reach < 100 mV within 100 ms.
- Ensure all Group 2 and Group 3 supplies reach < 200 mV within 100 ms.

# 3. Controlled Sequence Designs

## 3.1. Programmable Power Management Controller (PPMC) (Recommended Version)

Using a programmable power management controller provides a full-featured option to implement the power sequencing requirements.

These controllers provide the necessary power-up/down sequence control functions. These controllers can dynamically monitor and scale the regulator's output voltage, and supervise fault conditions such as over voltage or under voltage. To program the power management controller, typically a PMBus or $I^2C$ interface is used to connect to an intelligent host such as the system's microprocessor.

PPMC can be an optimal solution for systems in which up-time and fault tolerance are critical features and voltage monitoring and fault reporting are essential system requirements.

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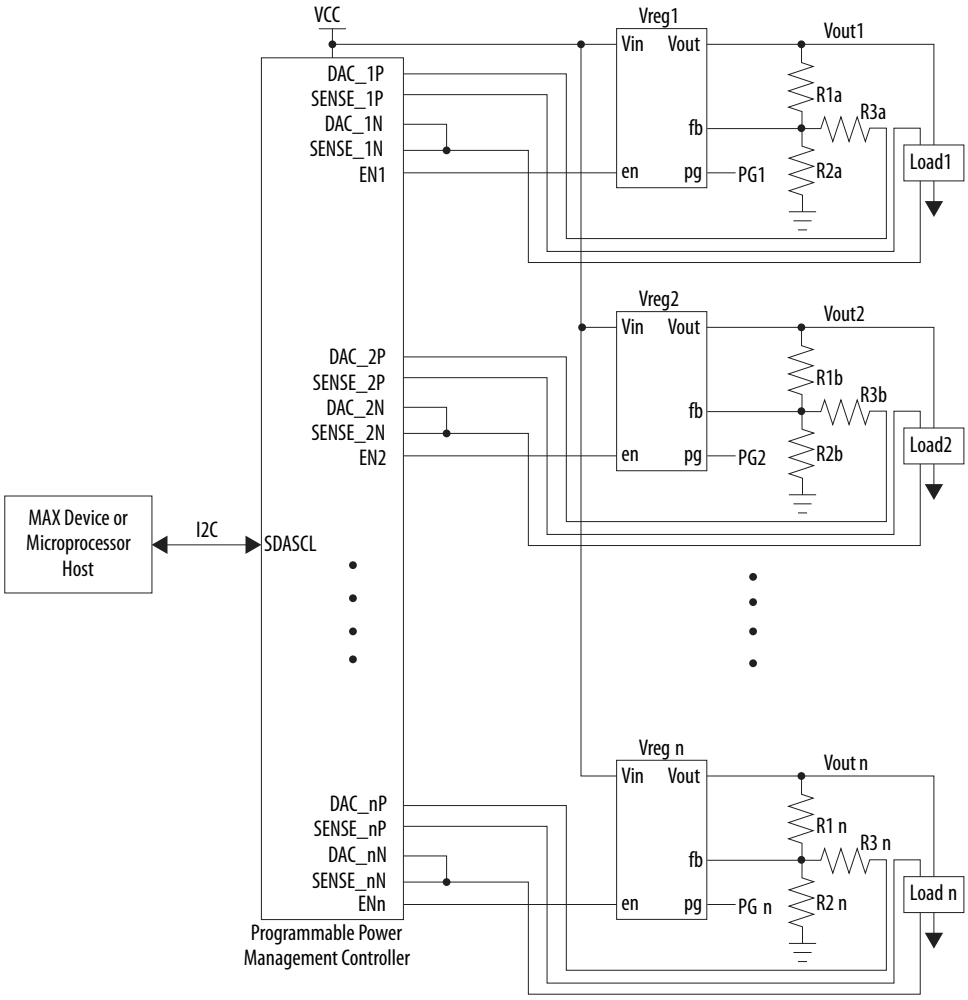
### 3.1.1. PPMC Example Design

**Figure 6. Simplified Programmable Power Management Controller With Multiple Channels**




A single channel of the PPMC typically provides the following features:

- Differential sense line inputs to remotely monitor the load voltage.
- Digital-to-Analog Converter (DAC) outputs to trim the regular output voltages. The DAC outputs drive the regulator's feedback input (`fb`) and control the regulator's output voltage.
- Enable Outputs (`EN1, EN2, ...ENn`) that drive the voltage regulator's Enable Inputs (`en`). The regulator's enable inputs control the desired power-up/down sequence.

Typically, PPMC devices have multiple channels so that a single controller can sequence multiple regulators. If more channels are required than what is offered by a single device, then multiple devices can be cascaded. A separate host interface (PMBus or $I^2C$) is used to connect the system processor and the PPMC to manage the controller software and programming.

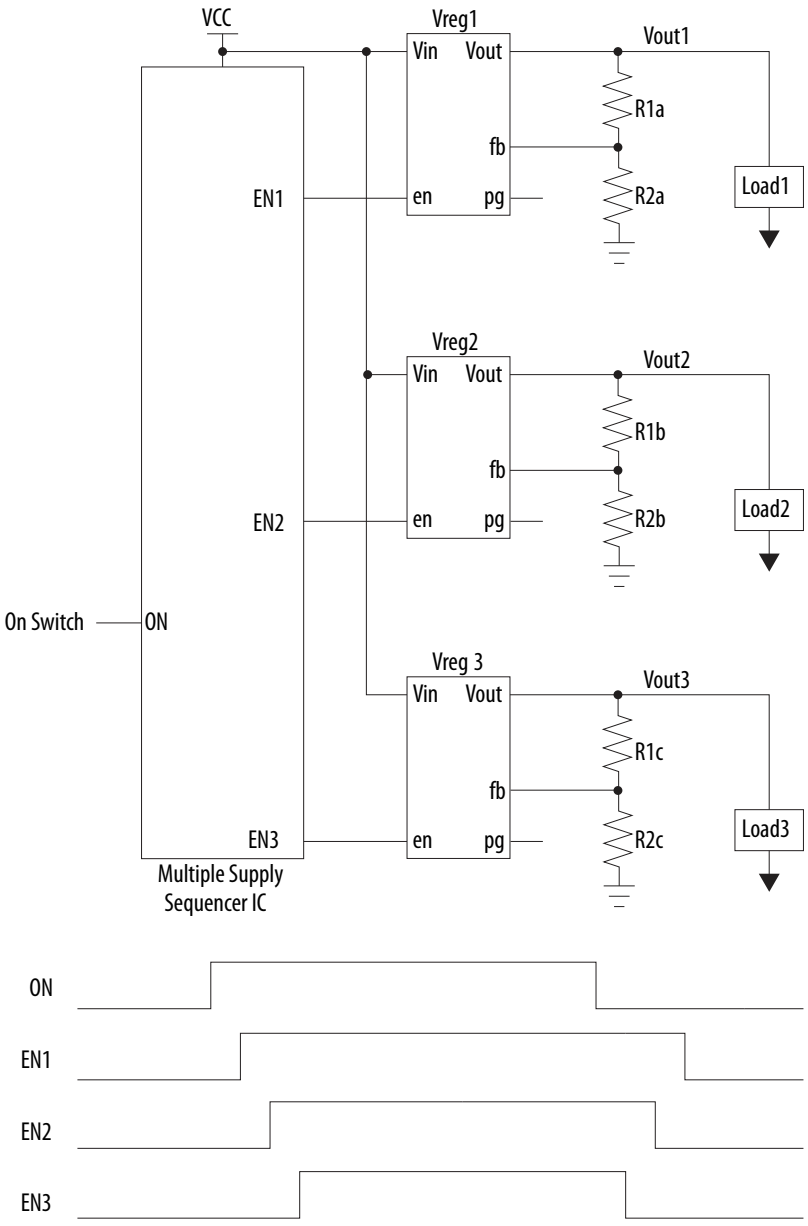
Consult your power module vendor for more information about PPMC.

### 3.1.2. Multiple Supply Sequencer

If only a simple power-up/power-down sequencing is required to follow the Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices power sequencing considerations, a low-cost multiple supply sequencer IC can be used.

These devices offer multiple sequenced output enables that are controlled by a dedicated input. When the input is switched on, the Output Enables (EN1/ EN2 /EN3) turn on in successive order after a programmed time delay. This time delay between the output enables can be adjusted.

**Figure 7. Example Schematic Design of Multiple Supply IC**




Consult your power module vendor for more information about multiple supply sequencer ICs.

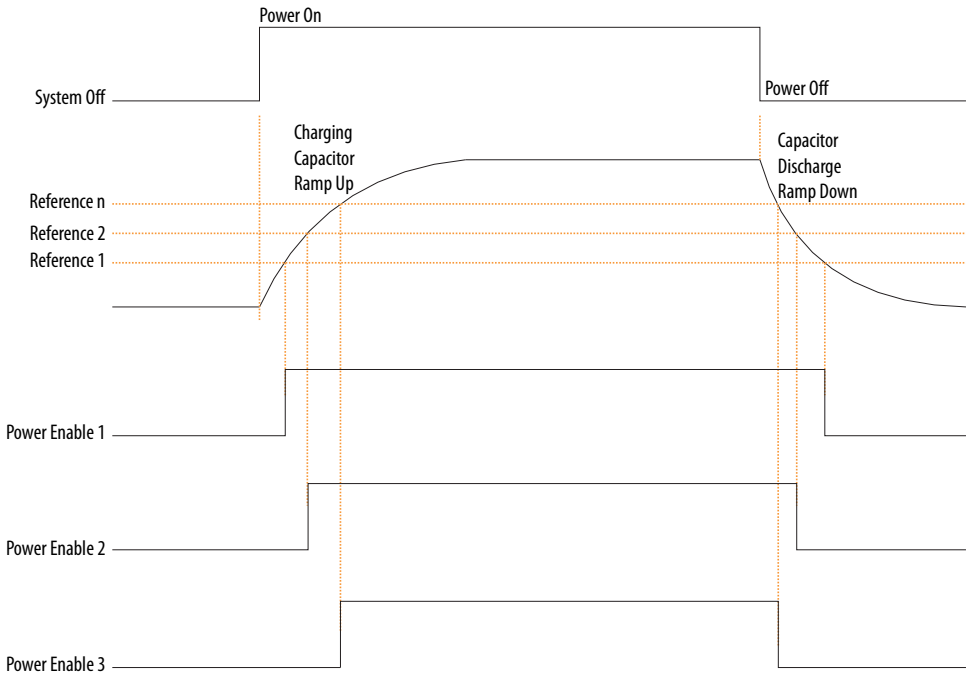
## 3.2. Low-Cost Discrete Sequencer Design

A discrete sequencer design is a low-cost option in which the charging and discharging voltage of a simple resistor-capacitor (RC) network and preset reference voltage levels are used.

The RC ramp-up/down voltage is compared with preset reference voltage levels to generate a series of sequenced power enable outputs to control the voltage regulators.

The power-on event triggers the capacitor charging. As the capacitor voltage rises above each of the preset reference voltage levels, the power enable outputs are sequentially turned on. Similarly, for the power-down event, the discharging of the capacitor causes the power enable outputs to turn off in the reverse sequential order.

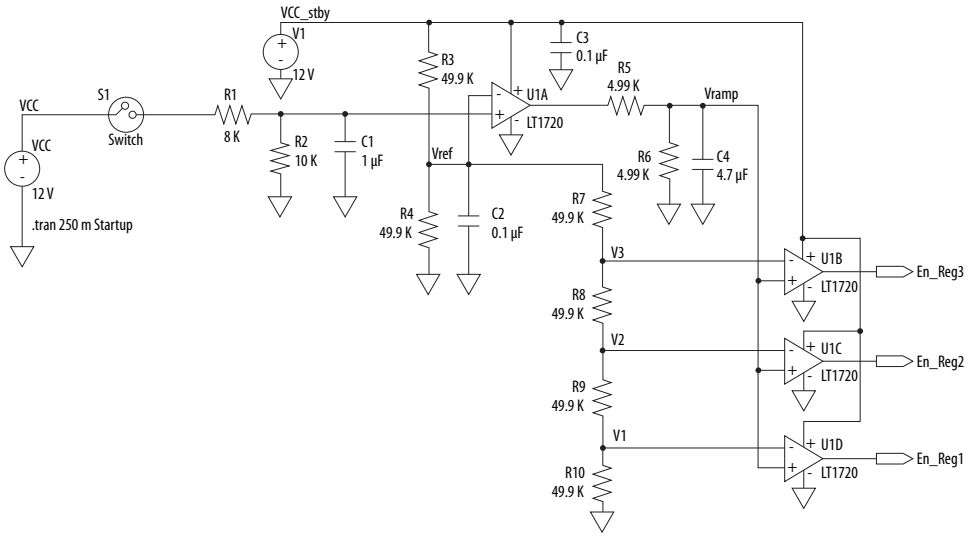
**Figure 8. Power-Up / Power-Down Sequencer**




## 3.2.1. Low-Cost Sequencer Circuit Description

The example design for the simple low-cost power-up/down sequencer uses a quad comparator IC **(U1)** and discrete resistors and capacitors (Recommended Version).

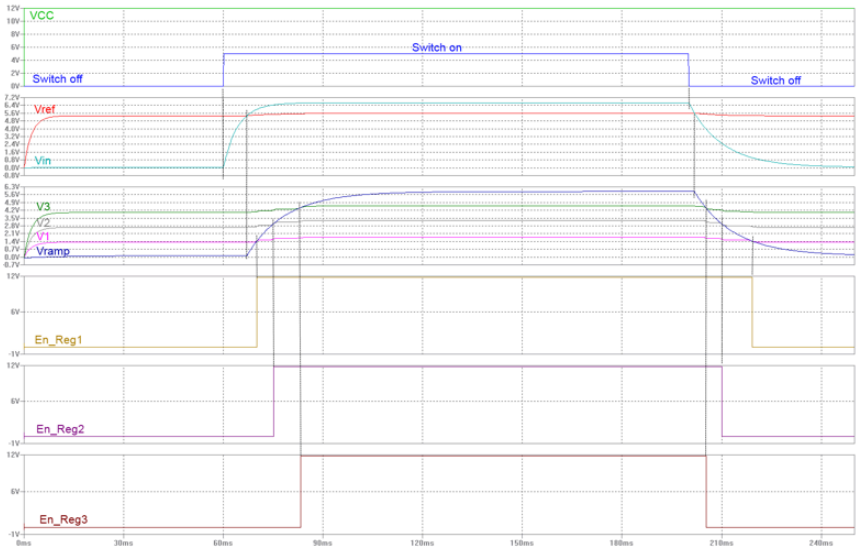
**Figure 9. Low-Cost Sequencer Example Circuit**




A system standby voltage VCC_stby is always present to power the comparator **U1A**. A reference voltage Vref is generated from VCC_stby through resistor dividers **R3** and **R4**. Vref is the reference voltage for the inverting input of comparator **U1A**. A more accurate Vref can be generated using a precision trimmed zener diode in place of resistor **R4**. The resistor ladder network consists of resistors **R7**, **R8**, **R9**, and **R10**. This ladder network further divides the reference voltages V3, V2, and V1. Comparator (**U1B**, **U1C**, and **U1D**) outputs drive the associated regulator enables (En_reg3, En_Reg2, En_Reg1). These outputs turn On/Off the voltage regulators (not shown). Switch **S1** is the system power On/Off switch.

## 3.2.2. Low-Cost Discrete Sequencer Simulation Results

**Figure 10. Circuit Simulation Results for Power-Up and Power-Down Events**



Initially, the power sequencer circuit is not operational because the power switch **S1** is open. As a result, all regulator enables (En_Reg1, En_Reg2, and En_Reg3) are low. As the regulator enables drive the voltage regulators, all voltage regulators are turned off.

### Power ON

- When switch **S1** is closed, the system turns on and the voltage VCC charges the capacitor **C1** to voltage level Vin.
- **C1** is charged through resistor **R1**. Voltage level Vin depends on the values of **R1** and **R2** which form voltage divider and Vin = (R2/(R1+R2))*VCC. **R1** and **R2** are selected such that the value of Vin is slightly higher than comparator **U1A**'s reference voltage Vref.
- When the value of Vin rises above Vref, comparator **U1A**'s output goes high and capacitor **C4** starts charging through resistor **R5**.
- Resistors **R5** and **R6** set the ramp voltage Vramp. Resistor **R5** and capacitor **C4** define the time constant for the ramp rate of Vramp. Vramp is the input voltage to the non-inverting inputs of comparators **U1B**, **U1C**, and **U1D**. As Vramp rises above the voltage references (**V1**, **V2**, and **V3**), it sequentially trips comparators **U1D**, **U1C,** and **U1B**, turning on regulator enables En_Reg1, En_Reg2, and En_Reg3.

### Power OFF

- The order of the power-down sequence is reverse of the power-up sequence.
- When switch **S1** is opened, the system starts shutting down. Capacitor **C1** starts discharging through **R2**. **R2** and **C1** set the decay rate of Vin during the power-down cycle.
- When Vin falls below Vref, comparator **U1A**'s output turns off. This discharges Vramp through the parallel combination of **R5** and **R6**.
- As Vramp discharges below **V3**, **V2**, and **V1**, the comparators **U1B**, **U1C** and **U1D** sequentially turn off their regulator enables.

This example circuit can be easily expanded to support more regulator enable (reg_en) outputs.

To expand the circuit, add more comparators and extend the resistor ladder network to generate additional reference voltage comparison points (for example, **V4**, **V5**, etc). Also, increase the Vramp charging/discharging rate to allow more time between the additional regulator enables. This time delay is controlled by the time constant determined by **R5**, **R6**, and **C4**.

# 4. Fault Tolerance

## 4.1. Managing Uncontrolled Loss of Power Events

Sudden loss of power events such as a utility grid blackout, accidental removal of the system power cable, or other uncontrolled loss of power events can create difficult power management scenarios for the system designer. To manage these types of exceptions with Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices, ensure the power management design incorporates these features:

1. Loss of power detection
2. Hold-up capacitor (if needed) to keep the Power Management Circuitry operational during shutdown
3. Reset logic to the FPGA and system to minimize power consumption during shutdown
4. Rapid discharge circuit for each power group to minimize power-down time

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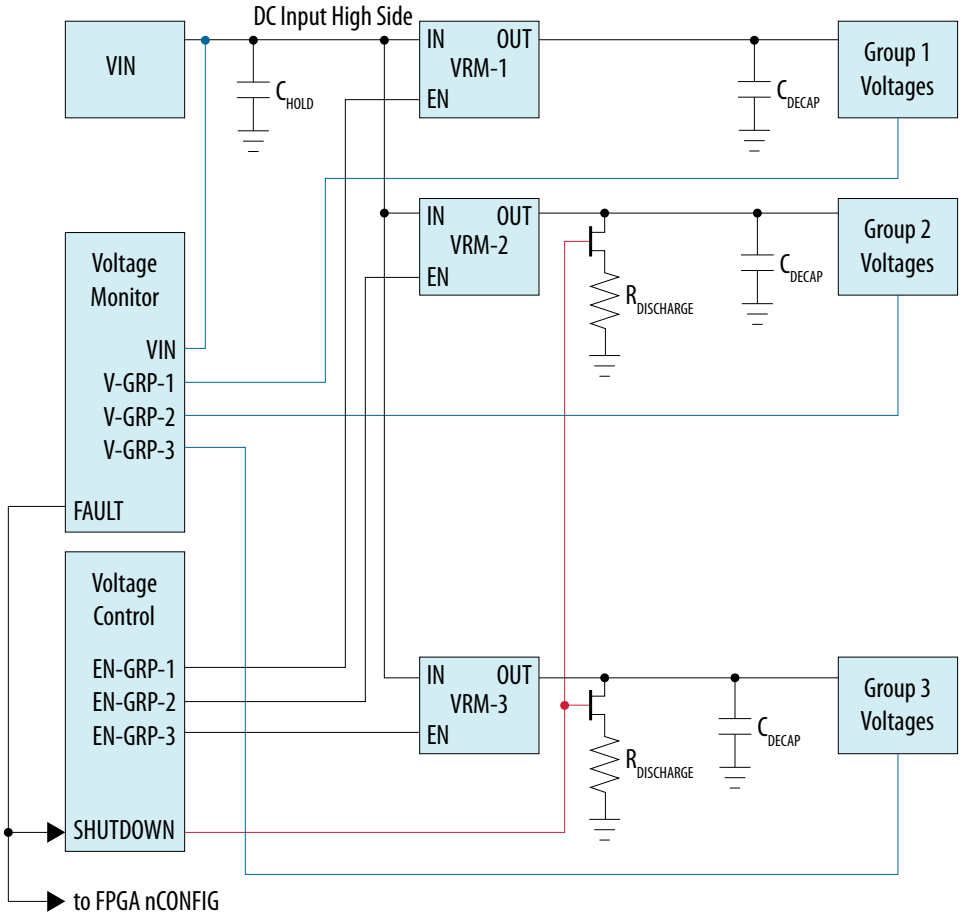
**Figure 11. Fault Tolerant Block Diagram (Required Version)**

The following figure shows a conceptual implementation for managing uncontrolled power loss events.



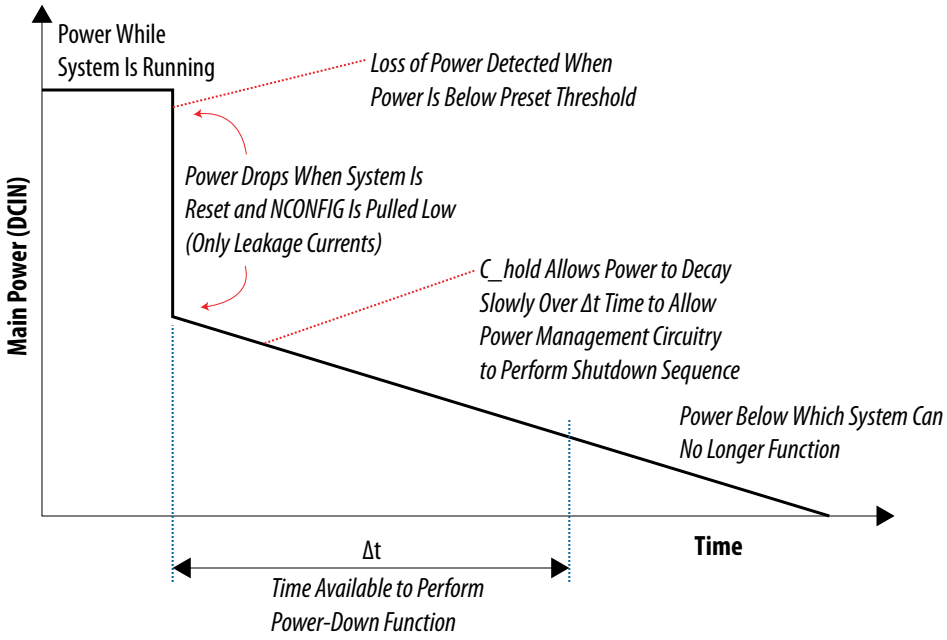

The Power Management Circuit (in the above diagram) is powered directly from the VIN high-side DC input voltage, but can operate down to 5 V. You may need $C_{HOLD}$ to maintain sufficient charge to keep the Power Management Circuitry operational during loss of power events. $C_{DECAP}$ Group 1-3 represents the total decoupling capacitance associated with each power rail grouping. $R_{DISCHARGE}$ 2-3 and its associated power FETs enable fast discharging of each power group voltage to 0 V when you initiate a shutdown sequence. The fast discharging circuit speeds up the power-down cycle of each rail (as the natural RC discharge decay is very slow) and can also define the order in which the rails discharge by trimming $R_{DISCHARGE}$. Without the fast discharge circuit, the shutdown time can be very long, requiring a larger capacitance for $C_{HOLD}$.

## Theory of Operation

While the system is running, the high-side DC input is maintained at VIN +/-10% tolerance. The power loss detection circuit continuously monitors the DC input for a loss of power event. This detection circuit can be a simple comparator with a reference voltage set to a threshold slightly below the -10% threshold, or it can be an Analog-to-Digital Converter (ADC) employing multiple successive samplings to discriminate against false power interruptions.

When a valid loss of power event occurs, the detection circuit generates a reset to the system. The reset signal pulls the FPGAs' NCONFIG signal low to reduce the device's operational current to just its static quiescent value. Concurrently, the Power Management Circuit is triggered to initiate a shutdown sequence. This reduces the value of $C_{HOLD}$ needed to support the Power Management Circuitry during the shutdown process.

**Figure 12. Main Power Loss Detection and Shutdown Event**




The Δt time that the Power Management Circuit has to perform a graceful power-down is dependent on the total power consumption of the system and $C_{HOLD}$ capacitor needed to maintain reliable system power. While the individual power groups are being disabled in reverse sequential order, the FET for each particular group is also successively turned on to facilitate a rapid discharge of their respective power rail to ground through the $R_{DISCHARGE}$ resistors. You must properly size the discharge FET and resistor to handle the instantaneous discharge current through it. The discharge resistor must be able to handle the single pulse power load for the duration of the discharge time. You can determine this from the data sheet of the selected resistor. The data sheet typically provides this data as a graph plotting the *Maximum pulse load power* versus the *Pulse duration* for various resistor package sizes. Determine the value of $C_{HOLD}$ from the energy stored in the capacitor and the total power required to maintain system operation, calculated from the following equations:

$$\text{Power} = \frac{\Delta E}{\Delta t} = \frac{\frac{1}{2} C(v_1^2 - v_2^2)}{(t_1 - t_2)}$$

$$C_{hold} = \frac{2 \times \left( P_{FPGA_{leakage}} + P_{System_{peripherals}} \right) \times (t_1 - t_2)}{\text{Eff} \times (v_1^2 - v_2^2)}$$

E = Energy stored in the capacitor in *Joules*

P = Power in *Watts*

V = Voltage in *Volts*

C = Capacitance in *Farads*

t = Time in *Seconds*

Eff = Efficiency percentage of the regulator

### Example Design

Consider an FPGA system that has total quiescent current of 25 A when the system is under reset (FPGA leakage and total system standby current), and the hold time of the capacitor needs to be 1 ms as the voltage drops from 10 V to 5 V. Also, assume that the voltage rail is 0.9 V.

Determine the $C_{HOLD}$ capacitance required for the Power Management Controller to maintain operation so that you can complete a proper power-down sequence.

From the above equation:

```
C_HOLD   = (2 * 25 A * 0.9 V * .001 s) / (0.85 * (10^2 -5^2))
         = 0.045 / 63.75 µF
         = 706 µF
```

## 4.2. Sequential vs. Simultaneous Power-Down

Some sequencers on the market may simultaneously bring all voltage rails down instead of powering the voltage rails down sequentially.

Take care when selecting a design for controlling the sequence during a fault condition. Non-sequential power-down controllers can violate the power-down specification of the Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices. External active discharge and trimming $R_{DISCHARGE}$ can alleviate this problem (refer to the "Fault Tolerant Block Diagram (Required Version)" in *Managing Uncontrolled Loss of Power Events*).

## 4.3. Voltage Regulators with Clamping Capability

There are voltage regulators on the market that clamp the output to GND in the event of a fault condition. This type of control can be disabled. Group 2 can be clamped only if it is clamped with the same control signal as Group 3. Otherwise, make sure that regulators in Group 1 and Group 2 do not have this option enabled.

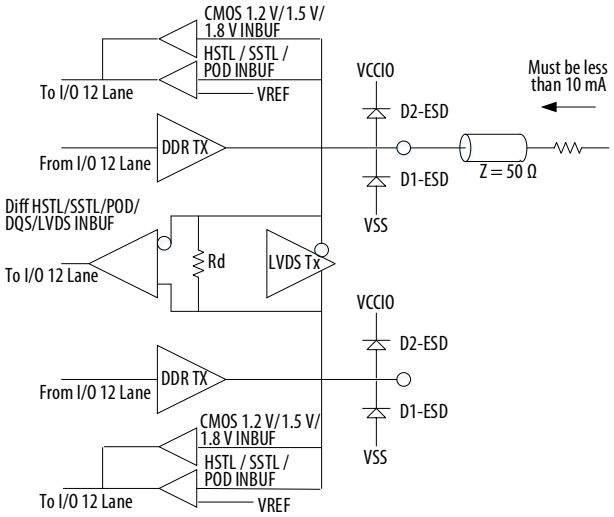
# 5. Driving Unpowered FPGA Pins

## 5.1. LVDS I/O Pin Guidance for Unpowered FPGA

Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 device LVDS I/O pins do not support 'Hot-Socketing;' these LVDS I/O pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per I/O bank. The voltage level must not exceed 1.89 V.

A series resistor can be used to help limit current if necessary. The worst case assumption is that VCCIO is ~0 V. If diode D2 is biased by 1.8 V, impedance into VCCIO is extremely low (refer to the figure below).

**Figure 13. LVDS I/O Banks Buffer Structure**




## 5.2. Transceiver Pin Guidance for Unpowered FPGA

Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 device transceiver pins do not support 'Hot-Socketing.'

Fully configure the transceiver block before driving or having any activity on the Intel Cyclone 10 GX and Intel Arria 10 device transceiver pins.

Intel Stratix 10 device transceiver pins do not support 'Hot-Socketing' although these transceiver pins can tolerate 1.0 Vp-p during power-up or power-down. This applies to L-tile and H-tile devices only.

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# 6. Document Revision History for AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices

| Document Version | Changes |
|---|---|
| 2019.05.20 | Made the following changes:<br>• Updated $V_{CCIO\_UIB}$ power grouping in the *Voltage Rail* table. |
| 2019.03.05 | Made the following changes:<br>• Added E-tile voltage rails and power-up exception to *Power-Up Sequence Requirements*.<br>• Changed **Original Text:** For Intel Cyclone 10 GX and Intel Arria 10 devices, you can combine and ramp up Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as Group 2 power rails VCCIO, VCCPGM, and VCCIO_HPS. to **Updated Text:** For Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 devices, you can combine and ramp up Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as Group 2 power rail VCCPT.<br>• Changed 1.1 Vp-p references to 1.0 Vp-p. |
| 2018.04.13 | Made the following changes:<br>• Deleted the note: To satisfy the power-up requirements, program the FPGA device immediately after the power-up sequence completes.<br>• Added links to *References* and moved it to the beginning. |
| 2018.02.28 | Made the following changes:<br>• Added Intel Cyclone 10 GX device support.<br>• Added "Sequential vs Simultaneous Power-Down."<br>• Added "Voltage Regulators with Clamping Capability."<br>• Added "Driving Unpowered FPGA Pins" - "LVDS I/O Pin Guidance for Unpowered FPGA" and "Transceiver Pin Guidance for Unpowered FPGA."<br>• Removed Hot-Plug support.<br>• Added POR Delay specifications for Intel Cyclone 10 GX and Intel Arria 10. |
| 2017.05.08 | Made the following changes:<br>• Added the following description for power-down sequence for Intel Arria 10 and Intel Stratix 10 devices "For Arria 10 and Stratix 10 devices, when the Group 3 power rails are 1.8V and share the same voltage regulator, then the Group 3 power rails can be combined with Group 2 power rails. In this case, Group 2 and Group 3 power rails can ramp down together." Updated the diagrams accordingly.<br>• Added the following note in "Hot-Plug Challenges" topic: "There are hot socket circuits in every 6-pack to monitor VCC, VCCT and VCCR power level. If any of those power supplies are not at operational level, all PMA outputs and inputs are gated low." |
| 2016.10.31 | Made the following changes:<br>• In the section "Hot Swap Controller and Regulator" updated the description to "When the line card is fully engaged, the card present indicator informs the host that a new card has been successfully inserted. The CONF_DONE signal should then be routed back to the master and sampled as an enable to the signals that are driven. This ensures that configuration is done, the device is stable, and that the master can drive the I/O to the newly powered up slave device without fear of damaging the part. The host system drives the line card's I/O pins and configures it for normal operation."<br>• In the "Hot-Plug Example" section added 2 new diagrams for "Hot-Plug Example using Staggered Pin Length Connectors." |

***continued...***

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| Document Version | Changes |
|---|---|
| 2016.09.20 | Made the following change:<br>• In topic "Power Sequence for Arria 10 and Stratix 10 Devices" for figure "Power-Down Sequence for Arria 10 Devices for combined Group2 and Group3 powers" edited the description to "During the power-up/down sequence, the device output pins are tri-stated. Intel recommends that the input pins should not be driven during this time to ensure long term reliability of the device." |
| 2016.06.16 | Made the following changes:<br>• Added new figures for "Power-Down Sequence for Arria 10 Devices", "Power-Down Sequence for Stratix 10 Devices" and "Power-Down Sequence for Arria 10 Devices for combined Group2 and Group3 powers".<br>• Added the "Power-Up Sequence Considerations for Stratix 10 Devices".<br>• Added a new section for "Managing Uncontrolled Loss of Power Events".<br>• Added a new figure for "Power-Up Sequence for Stratix 10 Devices". |
| 2015.1.02 | Made the following change:<br>• Clarified information in the "Power-Up Sequence for Arria 10 Devices" section. |
| 2013.09.06 | Initial release to MOLSON. |