Implementing Loopback in Triple-Speed Ethernet Designs With LVDS I/O and GX Transceivers

This application note describes two reference designs that demonstrate various types of loopback in a fully operational subsystem. The reference designs are SOPC Builder systems that integrate multiple instances of the Triple-Speed Ethernet MegaCore® functions operating in full-duplex mode with optional loopback paths.

One reference design runs in the Arria® II GX FPGA development board and integrates instances of the Triple-Speed Ethernet IP core with embedded GX blocks. The other reference design runs in the Stratix® IV FPGA development board and integrates instances of the Triple-Speed Ethernet IP core with embedded LVDS IO blocks.

The application note contains the following sections:

- “Features” on page 2—lists the features offered by the reference designs.
- “Architecture” on page 2—describes the components of the reference designs and the loopback paths you can enable.
- “Using the Reference Designs” on page 8—lists the hardware and software requirements, files, and directory structure. This section also includes step-by-step procedures to set up the hardware, and to configure and run the tests.
- “The Benchmark Application” on page 14—describes the application provided with the reference designs and its menu options.
- “Base Addresses and Configuration Registers” on page 21—lists the base addresses of the design components and describes the registers.
- “Interface Signals” on page 25—describes the top-level signals of the reference designs.

For more information on the Triple-Speed Ethernet IP core, refer to the Triple Speed Ethernet User Guide and Chapter 31 Triple Speed Ethernet in the MegaCore IP Library Release Notes and Errata.
Features

The reference designs offer the following features:

- Interface with 10/100/1000BASE-T or 1000BASE-X small form factor pluggable (SFP) modules using the 1.25-Gbps serial interface and SFP high-speed mezzanine connector (HSMC) daughtercard.

- Support the following loopback types in full-duplex mode:
  - Single-port loopback: MAC loopback, transceiver serial loopback, SFP local loopback, HSMC loopback, and stub loopback
  - Dual-port loopback using SFP modules with CAT5/CAT6 Ethernet or 1000BASE-X fiber optic cable assembly
  - MAC and PCS loopback using an external Ethernet packet generator

- Include a benchmark application that provides you with the required drivers and a command-line interface (CLI) to configure and run demonstration tests.

- Allow you to configure test parameters such as total number of packets, packet length, and data type.

- Display test progression that shows the number of packets sent and to be sent as well as the estimated throughput in number of packets per second and the error rate during packet reception.

- Support 10/100/1000-Mbps Ethernet operations in SGMII mode with auto-negotiation.

- Support programmable promiscuous mode; the MAC omits address filtering on receive when promiscuous mode is enabled.

Architecture

The reference designs provide a platform for you to control, test, and monitor different Ethernet operations. These designs include a packet generator that generates Ethernet packets and a packet monitor that receives the packets and verify them.

You have the option to turn on various loopback paths for demonstration and testing purposes. Depending on the loopback path you turn on, you can also choose to use an external packet generator.
Figure 1 shows a high-level block diagram of the reference designs and the loopback paths you can configure.

**Figure 1. Block Diagram**

**Note to Figure 1:**
(1) The red lines and arrows represent the loopback paths. See “Loopback Options” on page 7 for more information on the loopback paths.
Design Components

This section describes the components of the reference designs.

Nios II Processor

The processor sets up and configures the design components based on the commands you type at the CLI. You can also instruct the processor using the CLI to start the packet generation and monitor the status of the packet reception.

On-Chip Memory Core

The on-chip memory is 256 kilobytes (KB) in size and stores the software codes.

JTAG UART Core

This IP core transfers serial character streams between the Nios® II processor and SOPC Builder system. The Nios II processor communicates with the IP core by writing and reading the control and data registers of the IP core through the Avalon Memory-Mapped (Avalon-MM) interface.

PLL core

This IP core takes an input clock from a 100-MHz crystal on the development board and generates an 83.33-MHz PLL output clock. The output clock is used as a system-wide clock source for the SOPC Builder system.

PIO Core

This IP core provides general-purpose I/O ports that connect to the two-wire serial interface (TWSI) of the SFP module. The Nios II software drivers control the IP core. The IP core provides an easy access to the 10/100/1000BASE-T SFP’s external registers using the "bit banging" approach that conforms to the two-wire serial interface protocol.

Interval Timer Core

The Nios II processor uses this 32-bit timer to calculate the performance and throughput rate of various Ethernet operations.

Ethernet Packet Generator

This SOPC Builder custom component generates Ethernet packets in the format shown in Figure 2.

Figure 2. Frame Format


Packets generated do not include the 7-byte preamble and 1-byte start frame delimiter (SFD) fields. For each packet, the generator inserts a running sequence number for debugging purposes and a CRC-32 checksum to ensure data integrity and avoid errors during reception.
The generator has an Avalon Streaming (Avalon-ST) source port through which the packets are streamed out and an Avalon-MM slave port that provides access to the generator’s configuration and status registers. Using the provided benchmark application, you can configure these registers to specify the following:

- Number of packets to generate.
- MAC source and destination addresses—can be unicast, multicast, or broadcast addresses. If you use unicast addresses, set the source address to the address of the transmitting MAC and the destination address to the address of the receiving MAC. This setting ensures that the receiving Ethernet port in the reference designs receives valid packets.
- Packet length—you can specify a fixed or random packet length. A fixed length ranges between 24 to 9600 bytes; a random length ranges between 24 and 1518. The Triple-Speed Ethernet IP core pads undersized packets to meet the minimum required length, 64 bytes.
- Payload—you can specify the data type to be incremental or random. Incremental data starts from zero and gets incremented by one in subsequent packets. Random data is generated from the random seed you specify.
- Random seed—specify the random seed to generate random data.

For more information about the configuration registers and benchmark application, refer to the following sections:

- Configuration registers, “Ethernet Packet Generator Configuration Registers” on page 22.
- How to use the benchmark application, “Running the Benchmark Application” on page 13.

**Ethernet Packet Monitor**

This SOPC Builder custom component verifies the payload of all receive packets, indicates whether or not the packet is valid, and collects statistics about the packet such as the number of bytes received. When the packet monitor receives a packet, it verifies the packet by computing the CRC-32 checksum of the receive packet and verifies it against the CRC-32 checksum field in the packet.

The monitor has an Avalon-ST sink port through which packets are streamed in and an Avalon-MM slave port that provides access to the monitor’s configuration and status registers, and the statistics counters.

The monitor is automatically started each time you start the packet generator; stopped when you interrupt the packet generation.

For more information about the status registers and statistics counters, refer to “Ethernet Packet Monitor Configuration Registers” on page 23.
Ethernet Port 0

This port consists of an instance of the Triple-Speed Ethernet IP core, which is the 10/100/1000-Mbps Ethernet MAC and 1000BASE-X/SGMII PCS variation with an embedded physical medium attachment (PMA). For the Arria II GX design, the PMA uses the GX transceiver; for the Stratix IV GX design, the PMA uses the LVDS IO block.

Figure 1 on page 3 shows the loopback paths that you can exercise within Ethernet Port 0.

Ethernet Port 1

Figure 3 shows the components of Ethernet port 1 and optional loopback paths.

Figure 3. Ethernet Port 1 Components

The following list describes each component of Ethernet port 1:

- Avalon-ST Loopback—an SOPC Builder custom component that multiplexes the data from the Avalon-ST receive interface of the Triple-Speed Ethernet IP core and loops the data back to the Avalon-ST transmit interface. You can also configure this component to swap the source and destination addresses in the packet before the packet is looped back to the transmit interface. The section “Avalon-ST Loopback Configuration Registers” on page 24 describes the configuration registers of this component.

- Triple-Speed Ethernet IP core (Instance 1)—10/100/1000-Mbps Ethernet MAC variation.

- PCS Loopback—an SOPC Builder custom component that forwards Ethernet packets to the downstream component or loops the packet back to the GMII/MII transmit interface. This component contains a clock divider that automatically divides the PCS clock for the GMII/MII depending on the operating speed: 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. This
component also implements a rate adaption FIFO buffer to compensate the parts per million (ppm) difference between the transmit and receive clock. The FIFO buffer keeps track of the ppm difference and determines the required inter-packet gap to compensate the ppm difference. The section “PCS Loopback Configuration Registers” on page 24 describes the configuration registers for this component.

- Triple-Speed Ethernet IP core (Instance 2)—1000BASE-X/SGMII PCS variation with SGMII bridge enabled and an embedded PMA. For the Arria II GX design, the PMA uses the GX transceiver; for the Stratix IV GX design, the PMA uses the LVDS IO block. This component is instantiated using the MegaWizard Plug-in Manager and incorporated in the SOPC Builder system.

**Loopback Options**

You can configure the reference designs to implement the following types of loopback:

- Single-port loopback, Ethernet port 0:
  - a. MAC local loopback (path A in Figure 1 on page 3).
  - b. Transceiver serial loopback (path B in Figure 1 on page 3)—available only in GX transceivers.
  - c. External loopback on the serial interface of Ethernet port 0 using an HSMC loopback card. See path E in Figure 1 on page 3.
  - d. External PHY loopback for 10/100/1000BASE-T Copper SFP. See path G in Figure 1 on page 3. This option is not available for 1000BASE-X Fiber SFP connections.
  - e. Stub loopback using the RJ45 Loopback Stub for BASE-T SFPs for 10/100 Mbps or LC Duplex Fiber Loopback stub for BASE-X SFPs for 1000 Mbps (path F in Figure 1 on page 3), which requires an HSMC daughtercard and SFP module.

- Dual-port loopback, Ethernet port 0 to port 1:
  - External (RX-to-TX) PCS reverse loopback (paths P1 and D in Figure 1 on page 3).
  - External (RX-to-TX) Avalon-ST reverse loopback (paths P1 and C in Figure 1 on page 3).

Dual-port loopback requires an HSMC daughtercard, SFP modules, and fiber or copper Ethernet cable.

- Data path from an External Ethernet Packet Generator to Ethernet Port 1:
  - PCS loopback with external generator (paths P2 and D in Figure 1 on page 3).
  - Avalon-ST loopback with external generator (paths P2 and C in Figure 1 on page 3).
Using the Reference Designs

This section describes the required hardware and software setup.

Hardware and Software Requirements

To run the reference designs, you need the following hardware and software:

- Stratix IV GX FPGA development board with an 8-port SFP HSMC daughtercard by Terasic
- Arria II GX FPGA development board with an 8-port SFP HSMC daughtercard by Terasic
- Altera programming cable
- Two Finisar Active Copper SFP (FCMJ-8521-3) modules
- Two Finisar 1000BASE-X transceiver (FTLF8519P2BCL) modules
- HSMC loopback board (for HSMC loopback only)
- Straight-through CAT5/CAT6 Ethernet cable assembly or LC to LC Multimode Duplex Patch cable
- RJ45 loopback stub or LC Loopback Optical Patch cords
- Quartus® II software version 10.1 SP1
- Nios II EDS version 10.1 SP1
Figure 4 shows the Stratix IV GX FPGA development board and other required hardware.

**Figure 4. Required Hardware**
SFP HSMC Daughtercard

The SFP HSMC daughtercard connects to the development board and provides an interface to the SFP modules. Figure 5 shows the SFP HSMC daughtercard connected to the Arria II GX FPGA development board.

Figure 5. Arria II GX FPGA Development Board and SFP HSMC Daughtercard

The daughtercard has eight SFP connectors; the reference designs use only two connectors:

- SFP 4 and SFP 5 in the Stratix IV GX FPGA development board
- SFP 0 and SFP 1 in the Arria II GX FPGA development board

SFP Modules

The reference designs support the following SFP modules:

- Finisar 1000BASE-X SFP for fiber optic interface and does not require any configuration.
- Finisar 10/100/1000BASE-T SFP for copper interface.

  This SFP module utilizes the TWSI to configure the registers in its internal PHY. The TWSI operates with a bidirectional serial data line and an output serial clock line. To conform to the TWSI protocol, the reference designs use two toggling PIO pins to communicate with the PHY registers, whose base address is 0xAC.

You can configure the Marvell PHY registers of the SFP modules to enable auto-negotiation with a link partner to establish a common Ethernet operating mode. Using the benchmark application, you can set the PHYs to operate in any of the following modes:

- 10BASE-T full-duplex
- 100BASE-T full-duplex
- 1000BASE-T full-duplex
- 1000BASE-X full duplex

For more information about the PHYs of the SFP modules, refer to the *Marvell PHY 88E1111 Datasheet*.

Files and Directory Structure

The files, `tse_loopback_ref_design_for_stratixIV.zip` and `tse_loopback_ref_design_for_arriaII.zip`, contain the reference designs. Unzip the reference design files and you get the directory structure shown in Figure 6.

**Figure 6. Directory Structure**

```
<path>
  app
  demo
  pof
  software
  bsp
  tse_loopback_ref_design
```

- Working directory where the reference design zip files reside.
- tse_loopback_ref_design
  - Contains reference design files.
    - demo
      - Contains the .sof, .cdf, and .elf files for running the application.
    - pof
      - Contains the .pof files for the PFL and FLASH programmer.
    - tse_loopback_ref_design
      - Contains the Quartus II project.
    - software
      - Contains the Nios II software and scripts.
    - bsp
      - Contains the application library files.

Setting Up the Development Boards

Follow these steps to set up the development board:

1. To perform the HSMC loopback on the FPGA physical I/O, connect the HSMC loopback board to the HSMC port A on the development board. Go to step 3.

2. To perform other types of loopback, follow these steps:
   a. Connect the SFP HSMC daughtercard to HSMC port A on the development board.
   b. Insert the SFP modules of your choice into the following SFP connectors:
      - SFP0 and SFP1 on the daughtercard connected to the Arria II GX FPGA development board
      - SFP4 and SFP5 on the daughtercard connected to the Stratix IV GX FPGA development board
Both SFP modules must be either 10/100/1000BASE-T or 1000BASE-X.

Figure 7 shows the SFP connectors in the daughtercard.

**Figure 7. SFP Connectors**

- Depending on the loopback type you want to implement, connect the following items:
  - Standard CAT5/CAT6 RJ45 Ethernet cable for copper interface or LC-to-LC Multimode fiber optic cable to implement dual-port loopback
  - RJ45 Loopback Stub for BASE-T SFPs or LC Duplex Fiber Loopback stub for BASE-X SFPs

3. Connect the programming cable to the JTAG connection port:
   - J6 on the Arria II GX FPGA development board
   - J7 on the Stratix IV GX FPGA development board
4. Connect the power adapter to J4 on the development board.
5. Toggle the power switch (SW1) on the development board to supply the board with power.

**Configuring the Development Boards**

Follow these steps to configure the development boards with the hardware image of the reference designs:

1. Open a Nios II command shell. On Windows platform, click Start menu > All Programs > Altera > Nios II EDS > Nios II Command Shell.
2. In the command shell, change directory to `<path>/tse_loopback_ref_design/demo`, where `tse_ref_design_top.cdf` and `tse_ref_design_top.sof` reside.

3. Type the following command:

   nios2-configure-sof tse_ref_design_top.sof

   Figure 8 displays upon successful completion of the command.

### Figure 8. SOF Download

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**Running the Benchmark Application**

Follow these steps to run the benchmark application:

1. In the Nios II command shell, ensure that you are in the `<path>/tse_loopback_ref_design/demo` directory.

2. Type the following command in the command shell to download the pre-compiled benchmark application to the system memory:

   nios2-download -g tse_loopback_benchmark_app.elf ; nios2-terminal

   If you have more than one programming cable installed, type the following command:

   nios2-download --cable=<number> -g tse_loopback_benchmark_app.elf
   nios2-terminal --cable=<number>

   You can use the `--list` option to display a list of available hardware; the `-h` option for more information about the Nios II downloader and terminal.

   The command downloads the image file of the Nios II processor to the system memory and subsequently restarts the processor to begin code execution. An additional terminal starts running and you can use this terminal to interact with the benchmark application.

   The Test Menu (Figure 9 on page 14) appears when the benchmark application successfully starts.
The Benchmark Application

You can use this application to configure and run benchmark tests on the reference designs. This application provides the following menus:

- **Test Menu**—options for you to configure test parameters and run a test.
- **TSE Menu**—options for you to set the address and loopback options.
- **Report Menu**—options for you to view reports on the test results.

From these menus, you select an option by typing the option number followed by the input value for the option and press \( \rightarrow \). For user-defined inputs such as packet length, you can enter the inputs in hexadecimal (for example 0x1000) or decimal (for example 4000).

**Test Menu**

Figure 9 shows the Test Menu.

Test Menu provides the following options:

- **Technologies options**—select 10/100/1000BASE-T SGMII or 1000BASE-X SFP module.
- **Link Speed**—select one of the following: **10, 100** or **1000**. For 1000BASE-X, **1000** is automatically selected.

- **Link Configuration**—the reference designs only support full duplex.

- **Packet length**—select **64, 1518, 9600, random** or **user specified**. If you select **user specified**, enter a value between 64 to 9600 bytes. A random length can be between 24 to 1518 bytes.

- **Number of Packets**—select a value that represents the total number of packets to generate. For a user-specified value, enter a number between 1 and **(2^{32}-1)**, inclusive.

- **Packet Data**—select **increment** or **random**. The payload is a 32-bit unsigned integer. If you select **increment**, the payload starts at zero and is incremented by one in each subsequent byte. The value rolls over to zero when it reaches **(2^{32}-1)**. If you select **random**, the payload is set to a new pseudo-random integer in each packet. You can choose to use a predefined random generator seed (PRBS) value or specify your own in the next option.

- **Random Generator Seed Value**—enter the initial random seed for the PRBS generator. This option applies only when you set the **Packet Data** option to **random**.

- **Test Control**—starts the test. When started, the test runs until the total number of packets specified in the **Number of Packets** option are generated and transmitted. You can interrupt and stop the test by pressing **Enter**. When the test stops, the Report Menu displays together with the results.

- **Other Menu**—use this option to switch to the TSE Menu or Report Menu.
TSE Menu

Figure 10 shows the TSE Menu.

**Figure 10. TSE Menu**

The TSE menu provides the following options:

- **TSE Sender MAC Address**—48-bit MAC source address. It can be a unicast, multicast, or broadcast address. The default source address is 0xEE1122334450.

- **TSE Receiver MAC Address**—48-bit MAC destination address. It can be a unicast, multicast, or broadcast address. The default destination address used is 0xEE1122334450.

If you choose not to exercise any of the loopback paths, ensure that the destination address does not conflict with any addresses in the network. If you turn on single-port loopback, ensure that you either set the source and destination addresses to the address of the transmitting MAC or enable promiscuous mode. If you turn on dual-port loopback, set the source address to the address of the transmitting MAC and the destination address to the address of the receiving MAC. Address swapping in the Avalon-ST Loopback module is turned on by default.

- **MAC Promiscuous Mode Option**—use this option to enable promiscuous mode. When you enable promiscuous mode, the MAC omits address filtering on receive. Promiscuous mode is disabled by default.

- **Loopback Options**—select one of the following loopback types:
  - **MAC Local Loopback**—single-port loopback on the MII/GMII within Ethernet port 0. See path A in Figure 1 on page 3.
  - **Transceiver Serial Loopback**—single-port serial loopback within the GX transceiver in Ethernet port 0. See path B in Figure 1 on page 3.
■ **External Loopback Option**—loopback path that interfaces with external components such as HSMC loopback card and dual-port loopback types. See path P1 and P2 in Figure 1 on page 3.

■ **No loopback**—when selected, you can use the reference design to transmit packets to an external test equipment or network.

■ **External Loopback Option**—available only when you set **Loopback Options** to **External Loopback**. Select one of the following external loopback types:

■ **HSMC Loopback**—packets are looped back on the GX transceiver or LVDS IO pins in the HSMC loopback board. See path G in Figure 1 on page 3

■ **Loopback Stub**—packets are looped back using the external SFP modules using a stub; RJ45 Loopback Stub for Copper SFPs or LC Duplex Fiber Loopback stub for Fiber SFPs. See path F in Figure 1 on page 3.

■ **Two Port Loopback**—packets from Ethernet port 0 is sent to Ethernet port 1 and looped back to Ethernet port 0 using a cable assembly. See path P1 in Figure 1 on page 3.

■ **Two Port Loopback Options**—available only when you set **External Loopback Option** to **Two Port Loopback**. Select one of the following options:

■ **Port 1 MAC RX to TX**—the Avalon-ST module in Ethernet port 1 swaps the source and destination addresses of the receive packet and loops it back to Ethernet port 0. See path C in Figure 1 on page 3.

■ **Port 1 PCS RX to TX**—the PCS loopback module in Ethernet port 1 loops back the receive packet on the GMII/MII to Ethernet port 0. See path D in Figure 1 on page 3.

■ **Other Menus**—use this option to switch to the Test Menu or Report Menu.
Report Menu

Figure 11 shows the Report Menu.

The Report Menu displays the following information:

- Number—the running test number, starting from one, assigned to each test.
- Status—the test status, completed, interrupted, error or as displayed on the screen.
- TSE Sender MAC—the MAC source address.
- TSE Receiver MAC—the MAC destination address.
- Link Speed—10, 100, or 1000 Mbps and the operation mode, full duplex.
- Packets to Send—the total number of packets to be sent by the Ethernet Packet Generator, packet length and data type. For random data, the option also displays the seed value.
- Packets Sent—the actual number of packets sent by the Ethernet Packet Generator.
- Packets Received—the total number of packets received by the Ethernet Packet Monitor, and the number of valid and errored packets. The total number of packets received is the sum of valid and errored packets.
- Bytes Received—the total number of bytes, packet header and payload, received by the Ethernet Packet Monitor and the throughput rate in bits per second.

The Report Control option allows you to view previous test reports. Select next and prev to scroll through the reports, or enter the test number to go to a specific test report. The benchmark application can store up to nine test reports.
Test Progression Display

When you trigger a test, the benchmark application displays the progression of the test, which includes the number of packets sent, the number of remaining packets to be sent, and the estimated throughput.

Figure 12 shows an example of the test progression information displayed by the application. The arrow above each line represents the number of packets sent. The right margin shows the status of the test. The application also displays the estimated throughput rate, number of packets per second.

The Ethernet Packet Monitor uses a cycle counter register to keep track of the test duration. The monitor initializes the cycle counter to zero and starts incrementing the counter as soon as the first packet is received at the rate of the system clock. The monitor stops the counter when all packets are received or when the test is stopped.

The monitor computes the test duration by dividing the value of the cycle counter by the frequency of the system clock using floating point operations. Although this method of calculation is very accurate, it depends on the reception of the first and the last packet to start and stop the cycle counter respectively. In the absence of these events, or if a major error occurs, the reported duration can be inaccurate.

Tutorial: Running Dual-Port Loopback

This tutorial shows you how to configure a test that exercises the dual-port loopback path, Port 1 MAC RX to TX, using a 1000-Mbps full-duplex 10/100/1000BASE-T link. The total number of packets to send is 500,000 packets and each packet is 1000 bytes long.
To configure the test, type the following commands at the command line:

1. To configure the **Technology Option** to **10/100/1000BASE-T (SGMII)**, type `1a`.
2. To configure the **Link Speed** to **1000 Mbps**, type `2c`.
3. To configure the **Packet Length** to 1,000 bytes, type `4e 1000`.
4. To configure the **Number Packets** to 500,000 bytes, type `5d 500000`.
5. To configure the loopback option to dual-port loopback, switch to the TSE Menu by typing `8b`.
6. To set the **TSE Sender MAC Address** to 0xEE22334460, one of the predefined addresses, type `1b`.
   
   If you are using unicast addresses, set the MAC source address to the address of the transmitting MAC and the MAC destination address to the address of the receiving MAC. For single-port loopback, set the MAC source and destination addresses to the same address, the address of the transmitting MAC, or enable promiscuous mode.

7. To set the **TSE Receiver MAC Address** to 0xEE1122334450, one of the predefined addresses, type `2a`.
8. To enable promiscuous mode, type `3b`.
9. To configure the external loopback to dual-port loopback:
   a. Select **External Loopback Option** by typing `4c`. The External Loopback options display.
   b. Type `5d` to enable **Two-Port Loopback**. The Two-Port Loopback options display.
   c. Type `6a` to select **Port 1 MAC RX to TX**.
10. To run the test:
    a. Switch to the Test Menu by typing `7a`.
    b. Type `7a` to start the test.
    
    The test starts running and the test progression displays.
11. When the test completes, the Report Menu and test results display. See **Figure 11**.
12. To configure and run a new test, switch to the Test Menu by typing `2a`. You can also rerun the same test by typing `7a`. 
Table 1 lists the base address for each component in the reference designs. To access the configuration registers of these components, use the base address of the component and the register offset.

Table 1. Base Addresses of Reference Design Components

<table>
<thead>
<tr>
<th>Base Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000800</td>
<td>cpu_0</td>
<td>Nios II processor</td>
</tr>
<tr>
<td>0x00040000</td>
<td>onchip_mem</td>
<td>On-Chip Memory core, 256 KB on-chip memory storage</td>
</tr>
<tr>
<td>0x00001900</td>
<td>jtag_uart</td>
<td>JTAG UART core</td>
</tr>
<tr>
<td>0x00001A80</td>
<td>pll</td>
<td>Phased-locked loop core</td>
</tr>
<tr>
<td>0x00001B20</td>
<td>pio</td>
<td>PIO core, TWSI serial clock (SCL) 0</td>
</tr>
<tr>
<td>0x00001B30</td>
<td>pio_1</td>
<td>PIO core, TWSI serial data line (SDA) 0</td>
</tr>
<tr>
<td>0x00001B40</td>
<td>pio_2</td>
<td>PIO core, TWSI SCL 1</td>
</tr>
<tr>
<td>0x00001B50</td>
<td>pio_3</td>
<td>PIO core, TWSI SDA 1</td>
</tr>
<tr>
<td>0x00001A00</td>
<td>eth_gen_0</td>
<td>Ethernet packet generator</td>
</tr>
<tr>
<td>0x00001000</td>
<td>triple_speed_ethernet_0</td>
<td>Triple-Speed Ethernet instance 0, 10/100/1000-Mbps and 1000BASE-X/SGMII PCS with embedded PMA.</td>
</tr>
<tr>
<td>0x00001AA0</td>
<td>eth_mon_0</td>
<td>Ethernet packet monitor</td>
</tr>
<tr>
<td>0x00001AE0</td>
<td>timer</td>
<td>Interval Timer core</td>
</tr>
<tr>
<td>0x00001B00</td>
<td>timer_1</td>
<td>Interval Timer core</td>
</tr>
<tr>
<td>0x00000400</td>
<td>triple_speed_ethernet_1</td>
<td>Triple-Speed Ethernet instance 1, 10/100/1000-Mbps MAC</td>
</tr>
<tr>
<td>0x00000200</td>
<td>pcs_loopback_wrapper_0</td>
<td>PCS loopback module</td>
</tr>
<tr>
<td>0x00002000</td>
<td>sgmi_pcs_0</td>
<td>Triple-Speed Ethernet instance 2, SGMII PCS with embedded PMA</td>
</tr>
<tr>
<td>0x00000400</td>
<td>avalon_st_loopback_wrapper_0</td>
<td>Avalon-ST loopback module</td>
</tr>
</tbody>
</table>

Subsequent sections describe the following configuration registers:

- “Ethernet Packet Generator Configuration Registers” on page 22
- “Ethernet Packet Monitor Configuration Registers” on page 23
- “PCS Loopback Configuration Registers” on page 24
- “Avalon-ST Loopback Configuration Registers” on page 24

For more information on the Triple-Speed Ethernet configuration registers, refer to the

*Triple Speed Ethernet User Guide.*
Ethernet Packet Generator Configuration Registers

Table 2 describes the configuration registers of the Ethernet packet generator.

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Name</th>
<th>Bit Number</th>
<th>Bit Name</th>
<th>R/W</th>
<th>H/W Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>number_packet</td>
<td>31:0</td>
<td>—</td>
<td>RW</td>
<td>0x0</td>
<td>Specifies the total number of packets to be generated. Maximum number is $2^{32}$.</td>
</tr>
<tr>
<td>0x04</td>
<td>configuration</td>
<td>0</td>
<td>LENGTH_SEL</td>
<td>RW</td>
<td>0x0</td>
<td>0: Fixed packet length 1: Random packet length</td>
</tr>
<tr>
<td></td>
<td>configuration</td>
<td>14:1</td>
<td>PKT_LENGTH</td>
<td>RW</td>
<td>0x0</td>
<td>Specifies the packet length. Valid values are between 24 to 9600. Applicable only when bit 0 of this register is set to 0.</td>
</tr>
<tr>
<td></td>
<td>configuration</td>
<td>15</td>
<td>PATTERN_SEL</td>
<td>RW</td>
<td>0x0</td>
<td>Specifies the data pattern. 0: Incremental. Data starts from zero and is incremented by 1 in subsequent bytes. 1: Random.</td>
</tr>
<tr>
<td></td>
<td>configuration</td>
<td>31:16</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0x08</td>
<td>rand_seed0</td>
<td>31:0</td>
<td>—</td>
<td>RW</td>
<td>0x0</td>
<td>The lower 32 bits of the random seed. Occupies bits 31:0 of the PRBS generator when the data pattern is set to random (bit 15 of the configuration register).</td>
</tr>
<tr>
<td>0x0C</td>
<td>rand_seed1</td>
<td>15:0</td>
<td>—</td>
<td>RW</td>
<td>0x0</td>
<td>The upper 16 bits of the random seed. Occupies bits 47:32 of the PRBS generator when the data pattern is set to random (bit 15 of the configuration register).</td>
</tr>
<tr>
<td></td>
<td>rand_seed1</td>
<td>31:16</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0x10</td>
<td>source_addr0</td>
<td>31:0</td>
<td>—</td>
<td>RW</td>
<td>0x0</td>
<td>6-byte MAC address.</td>
</tr>
<tr>
<td>0x14</td>
<td>source_addr1</td>
<td>31:0</td>
<td>—</td>
<td>RW</td>
<td>0x0</td>
<td>■ source/destination_addr = Last four bytes of the address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ Bits 0 to 15 of source/destination_addr = First two bytes of the address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ Bits 16 to 31 of source/destination_addr are unused.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For example, if the source MAC address is 00-1C-23-17-4A-CB, the following assignments are made: source_addr0 = 0x17231C00 source_addr1 = 0x0000CB4A</td>
</tr>
<tr>
<td>0x18</td>
<td>destination_addr0</td>
<td>31:0</td>
<td>—</td>
<td>RW</td>
<td>0x0</td>
<td></td>
</tr>
<tr>
<td>0x1C</td>
<td>destination_addr1</td>
<td>31:0</td>
<td>—</td>
<td>RW</td>
<td>0x0</td>
<td></td>
</tr>
</tbody>
</table>
### Ethernet Packet Monitor Configuration Registers

Table 3 describes the configuration registers of the Ethernet packet monitor.

#### Table 3. Ethernet Packet Monitor Configuration Registers (Part 1 of 2)

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Name</th>
<th>Bit Number</th>
<th>Bit Name</th>
<th>R/W</th>
<th>H/W Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>number_packet</td>
<td>31:0</td>
<td>—</td>
<td>RO</td>
<td>0x0</td>
<td>Total number of packets the monitor is expected to receive.</td>
</tr>
<tr>
<td>0x04</td>
<td>packet_rx_ok</td>
<td>31:0</td>
<td>—</td>
<td>RO</td>
<td>0x0</td>
<td>Total number of good packets received.</td>
</tr>
<tr>
<td>0x08</td>
<td>packet_rx_error</td>
<td>31:0</td>
<td>—</td>
<td>RO</td>
<td>0x0</td>
<td>Total number of packets received with error.</td>
</tr>
<tr>
<td>0x0C</td>
<td>byte_rx_count_0</td>
<td>31:0</td>
<td>—</td>
<td>RO</td>
<td>0x0</td>
<td>64-bit counter that keeps track of the total number of bytes received. The byte_rx_count_0 register represents the lower 32 bits, byte_rx_count_1 represents the upper 32 bits. Read byte_rx_count_0 followed by byte_rx_count_1 in the subsequent cycle to get an accurate count.</td>
</tr>
<tr>
<td>0x10</td>
<td>byte_rx_count_1</td>
<td>31:0</td>
<td>—</td>
<td>RO</td>
<td>0x0</td>
<td>64-bit counter that keeps track of the total number of cycles the monitor takes to receive all packets. The cycle_rx_count_0 register represents the lower 32 bits, cycle_rx_count_1 represents the upper 32 bits. Read byte_rx_count_0 followed by byte_rx_count_1 in the subsequent cycle to get an accurate count.</td>
</tr>
<tr>
<td>0x14</td>
<td>cycle_rx_count_0</td>
<td>31:0</td>
<td>—</td>
<td>RO</td>
<td>0x0</td>
<td>64-bit counter that keeps track of the total number of cycles the monitor takes to receive all packets. The cycle_rx_count_0 register represents the lower 32 bits, cycle_rx_count_1 represents the upper 32 bits. Read byte_rx_count_0 followed by byte_rx_count_1 in the subsequent cycle to get an accurate count.</td>
</tr>
<tr>
<td>0x18</td>
<td>cycle_rx_count_1</td>
<td>31:0</td>
<td>—</td>
<td>RO</td>
<td>0x0</td>
<td>64-bit counter that keeps track of the total number of cycles the monitor takes to receive all packets. The cycle_rx_count_0 register represents the lower 32 bits, cycle_rx_count_1 represents the upper 32 bits. Read byte_rx_count_0 followed by byte_rx_count_1 in the subsequent cycle to get an accurate count.</td>
</tr>
</tbody>
</table>
### Table 3. Ethernet Packet Monitor Configuration Registers (Part 2 of 2)

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Name</th>
<th>Bit Number</th>
<th>Bit Name</th>
<th>R/W</th>
<th>H/W Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1C</td>
<td>rx_control_status</td>
<td>0</td>
<td>START</td>
<td>RW</td>
<td>0x0</td>
<td>Set this bit to 1 to start packet reception. This bit clears when packet reception starts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>STOP</td>
<td>RW</td>
<td>0x0</td>
<td>Set this bit to 1 to stop packet reception. This bit clears each time packet reception starts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>RX_DONE</td>
<td>RO</td>
<td>0x0</td>
<td>A value of 1 indicates that the packet monitor has received the total number of packets specified in the number_packet register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>CRCBAD</td>
<td>RO</td>
<td>0x0</td>
<td>A value of 1 indicates CRC error in the current packet received by the monitor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>9:4</td>
<td>RX_ERR</td>
<td>RO</td>
<td>0x0</td>
<td>Receive error status. The rx_err[] signal of the Triple-Speed Ethernet IP core is mapped to this register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>31:10</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

### PCS Loopback Configuration Registers

Table 4 describes the configuration registers of the PCS loopback component.

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Name</th>
<th>Bit Number</th>
<th>Bit Name</th>
<th>R/W</th>
<th>H/W Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>configuration</td>
<td>0</td>
<td>PCS_LOOPBACK_ENA</td>
<td>RW</td>
<td>0x0</td>
<td>0: Disables PCS loopback path. 1: Enables PCS loopback path.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15:1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0x02</td>
<td>interface_disable</td>
<td>0</td>
<td>MAC_IF_DIS</td>
<td>RW</td>
<td>0x0</td>
<td>0: Enables the MII/GMII. 1: Disables the MII/GMII</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15:1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

### Avalon-ST Loopback Configuration Registers

Table 5 describes the configuration registers of the Avalon-ST loopback component.

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Name</th>
<th>Bit Number</th>
<th>Bit Name</th>
<th>R/W</th>
<th>H/W Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>configuration</td>
<td>0</td>
<td>AVALON_ST_LOOPBACK_ENA</td>
<td>RW</td>
<td>0x1</td>
<td>0: Disables the loopback path. 1: Enables the loopback path.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15:2</td>
<td>SRC_DST_ADDR_SWAP</td>
<td>RW</td>
<td>0x1</td>
<td>0: Disables address swapping. 1: Enables address swapping. The source and destination addresses are swapped before the receive packet is looped back to the transmit path.</td>
</tr>
</tbody>
</table>
Interface Signals

This section describes the top-level signals of the reference designs.

Clock and Reset Signals

Table 6 describes the clock and reset signals.

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>I</td>
<td>100-MHz reference clock. Connect this clock signal to the LVDS IO pin AV22/AW22 on the Stratix IV GX FPGA development board, or AJ19/AK19 on the Arria II GX FPGA development board.</td>
</tr>
<tr>
<td>ref_clk_to_the_triple_speed_ethernet</td>
<td>I</td>
<td>125-MHz reference clock for the transceiver. Connect this clock signal to the LVDS IO pin J2 on the Stratix IV GX FPGA development board, or the F18/F17 pin on the Arria II GX FPGA development board.</td>
</tr>
<tr>
<td>reset_n</td>
<td>I</td>
<td>Single reset signal for all logic in the reference design. Connect this reset signal to the USER_PB1 (S4) switch on the Stratix IV GX FPGA development board, or the CPU_RESET (PB3) switch on the Arria II GX FPGA development board.</td>
</tr>
</tbody>
</table>

Triple-Speed Ethernet Instance 0 Signals

Table 7 describes the signals of the Triple-Speed Ethernet instance 0.

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>rxp_to_the_triple_speed_ethernet_0</td>
<td>I</td>
<td>Serial differential receive interface. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 90/92, which corresponds to port 4 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 30/32, which corresponds to port 0 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
<tr>
<td>txp_to_the_triple_speed_ethernet_0</td>
<td>O</td>
<td>Serial differential transmit interface. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 89/91, which corresponds to port 4 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 29/31, which corresponds to port 0 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
<tr>
<td>led_an_from_the_triple_speed_ethernet_0</td>
<td>O</td>
<td>Auto-negotiation status. Connect this signal to USR_LED1 in the Stratix IV GX FPGA or Arria II GX FPGA development board.</td>
</tr>
<tr>
<td>led_link_from_the_triple_speed_ethernet_0</td>
<td>O</td>
<td>Link synchronization status. Connect this signal to USR_LED0 in the Stratix IV GX FPGA or Arria II GX FPGA development board.</td>
</tr>
<tr>
<td>led_col_from_the_triple_speed_ethernet_0</td>
<td>O</td>
<td>Collision detection during frame transmission. Connect this signal to USR_LED2 in the Stratix IV GX development board. Leave this signal unassigned in the Arria II GX FPGA development board.</td>
</tr>
<tr>
<td>led_crs_from_the_triple_speed_ethernet_0</td>
<td>O</td>
<td>Carrier Sense on transmit and receive path. It is connected to USR_LED3 in Stratix IV GX Development Board. It is not assigned in Arria II GX Development Board.</td>
</tr>
</tbody>
</table>
**Triple-Speed Ethernet Instance 1 Signals**

Table 8 describes the signals of the Triple-Speed Ethernet instance 1.

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>rxp_to_the_triple_speed_ethernet_1</td>
<td>I</td>
<td>Serial differential receive interface. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 114/116, which corresponds to port 5 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 26/28, which corresponds to port 1 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
<tr>
<td>bxp_to_the_triple_speed_ethernet_1</td>
<td>O</td>
<td>Serial differential transmit interface. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 113/115, which corresponds to port 5 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 25/27, which corresponds to port 1 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
<tr>
<td>led_an_from_the_triple_speed_ethernet_1</td>
<td>O</td>
<td>Auto-negotiation status. Connect this signal to USR_LED5 in the Stratix IV GX FPGA development board or USR_LED3 in the Arria II GX FPGA development board.</td>
</tr>
<tr>
<td>led_link_from_the_triple_speed_ethernet_1</td>
<td>O</td>
<td>Link synchronization status. Connect this signal to USR_LED4 in the Stratix IV GX FPGA development board or USR_LED2 in the Arria II GX FPGA development board.</td>
</tr>
<tr>
<td>led_col_from_the_triple_speed_ethernet_1</td>
<td>O</td>
<td>Collision detection during frame transmission. Connect this signal to USR_LED6 in the Stratix IV GX development board. Leave this signal unassigned in the Arria II GX FPGA development board.</td>
</tr>
<tr>
<td>led_crs_from_the_triple_speed_ethernet_1</td>
<td>O</td>
<td>Carrier Sense on transmit and receive path. It is connected to USR_LED7 in Stratix IV GX development board. It is not assigned in Arria II GX development board.</td>
</tr>
</tbody>
</table>

**SFP Signals**

Table 9 describes the signals of the SFP module.

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>out_port_from_the_pio</td>
<td>O</td>
<td>SFP serial clock line for Ethernet port 0. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 102, which corresponds to port 4 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 83, which corresponds to port 0 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
<tr>
<td>bidir_port_to_and_from_the_pio_1</td>
<td>I</td>
<td>SFP serial data line for Ethernet port 0. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 101, which corresponds to port 4 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 80, which corresponds to port 0 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
</tbody>
</table>
Table 9. SFP Signals (Part 2 of 2)

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>out_port_from_the_pio_2</td>
<td>0</td>
<td>SFP serial clock line for Ethernet port 1. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 119, which corresponds to port 5 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 72, which corresponds to port 1 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
<tr>
<td>bidir_port_to_and_from_the_pio_3</td>
<td>0</td>
<td>SFP serial data line for Ethernet port 1. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 110, which corresponds to port 5 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 71, which corresponds to port 1 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
<tr>
<td>sfpa_txdisable</td>
<td>0</td>
<td>SFP transmitter disable for Ethernet port 0. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 97, which corresponds to port 4 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 79, which corresponds to port 0 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
<tr>
<td>sfpb_txdisable</td>
<td>0</td>
<td>SFP transmitter disable for Ethernet port 1. Connect this signal to HSMC port A in the development boards. In the Stratix IV GX FPGA development board, HSMC port A is pin 109, which corresponds to port 5 (LVDS IO) in the HSMC daughtercard. In the Arria II GX FPGA development board, HSMC port A is pin 68, which corresponds to port 1 (GX transceiver) in the HSMC daughtercard.</td>
</tr>
</tbody>
</table>

Document Revision History

Table 10 shows the revision history for this document.

Table 10. Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2011</td>
<td>1.0</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>