Understanding Timing in Altera CPLDs

AN-629-1.0 Application Note

This application note describes external and internal timing parameters, and illustrates the timing models for MAX® II and MAX V devices.

Altera® devices provide predictable device performance that is consistent from simulation-to-application. Before programming a device, you can determine the worst-case timing delays for your design. To approximate propagation delays, you can use:

- Quartus® II TimeQuest Timing Analyzer
- Timing models provided in this application note
- Timing parameters listed in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* and *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.

For the most precise timing results, you use the Quartus II TimeQuest Timing Analyzer. For more information, refer to "Timing Model Versus the Quartus II TimeQuest Timing Analyzer" on page 9.

Familiarity with device architecture and characteristics is assumed. For a complete description of the architecture and the specific values of timing parameters listed in this application note, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* and *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.

This application note contains the following sections:

101 Innovation Drive
San Jose, CA 95134
www.altera.com

External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal timing parameters.

You can find the values of the external timing parameters in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* and *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*. These external timing parameters are worst-case values, derived from extensive performance measurements and ensured by testing.

Table 1 lists external timing parameters for MAX II and MAX V devices.

Table 1. External Timing Parameters for MAX II and MAX V Devices

Parameter	Description
t_{PD1}	Pin-to-pin delay for the worst case I/O placement with a diagonal path across the device with combinational logic implemented in a single look-up table (LUT) in a logic array block (LAB) adjacent to the output pin. Use the fast I/O connection from the adjacent logic element (LE) to the output pin.
t_{PD2}	Pin-to-pin delay for the best case I/O placement with combinational logic (2-input AND gate) implemented in a single edge LE adjacent to the input pin. The longest pin path of the two inputs is shown. Use the fast I/O connection from the adjacent LE to the output pin.
t_{CLR}	Time to clear register delay. The time required for a low signal to appear at the external output and measured from the input transition.
t_{SU}	Global clock setup time. The time that data must be present at the input pin before the global (synchronous) clock signal is asserted at the clock pin.
t_{H}	Global clock hold time. The time that data must be present at the input pin after the global clock signal is asserted at the clock pin.
t_{CO}	Global clock to output delay. The time required to obtain a valid output after the global clock is asserted at the clock pin.
t_{CNT}	Minimum global clock period. The minimum period maintained by a globally clocked counter.

Internal Timing Parameters

Within a device, the timing delays contributed by individual architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal parameters are shown in italic type.

Table 2 lists the internal timing microparameters for MAX II and MAX V devices.

Table 2. Internal Timing Microparameters for MAX II and MAX V Devices (Part 1 of 2)

Parameter	Description
t_{LUT}	LE combinational LUT delay for data-in to data-out.
t_{COMB}	Combinational path delay. The delay from the time when a combinational logic signal from the LUT bypasses the LE register to the time it becomes available at the LE output.
t_{CLR}	LE register clear delay. The delay from the assertion of the register's asynchronous clear input to the time the register output stabilizes at logical low.
t_{PRE}	LE register preset delay. The delay from the assertion of the register's asynchronous preset input to the time the register output stabilizes at logical high.

Table 2. Internal Timing Microparameters for MAX II and MAX V Devices (Part 2 of 2)

Parameter	Description
t_{SU}	LE register setup time before clock. The time required for a signal to be stable at the register's data and enable inputs before the register clock rising edge to ensure that the register correctly stores the input data.
t_{H}	LE register hold time after clock. The time required for a signal to be stable at the register's data and enable inputs after the register clock's rising edge to ensure that the register correctly stores the input data.
t_{CO}	LE register clock-to-output delay. The delay from the rising edge of the register's clock to the time the data appears at the register output.
t_{C}	Register control delay. The time required for a signal to be routed to the clock, preset, or clear input of an LE register.
t_{FASTIO}	Combinational output delay. t_{FASTIO} is the time required for a combinational signal from the LE adjacent to the I/O block using the fast I/O connection.
t_{IN}	I/O input pad and buffer delay. The t_{IN} applies to I/O pins used as inputs.
t_{GLOB}	t_{GLOB} applies to GCLK pins when used for global signals. t_{GLOB} is the delay required for a global signal to be routed from the GCLK pins to the LAB column clocks through the global clock network.
t_{IOE}	Internal generated output enable delay. The delay from an internally generated signal on the interconnect to the output enable of the tri-state buffer.
t_{DL}	Input routing delay. The delay incurred from the row I/O pin used as input to the LE adjacent to it.
t_{IODR}	Output data delay for the row interconnect. The delay incurred by the signals routed from an interconnect to an I/O cell.
t_{OD}	Output delay buffer and pad delay. For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to the *Timing Model and Specifications* section in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* and the *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.
t_{XZ}	Output buffer disable delay. The delay required for high impedance to appear at the output pin after the output buffer's enable control is disabled. For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to the *Timing Model and Specifications* section in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* and the *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.
t_{ZX}	Output buffer enable delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled. For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to the *Timing Model and Specifications* section in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* and the *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.
t_{C4}	Delay for a column interconnect with average loading. t_{C4} covers a distance of four LAB rows.
t_{R4}	Delay for a row interconnect with average loading. t_{R4} covers a distance of four LAB columns.
t_{LOCAL}	Local interconnect delay.

Internal Timing Parameters for User Flash Memory in MAX II and MAX V Devices

Timing parameters for user flash memory (UFM) in MAX II and MAX V devices are the timing delays contributed by the UFM architectural elements, which cannot be measured explicitly. All timing parameters are shown in italic type.

Table 3 lists the timing microparameters for UFM in MAX II and MAX V devices.

Table 3. Internal Timing Microparameters for UFM in MAX II and MAX V Devices

Parameter	Description
t_{ASU}	Address register shift signal setup to the address register clock.
t_{AH}	Address register shift signal hold from the address register clock.
t_{ADS}	Address register data in setup to the address register clock.
t_{ADH}	Address register data in hold from the address register clock.
t_{DSS}	Data register shift signal setup to the data register clock.
t_{DSH}	Data register shift signal hold from the data register clock.
t_{DDS}	Data register data in setup to the data register clock.
t_{DDH}	Data register data in hold from the data register clock.
t_{DCO}	Delay incurred from the data register clock to the data register output when shifting the data out.
t_{DP}	PROGRAM signal to the data clock hold time.
t_{PB}	Maximum delay between the PROGRAM rising edge and the UFM BUSY signal rising edge.
t_{BP}	Minimum delay allowed from the UFM BUSY signal going low to the PROGRAM signal going low.
t_{PPMX}	Maximum length of the busy pulse during a program.
t_{AE}	Minimum ERASE signal to the address clock hold time.
t_{EB}	Maximum delay between the ERASE rising edge and the UFM BUSY signal rising edge.
t_{BE}	Minimum delay allowed from the UFM BUSY signal going low to the ERASE signal going low.
t_{EPMX}	Maximum length of the busy pulse during an erase.
t_{RA}	Maximum read-access time. The delay incurred between the DRSHFT signal going low to the first bit of data observed at the data register output.
t_{OE}	Delay from the OSC_ENA signal reaching UFM to the rising clock of OSC leaving UFM.
t_{OSCS}	Maximum delay between the OSC_ENA rising edge and the ERASE/PROGRAM signal rising edge.
t_{OSCH}	Minimum delay allowed from the ERASE/PROGRAM signal going low to the OSC_ENA signal going low.

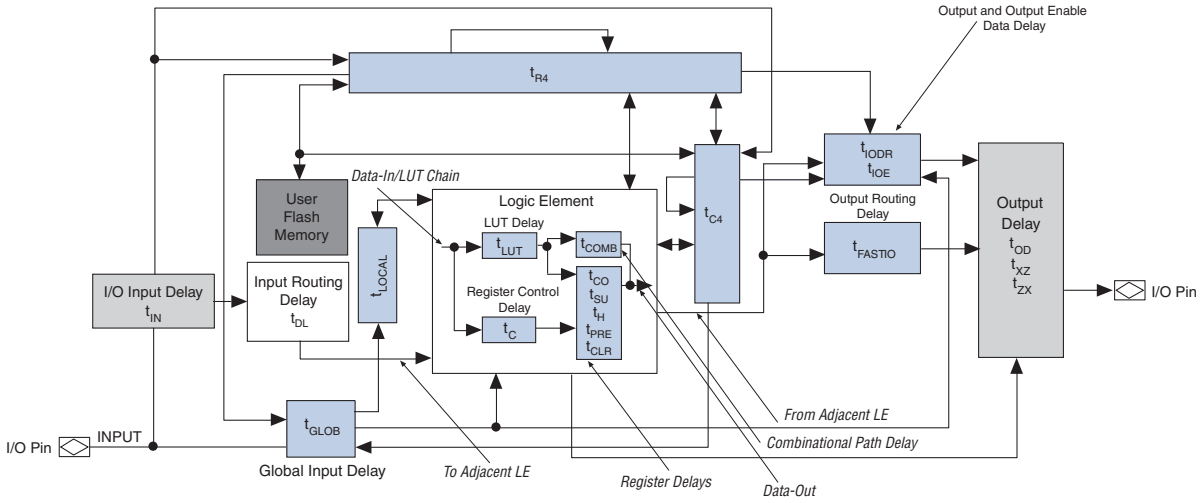
Timing Models

Timing models are simplified block diagrams that illustrate delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your design by examining the equations listed in the Quartus II Text-Format Report File (**.rpt**) for the project. You can then add up the appropriate internal timing parameters to estimate the delays through the device.

MAX II and MAX V device architecture has a globally routed clock. The MultiTrack interconnect ensures predictable performance, accurate simulation, and accurate timing analysis across all MAX II and MAX V device densities and speed grades.

Figure 1 shows the timing model for MAX II and MAX V devices.

Figure 1. Timing Model for MAX II and MAX V Devices



Calculating Timing Delays

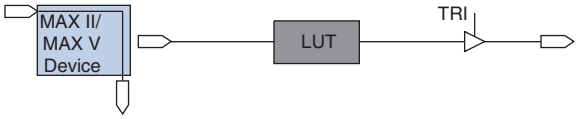
You can calculate approximate pin-to-pin timing delays for MAX II and MAX V devices with the timing model shown in Figure 1.

For more information, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* and the *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.

Each external timing parameter is calculated from a combination of internal timing parameters. Figure 2 through Figure 6 show the external timing parameters for MAX II and MAX V devices. To calculate the delay for a signal that follows a different path through MAX II and MAX V devices, refer to the timing model to determine which internal timing parameters to add together.

For the most precise timing results, use the Quartus II TimeQuest Timing Analyzer, which accounts for the effects of secondary factors such as placement and fan-out.

Figure 2. External Timing Parameter (t_{PD1}) *(Note 1)*



Note to Figure 2:

(1) $t_{PD1} = t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT} + t_{COMB} + t_{FASTIO} + (t_{OD} + \Delta t_{OD})$

Δt_{OD} is the adder delay (refer to Figure 2) for the t_{OD} microparameter when using an I/O standard other than 3.3-V LVTTL with 16 mA current strength.

For more information about adder delay values, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* and the *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.

Table 4 lists the numbers of LABs according to device density.

Table 4. Numbers of LABs According to Device Density

Device Family	Device Density	N LAB Rows	M LAB Columns
MAX II	EPM240	4	6
	EPM570	7	12
	EPM1270	10	16
	EPM2210	13	20
MAX V	5M40Z	4	6
	5M80Z	4	6
	5M160Z	4	6
	5M240Z *(1)*	4	6
	5M240Z *(2)*	7	12
	5M570Z	7	12
	5M1270Z *(3)*	10	16
	5M1270Z *(4)*	13	20
	5M2210Z	13	20

Notes to Table 4:

(1) Not applicable to the T144 package of the 5M240Z device.
(2) Only applicable to the T144 package of the 5M240Z device.
(3) Not applicable to the F324 package of the 5M1270Z device.
(4) Only applicable to the F324 package of the 5M1270Z device.

The following is an external timing example:

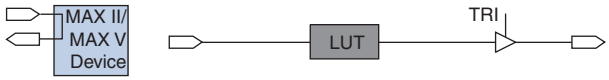
t_{PD1} for the 5M240Z device using an I/O standard of 3.3-V LVTTL fast slew rate with a drive strength of 16 mA:

$$t_{PD1} = t_{IN} + 4 \times t_{R4}/4 + 6 \times t_{C4}/4 + t_{LUT} + t_{COMB} + t_{FASTIO} + t_{OD} \ldots\ldots (a)$$

t_{PD1} for the 5M240Z device using an I/O standard of 2.5-V LVTTL fast slew rate with a drive strength of 7 mA:

$$t_{PD1} = (a) + (\Delta t_{OD} \text{ of 2.5-V LVTTL fast slew 7 mA})$$

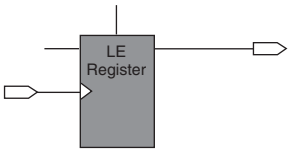
Figure 3. External Timing Parameter (t_{PD2}) *(Note 1)*



Note to Figure 3:

(1) $t_{PD2} = t_{IN} + t_{DL} + t_{LUT} + t_{COMB} + t_{FASTIO} + (t_{OD} + \Delta t_{OD})$

Figure 4. External Timing Parameter (t_{CO}) *(Note 1), (2)*

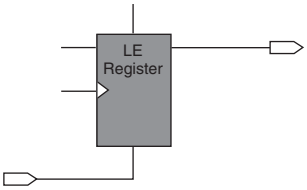


Notes to Figure 4:

(1) $t_{CO} = t_{GLOB} + t_C + t_{CO} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ or } t_{IODR}) + (t_{OD} + \Delta t_{OD})$

(2) The constants N and M are subject to change according to the position of the LAB in the entire device.

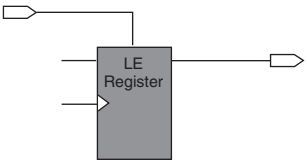
Figure 5. LE Register Clear and Preset Time (t_{CLR}) *(Note 1)*



Note to Figure 5:

(1) $t_{CLR} = t_{GLOB} + t_C + t_{CLR} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ or } t_{IODR}) + (t_{OD} + \Delta t_{OD})$

Figure 6. LE Register Clear and Preset Time (t_{PRE}) *(Note 1)*



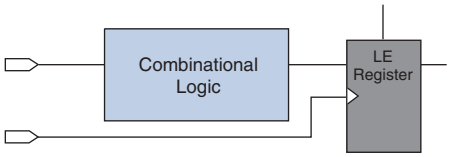
Note to Figure 6:

(1) $t_{PRE} = t_{GLOB} + t_{LOCAL} + t_C + t_{PRE} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ or } t_{IODR}) + (t_{OD} + \Delta t_{OD})$

Setup and Hold Time from an I/O Data and Clock Input

The Quartus II software might insert additional routing delays from the input pin to the register input to ensure a zero hold time for the LE register. Altera recommends using the Quartus II TimeQuest Timing Analyzer to obtain the setup and hold time. Figure 7 and Figure 8 show the setup and hold time for MAX II and MAX V devices.

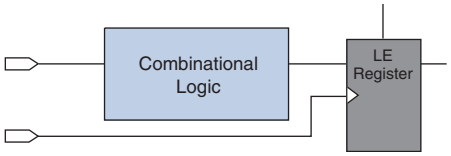
Figure 7. Setup and Hold Time (t_{SU}) *(Note 1)*



Note to Figure 7:

(1) $t_{SU} = (t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT}) - (t_{GLOB} + t_C) + t_{SU}$

Figure 8. Setup and Hold Time (t_H) *(Note 1)*



Note to Figure 8:

(1) $t_H = (t_{GLOB} + t_C) - (t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT}) + t_H$

For Figure 4 through Figure 8, the constants N and M are subject to change according to the position of the LAB in the entire device for combinational logic implementation.

Programmable Input Delay

To guarantee a zero hold time, the programmable input delay provides an option to add a delay to the input pin. You can set this option in the Assignment Editor (Assignments menu) on a pin-by-pin basis. To turn on the input delay for the selected input pin in the Quartus II software, perform the following steps:

1. Select the input pin name in the design file.
2. Right-click and select **Locate** in the Assignment Editor.
3. Double-click the cell under Assignment Name and select **Input Delay from Pin to Internal Cells** from the pull-down list.
4. Double-click the **Value** cell to the right of the assignment name just made and enter **1**.
5. On the File menu, click **Save**.

Timing Model Versus the Quartus II TimeQuest Timing Analyzer

While hand calculations based on the timing model can provide you with an estimate of your design performance, Altera recommends using the Quartus II TimeQuest Timing Analyzer to obtain the most accurate information on design performance because it takes into account secondary factors that influence the routing microparameters such as:

- Fan-out for each signal in the delay path
- Positions of other loads relative to the signal source and destination
- Distance between the signal source and destination
- Various interconnect lengths where some interconnects are truncated at the edge of the device

Document Revision History

Table 5 lists the revision history for this application note.

Table 5. Document Revision History

Date	Version	Changes
December 2010	1.0	Initial release.