


This reference design describes how to map a 3-gigabit-per-second serial digital interface (3G-SDI) Level B and a dual link high-definition serial digital interface (HD-SDI) using the Altera® SDI MegaCore® function and the Audio Video Development Kit, Stratix® IV GX Edition. The Audio Video Development Kit, Stratix IV GX Edition, consists of the Stratix IV GX development board and two SDI high-speed mezzanine cards (HSMC). The dual link HD-SDI consists of two SMPTE 292M HD-SDI operating at a nominal rate of 2.970 GB per second or 2.967 GB per second.

This application note describes the following two demonstrations:

- Mapping of 3G-SDI level B to dual link HD-SDI (receiver)
- Mapping of dual link HD-SDI to 3G-SDI level B (receiver)

 For more information about the Stratix IV GX audio and video development kit, refer to the *Audio Video Development Kit, Stratix IV GX Edition User Guide*. For more information about the Stratix IV GX FPGA development board, refer to the *Stratix IV GX FPGA Development Board Reference Manual*; for more information about the SDI HSMC, refer to the *SDI HSMC Reference Manual* or *AN 600: Serial Digital Interface Reference Design for Stratix IV Devices*. For more information about the SDI MegaCore function, refer to the *SDI MegaCore Function User Guide* or contact your Altera representative.

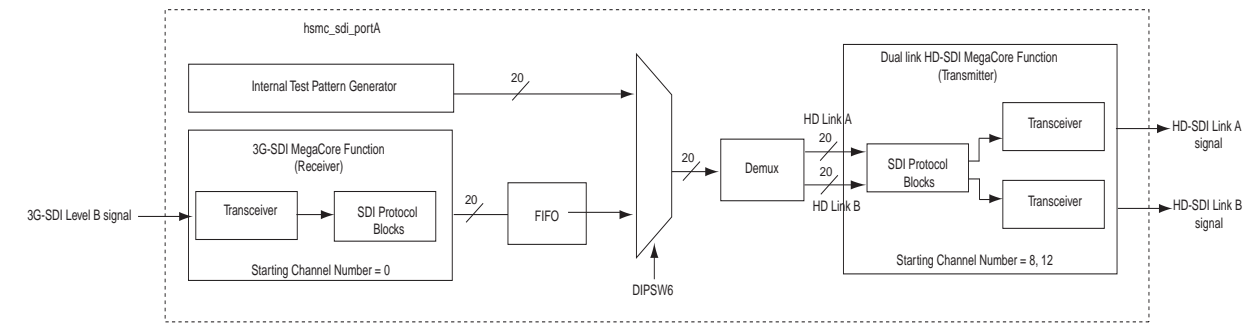
Functional Description

The reference design provides a general platform to perform signal mapping from 3G-SDI Level B signal to two HD-SDI signals and vice versa. [Figure 1 on page 2](#) and [Figure 2 on page 3](#) show two high-level block diagrams of the reference design.

Mapping of 3G-SDI Level B to Dual Link HD-SDI

The following sections describe the various elements used in the mapping of the 3G-SDI level B to dual link HD-SDI as shown in Figure 1.

Figure 1. Block Diagram—Mapping of 3G-SDI Level B to Dual Link HD-SDI



3G-SDI Receiver

The triple-standard SDI receiver MegaCore function provides a 3G-SDI level B receiver interface.

Dual Link HD-SDI Transmitter

The dual link HD-SDI transmitter MegaCore function outputs two links of 1.485-Gbps 1080i data stream.

Demux

The demultiplexer logic receives the input from the internal pattern generator or the 3G-SDI signal from the triple-standard receiver, and then demultiplexes the 3G-SDI signal to two HD link data stream. The DIPSW6 on the development kit selects either the HD link A or HD link B option.

Pattern Generator

The pattern generator outputs a test pattern.

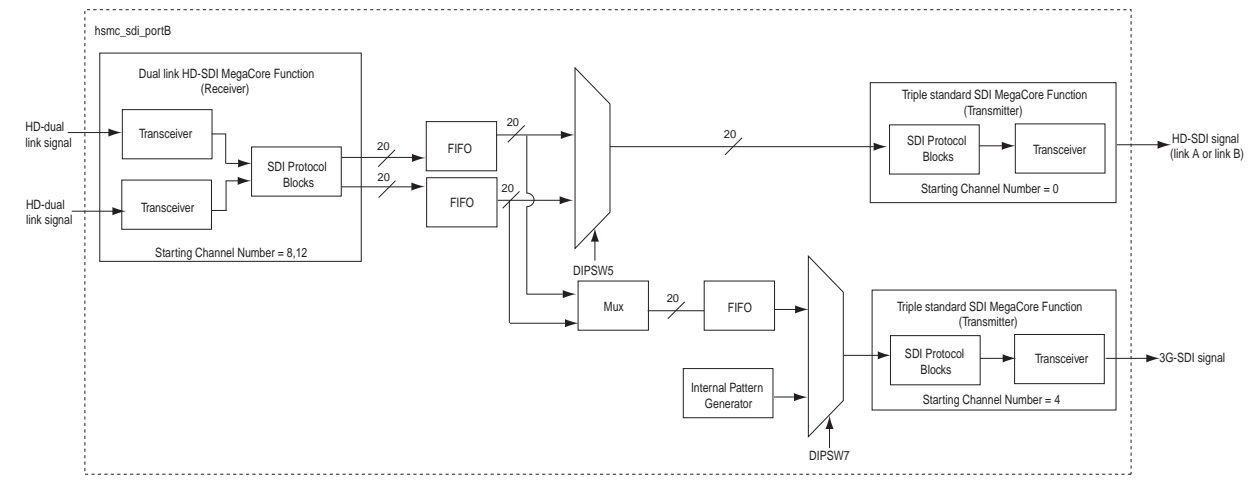
FIFO

The FIFO stores the parallel video data. When the FIFO buffer is half full, the transmitter starts to read, encode, and transmit the data.

Mapping of Dual Link HD-SDI to 3G-SDI Level B

The following sections describe the various elements used to map the dual link HD-SDI to the 3G-SDI level B as shown in [Figure 2](#).

Figure 2. Block Diagram—Mapping of Dual Link HD-SDI to 3G-SDI Level B



Dual link HD-SDI Receiver

The dual link HD-SDI receiver MegaCore function provides a dual link HD-SDI receiver interface. The dual link HD-SDI timing difference between link A and link B at the source must not exceed 40 ns (specification of SMPTE372). You must assert `rst_rx` when both link A and link B are ready to receive data for the first time.

Triple-Standard SDI Transmitter

The triple-standard SDI MegaCore function transmitter, `inst2`, is used to transmit HD signal. The `DIPSW5` on the development kit is used to transmit HD Link A data stream or HD Link B data stream.

The triple-standard SDI MegaCore function transmitter, `inst3`, is used to transmit 3Gb signal. The `DIPSW6` on the development kit is used to transmit 3Gb signal generated from the internal pattern generator or the 3Gb signal multiplexor from two receiver HD signal.

FIFO

The FIFO stores the parallel video data. When the FIFO buffer is half full, the transmitter starts to read, encode, and transmit the data.

Mux (Serial Interleave Streaming)

The multiplexer logic receives the input from two dual link HD-SDI data and streams the input into the interleaved 3G-SDI level B data.

Data Conversions

Figure 3 and Figure 4 show the conversion of 3G-SDI Level B data to 2 HD-SDI data streams and vice versa.

Figure 3. Conversion of 3G-SDI Level B Data to 2 HD-SDI Data Streams

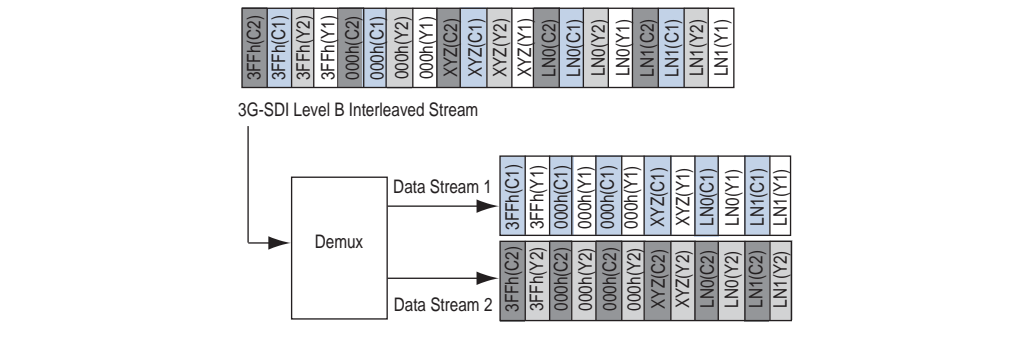


Figure 4. Conversion of 2 HD-SDI Data Streams to 3G-SDI Level B Data

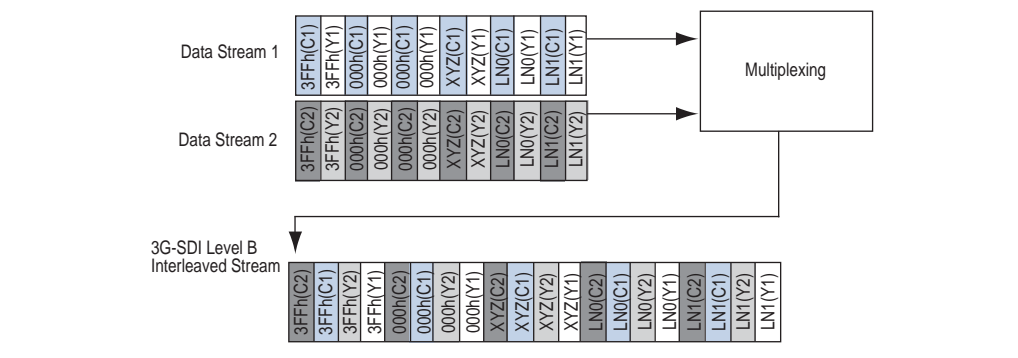
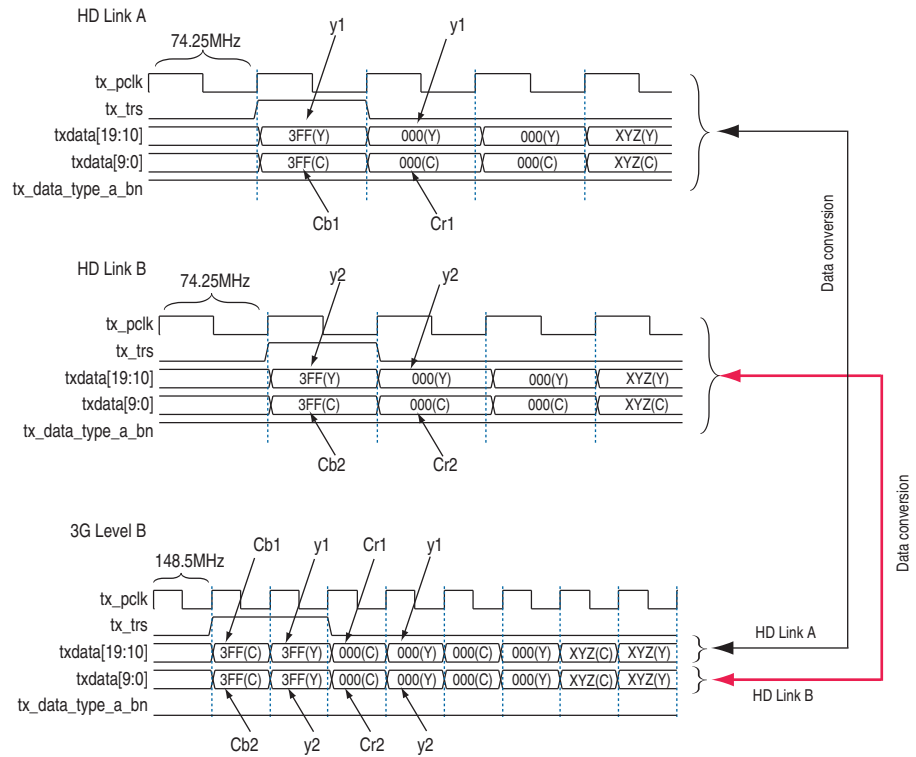


Figure 5 shows the timing diagrams of the data conversions from 3G-SDI Level B to 2 HD-SDI data streams and vice versa.

Figure 5. Data Conversions from 3G-SDI Level B Data to 2 HD-SDI Data Streams and Vice Versa



Getting Started

This section discusses the requirements and related procedures to demonstrate the reference design with the Stratix IV GX development board. This section contains the following topics:

- [Hardware and Software Requirements](#)
- [Setting Up the Hardware](#)
- [Running the Reference Design](#)

Hardware and Software Requirements

The reference design requires the following hardware and software:

- Stratix IV GX development board
- Two SDI HSMC
- SDI MegaCore function
- Quartus® II software, version 10.0 sp1 patch 1.181

To obtain the Audio Video Development Kit, Stratix IV GX Edition, contact your local Altera representative.

Setting Up the Hardware

Figure 6 shows how the Stratix IV GX development board is connected to the SDI HSMC.

Figure 6. Hardware Setup

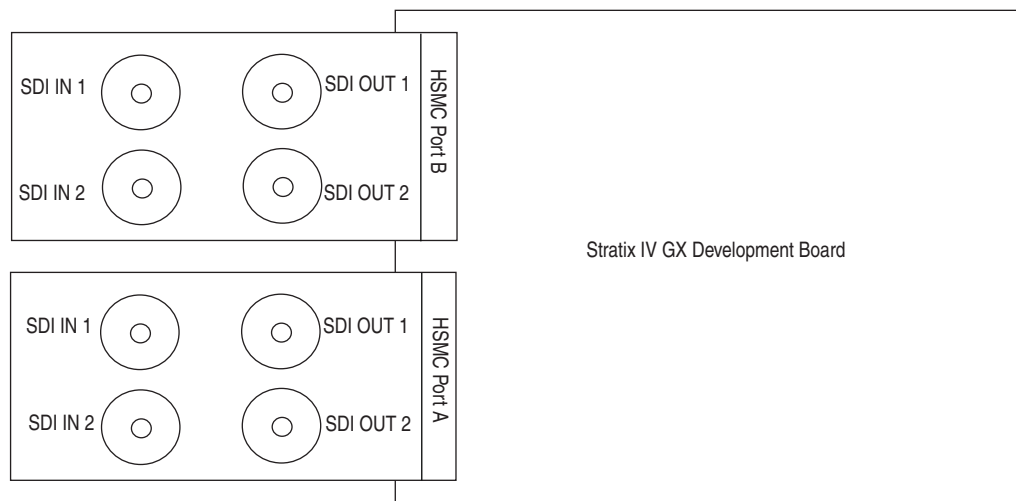


Table 1 describes the HSMC ports that are mapped to the design instance.

Table 1. Mapping of HSMC Ports to the Design Instance

HSMC Port	Design Instance Name	Description
HSMC Port A		
SDI OUT 1	hd_dl_tx_inst (HD Link B)	Transmits lower stream of the dual link HD-SDI data[19:0].
SDI OUT 2	hd_dl_tx_inst (HD Link A)	Transmits upper stream of the dual link HD-SDI data[39:20].
SDI IN 1	threeG_rx_inst0	Triple-standard receiver receives the 3G-SDI Level B signal.
SDI IN 2	threeG_rx_inst1	Triple-standard receiver receives the 3G-SDI Level B signal (for loopback verification).
HSMC Port B		
SDI OUT 1	tripleStd_tx_inst2	Triple-standard transmitter transmits HD stream A or stream B signals.
SDI OUT 2	tripleStd_tx_inst3	Triple-standard transmitter transmits 3G-SDI Level B signal from two HD streams.
SDI IN 1	hd_dl_rx_inst (HD Link B)	Receives lower stream of the dual link HD-SDI data[19:0].
SDI IN 2	hd_dl_rx_inst (HD Link A)	Receives upper stream of dual link HD-SDI data[39:20].

Table 2 describes the function of each user-defined dual in-line package (DIP) switch control. When the switch is in the OFF position, logic 1 is selected. When the switch is in the ON position, logic 0 is selected.

Table 2. SW3 DIP Switch Controls

DIPSW	Description
8	1= Hold reset 0= Release reset
7	1= hd_dl_tx_inst: hd txdata from the internal pattern 0= hd_dl_tx_inst: hd txdata demux from the 3gb
6	1= tripleStd_tx_inst3: 3gb txdata from the internal pattern 0= tripleStd_tx_inst3: 3gb txdata mux from hd_dl_rx_inst
5	1= tripleStd_tx_inst2: hd txdata link A 0= tripleStd_tx_inst2: hd txdata link B
4, 3, 2, 1	Not used

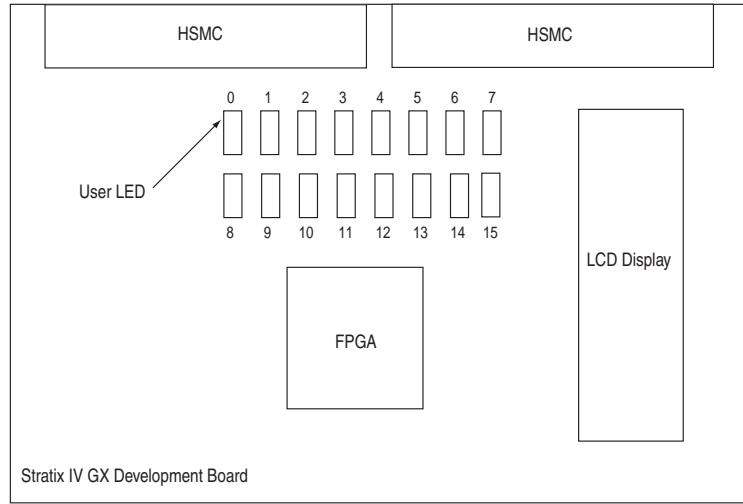
Table 3 describes the function of each LED on the Stratix IV GX development board.

Table 3. LEDs on Stratix IV GX FPGA Development Board

LED	Description
0	Alignment lock HSMC port A: 3G SDI receiver inst0
1	TRS lock HSMC port A: 3G SDI receiver inst0
2	Frame lock HSMC port A: 3G SDI receiver inst0
3	Not used
4	Alignment lock HSMC port A: 3G SDI receiver inst1
5	TRS lock HSMC port A: 3G SDI receiver inst1
6	Frame lock HSMC port A: 3G SDI receiver inst1
7	Not used
8	Alignment lock HSMC port B: Dual link HD-SDI receiver (Link A)
9	TRS lock HSMC port B: Dual link HD-SDI receiver (Link A)
10	Frame lock HSMC port B: Dual link HD-SDI receiver (Link A)
11	Alignment lock HSMC port B: Dual link HD-SDI receiver (Link B)
12	TRS lock HSMC port B: Dual link HD-SDI receiver (Link B)
13	Frame lock HSMC port B: Dual link HD-SDI receiver (Link B)
14	Not used
15	Dual link HD-SDI receiver Link A and Link B is aligned

Figure 7 shows the orientation of the LEDs on the Stratix IV GX development board.

Figure 7. User LED on the Stratix IV FPGA Development Board

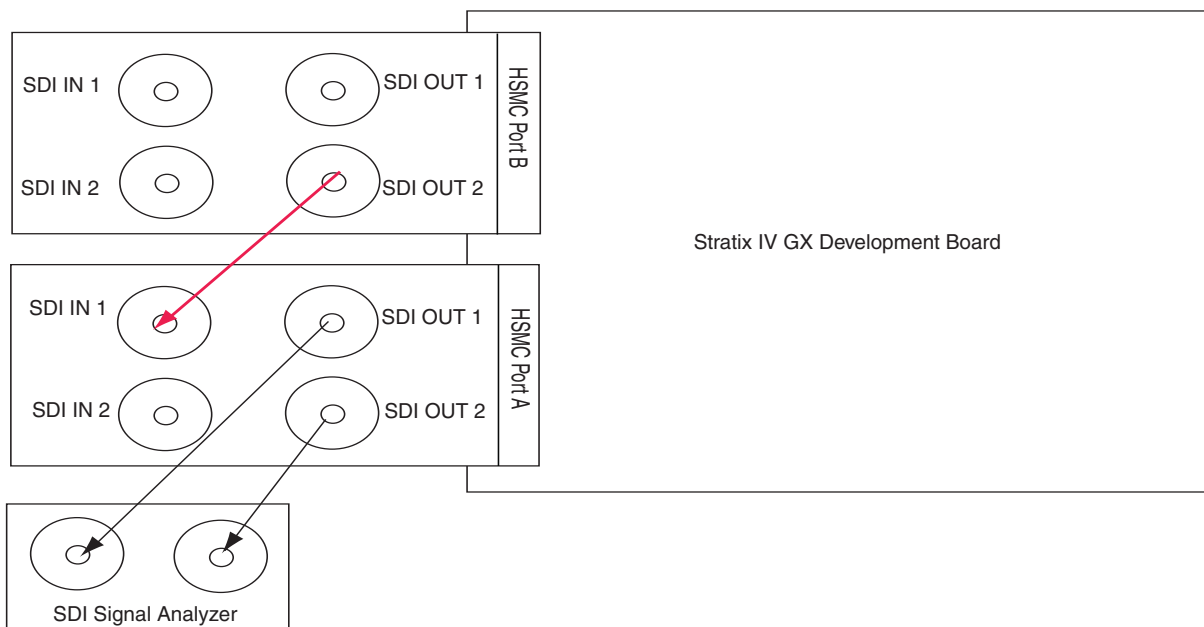


Running the Reference Design

To run the reference design, follow these steps:

1. Connect two SDI HSMCs to the HSMA and HSMB ports on the FPGA development board as shown in [Figure 6 on page 6](#).
2. Set up the HSMC port A and HSMC port B connections to map the 3G-SDI level B to the dual link HD-SDI. Connect an SDI signal analyzer to the transmitter output SDI OUT 1 port or SDI OUT 2 port as shown in [Figure 8](#).

Figure 8. 3G-SDI Level B to Dual Link HD-SDI Hardware Setup



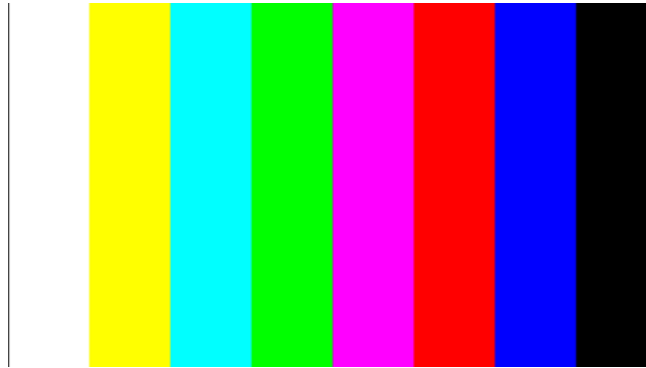
3. Connect the power supply to the board.
4. Launch the Quartus II software and compile the reference design. To compile the reference design, follow these steps:
 - a. On the File menu click **Open Project**, navigate to `\<directory>\s4gxsdi.qpf`, and then click **Open**.
 - b. On the Processing menu, click **Start Compilation**.
5. Download the Quartus II-generated SRAM object file (.sof):
 - a. Connect the USB-Blaster™ download cable to the board's USB Type-B Connector.
 - b. On the Tools menu, click **Programmer**. The software automatically detects the **s4gxsdi.sof** file during compilation and it appears on the pop-up window. Click **Start** to download the Quartus II-generated file to the board. If the file does not appear in the pop-up window, click **Add File**, navigate to `\<directory>\s4gxsdi.sof`, and then click **Open**.



This design is volatile. You must reload this design each time the board is powered on.

6. To transmit 3Gb signal (port B) using the internal pattern, set DIPSW6 = 1 and DIPSW7 = 0. Reset the hardware by controlling DIPSW8.
7. Observe the signal behavior on your signal analyzer. SDI OUT 1 port signal represents the HD stream A signal and the SDI OUT 2 port signal represents the HD stream B signal, demux from receiving 3GB signal.

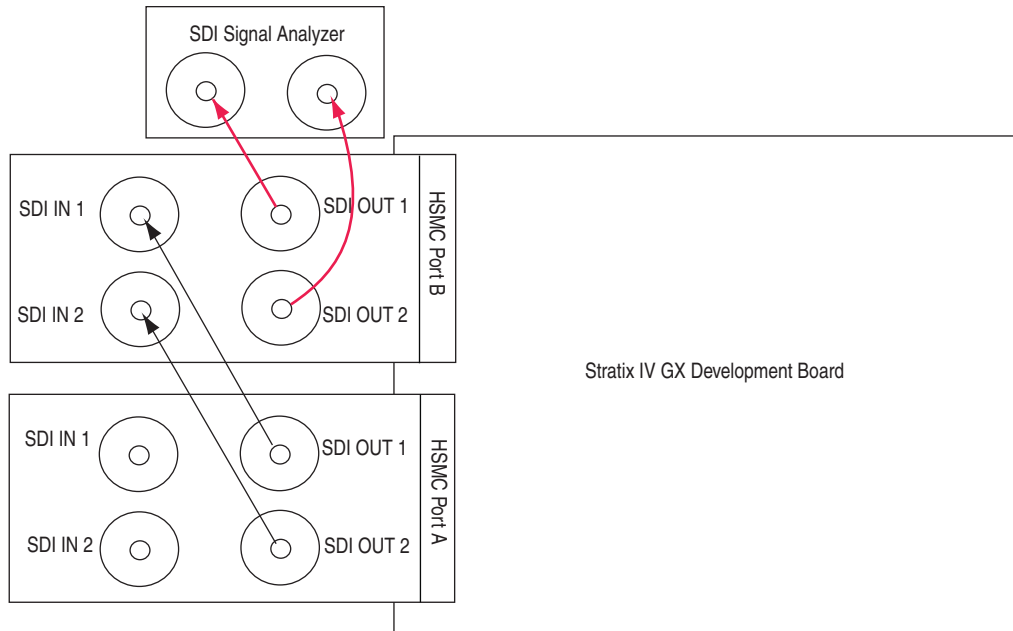
Figure 9. HD Link A and HD Link B Image



8. Connect the dual link HD-SDI Link A signal source from the SDI OUT 2 port of the HSMA to the receiver input SDI IN 2 port of the HSMB. Connect the dual link HD-SDI Link A signal source from the SDI OUT 1 port of the HSMA to the receiver input SDI IN 1 port of the HSMB. Observe the HD dual link receiver. Link A and Link B receiver should be able to lock.

9. Set up the HSMC port A and HSMC port B connections to map the dual link HD-SDI to the 3G-SDI level B. Connect the dual link HD-SDI Link A signal source from the SDI OUT 2 port of the HSMA to the receiver input SDI IN 2 port of the HSMB. Connect an SDI analyzer to the transmitter output SDI OUT 1 port or SDI OUT 2 port of the HSMB as shown in [Figure 10](#).

Figure 10. 3G-SDI Level B to Dual Link HD-SDI Hardware Setup



10. Repeat steps [3](#), [4](#), and [5](#).
11. To transmit HD dual link signal (port A) using the internal pattern, set `DIPSW6 = 0` and `DIPSW7 = 1`. Reset the hardware by controlling `DIPSW8`.
12. Observe the signal behavior on your signal analyzer. SDI OUT 2 port signal represents the interleaved multiplexed 3Gb signal and SDI OUT 1 port signal represents the demultiplexed HD dual link signal.

13. Specify the following board settings, and observe the signal behavior. Specify `DIPSW5 = 1` to control output link A or link B for SDI OUT 1 port.

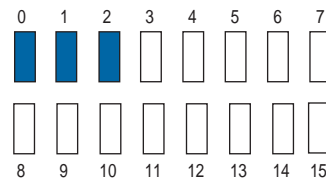
Figure 11. SDI_OUT1: HD Link B (if internal Pattern is Selected)



Figure 12. SDI_OUT2: HD Link A (if internal Pattern is Selected)

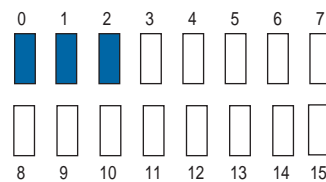


14. Connect the SDI OUT 2 port of the HSMB to the receiver input SDI IN 1 port of the HSMA. Ensure that the 3Gb signal that is transmitted from SDI OUT 2 port of the HSMB is locked by the 3G instance of SDI IN 1 port of the HSMA.
15. Observe the condition of the LEDs for the following implementations:
- The LEDs indicate the following conditions for the 3G-SDI instance Ch0:
 - LED 0 illuminates when the receiver is word aligned.
 - LED 1 illuminates when the received line format is stable.
 - LED 2 illuminates when the receiver frame format is stable.

Figure 13. Condition of LEDs for 3G-SDI Instance Ch0

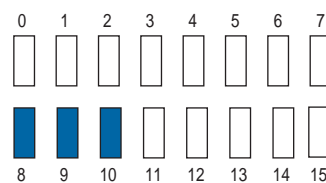
b. The LEDs indicate the following conditions for the 3G-SDI instance Ch1:

- LED 0 illuminates when the receiver is word aligned.
- LED 1 illuminates when the received line format is stable.
- LED 2 illuminates when the receiver frame format is stable.

Figure 14. Condition of LEDs for 3G-SDI Instance Ch1

c. The LEDs indicate the following conditions for the dual link HD-SDI receiver (Link A):

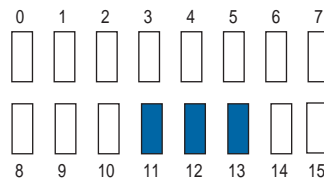
- LED 8 illuminates when the receiver is word aligned.
- LED 9 illuminates when the received line format is stable.
- LED 10 illuminates when the receiver frame format is stable.

Figure 15. Condition of LEDs for Dual Link HD-SDI (Link A)

d. The LEDs indicate the following conditions for the dual link HD-SDI receiver (Link B):

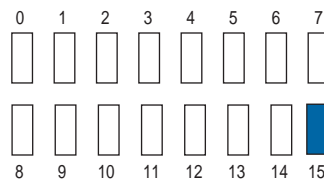
- LED 11 illuminates when the receiver is word aligned.
- LED 12 illuminates when the received line format is stable.
- LED 13 illuminates when the receiver frame format is stable.

Figure 16. Condition of LEDs for Dual Link HD-SDI (Link B)



- e. The LEDs indicate the following conditions when the dual link HD-SDI (Link A) receiver is carry parallel rxdata[39:20], while the HD dual link B is carry parallel radata[19:0]:
 - LED 15 illuminates when Link A and Link B of the dual link HD-SDI receiver are aligned.

Figure 17. Condition of LEDs when HD-Dual Link A and Link B are Aligned



Conclusion

This application note provides ways to use the SDI reference design with the Stratix IV GX development board and the SDI HSMC to perform conversions between the dual link HD-SDI and 3G-SDI.

Document Revision History

Table 4 shows the revision history for this document.

Table 4. Document Revision History

Date	Version	Changes
December 2010	1.0	Initial release.