This application note describes how to use the on-chip signal quality monitoring circuitry (EyeQ) feature available in Stratix IV transceivers to help you estimate the horizontal eye-opening and select the best data sampling point at the receiver. It also describes the system-level blocks that are required to use the EyeQ feature.

Popular data communication, telecommunication serial protocols, and proprietary links target very stringent bit error ratio (BER) requirements. For example, Common Electrical I/O (CEI-6G-LR) targets a BER of 1E-15 at data rates up to 6.375 Gbps across 40 inches of copper. Encoded data streams of 64/66B experience significant inter-symbol interference (ISI) at these data rates due to the low-pass filter effect of the 40-inch trace and backplane connectors.

Meeting the stringent BER targets of 1E-15 over lossy backplanes and connectors is challenging. Altera’s 40-nm Stratix IV GX and GT high-speed transceivers are equipped with the following features to meet these BER targets:

- Signal conditioning circuitry—combat ISI introduced by lossy backplanes and connectors with three tap transmitter pre-emphasis, up to 16 dB of continuous time linear equalization, and decision feedback equalizer (DFE)
- On-chip signal quality monitoring circuitry (EyeQ)—estimates the horizontal eye-opening at the receiver serial data sampling point and helps you select an optimum data sampling point at the receiver

**Link Evaluation and Remote In-System Debugging**

The EyeQ feature is designed to work with the following two applications:

- Optimal signal conditioning during the link evaluation (refer to “Using the EyeQ Feature During Link Evaluation”)
- Remote in-system debugging on the receiving bit errors (refer to “Using the EyeQ Feature for Remote In-System Debugging”)

**Using the EyeQ Feature During Link Evaluation**

The EyeQ feature in Stratix IV transceivers is designed to estimate the actual eye opening at the receiver data sampling point. You can use the EyeQ feature during the link evaluation phase to select the optimal combination of signal conditioning settings that result in the widest eye opening.

The horizontal eye opening at the receiver data sampling point is the percentage of the unit interval (UI) where the signal amplitude is greater than the sampling threshold. The wider the eye opening at the receiver data sampling point, the better the sampling margin, resulting in a better BER performance.
It is impossible to physically measure the eye opening at the receiver data sampling point with an oscilloscope. The nearest accessible probe point is at the receiver serial input pins on the device package. Measuring the eye-diagram at a receiver serial input pin of a device package does not give a true picture of the eye-width at the data sampling point, especially when you enable receiver equalization.

Figure 1 shows the eye diagram at a receiver input pin of a device package which is completely closed due to ISI. The eye diagram at the data sampling point is significantly open after equalization.

**Figure 1. Horizontal Eye Opening Before and After Receiver Equalization**

![Eye Diagram Captured at a Receiver Input Pin of a Device Package](image1)

![Eye Diagram After Receiver Equalization](image2)

**Using the EyeQ Feature for Remote In-System Debugging**

Under normal operation when the EyeQ feature is not enabled, the recovered clock from the clock data recovery (CDR) unit is used to sample the serial data at the receiver. The recovered clock from the bang-bang phase detector-based CDR is usually located at the center of the eye which may not always be the optimum sampling point.

Figure 2 shows an eye diagram at the receiver with the optimum sampling point not being in the middle because of unequal rise and fall times. The recovered clock from the CDR that samples the incoming data at the middle of the eye barely meets the BER requirement. Variation in environmental conditions and aging could cause further degradation in signal integrity, which results in bit errors.
As part of remote in-system debug, you can enable the EyeQ feature and select the optimum sampling point to provide a better sampling margin and BER performance.

Figure 2. Optimal Sampling Point Not Located at the Center of the Eye

Measuring the Horizontal Eye Opening Using the EyeQ Feature

Unlike transmitter pre-emphasis and receiver equalization, the EyeQ feature does not combat high-frequency losses introduced by backplane connectors and traces. Instead, it allows you to estimate the effectiveness of a given transmitter pre-emphasis, or both receiver equalization settings by measuring the horizontal eye opening. Settings that yield a wider eye opening provide a better sampling margin and better BER performance.

The EyeQ feature provides 32 phase steps spanning one complete UI. You can select each of the 32 phase steps, one at a time, to sample the serial received data. By stepping through these 32 phase steps and monitoring the BER at each phase step, you can measure the horizontal eye opening after receiver equalization, as shown in Figure 3.
The target BER of 1E-12 in the eye diagram (Figure 3) is achieved for 18 (marked in green) out of 32 phase steps generated by the EyeQ feature. This is an estimate of the eye opening after receiver equalization. To evaluate if another equalization setting yields a wider eye opening, simply step through the 32 EyeQ phase steps with the new equalization setting. If the number of EyeQ phase steps that meet the target BER with the new equalization setting is more than the old equalization setting, the new setting yields a wider eye opening and potentially better BER performance.
Describing the EyeQ Feature

Figure 4 shows a block diagram of the EyeQ feature.

Figure 4. Block Diagram of the EyeQ Feature

Each receiver channel located in Stratix IV transceiver blocks has independent EyeQ circuitry that is comprised of the following blocks:

- **Phase interpolator**—the recovered clock from the CDR feeds into the phase interpolator. The phase interpolator uses this recovered clock as a reference to generate the 32 phase steps spanning one UI.

- **EyeQ data sampler**—uses the user-selected phase step to sample the data post receiver equalization. For phase steps that have the signal amplitude above the sampling threshold, the EyeQ data sampler captures the serial bits correctly, which yields good BER performance. For the remaining phase steps, the EyeQ data sampler captures the serial bits incorrectly, yielding poor BER performance. Stepping through all 32 phase steps and monitoring the BER for each provides an estimate of the horizontal eye opening.

- **Datapath selection multiplexers**—if you enable the EyeQ feature, the datapath selection multiplexers select the data sampled by the EyeQ data sampler to feed to the deserializer. Otherwise, it selects the data sampled by the receiver CDR to feed the deserializer.
**Required Soft-Blocks for the EyeQ Feature**

The EyeQ feature in the receiver channel is only responsible for generating the 32 phase steps from the recovered clock. To use the EyeQ feature, you must implement the following additional blocks in the FPGA fabric:

- Dynamic reconfiguration controller (ALTGX_RECONFIG megafunction)—enables the EyeQ feature and steps through the 32 phase steps for the desired receiver channel. It interfaces with the user-logic through the standard Avalon® memory mapped interface.

- User-logic—instructs the dynamic reconfiguration controller through the Avalon memory mapped interface to enable the EyeQ feature and step through the 32 phase steps.

- BER checker—monitors the BER for the selected phase step.

For step-by-step instructions about how to enable the EyeQ feature and step through the 32 phase steps with the ALTGX_RECONFIG controller, refer to the “EyeQ” section in the *Stratix IV Dynamic Reconfiguration* chapter in the *Stratix IV Device Handbook*.

You must assert \texttt{rx\_digital\_reset} (receiver physical coding sublayer [PCS] reset) for two parallel clock cycles whenever you enable or disable the EyeQ feature or select a new EyeQ phase step for the channel.

**Figure 5** shows a typical implementation block diagram of the EyeQ feature.

---

**Figure 5. System Implementation Block Diagram for the EyeQ Feature**

- **Off-Chip**
  - RX
  - Rx Equalization

- **Receiver PMA**
  - Receiver CDR
  - Deserializer
  - EyeQ

- **Receiver PCS**
  - PCS Blocks
  - rx\_ckout

- **FPGA Fabric**
  - BER Checker
  - Dynamic Reconfiguration Controller
  - Avalon Memory-Mapped Interface

- User Logic
Recommended EyeQ Feature Flow Process for Link Evaluation

To improve the sampling margin at the receiver and to meet a stringent BER target, use the recommended EyeQ feature flow process shown in Figure 6 during link evaluation.

Figure 6. Recommended EyeQ Feature Flow Process During Link Signal Integrity Evaluation

```
Establish the transceiver link with the EyeQ feature disabled (1)

Program signal conditioning settings (Tx Preemphasis, Rx Equalization) that must be evaluated

1) Enable the EyeQ feature with phase step 0 using the ALTGX_RECONFIG megafunction
2) Note the BER for phase step 0

Does the last programmed EyeQ phase step = 31?

1) Increment the EyeQ phase step selection by 1 using the ALTGX_RECONFIG megafunction
2) Note the BER for the new phase step

Plot the 32 phase steps on the X-axis and the corresponding BER values on the Y-axis to estimate the horizontal eye opening

Does the last programmed EyeQ phase step = 31?

1) Increment the EyeQ phase step selection by 1 using the ALTGX_RECONFIG megafunction
2) Note the BER for the new phase step

Plot the 32 phase steps on the X-axis and the corresponding BER values on the Y-axis to estimate the horizontal eye opening

Does the eye opening provide a sufficient sampling margin to meet the stringent BER target?

Yes
The target BER and sampling margin are achieved with the selected settings

No
```

Note to Figure 6:

(1) The established transceiver link implies that the CDR has locked to the incoming data and the stable recovered clock is used to sample it.

Figure 7 and Figure 8 show a sample EyeQ phase step versus BER plots derived with the flow shown in Figure 6.

- The plot in Figure 7 uses the linear receiver (RX) equalization setting of 3 and yields 19 EyeQ phase steps (0 – 15 and 29 – 31) that meet the BER target of 1E-15.
- The plot in Figure 8 uses the linear RX equalization setting of 9 and yields 23 EyeQ phase steps (0 – 19 and 29 – 31) that meet the BER target of 1E-15.
As evident from Figure 7 and Figure 8, the equalization setting of 9 yields a wider horizontal eye opening and a better sampling margin when compared with the equalization setting of 3.

**Figure 7. Example of BER Versus EyeQ Phase Step Plot for an RX Equalization Setting of 3**
Translating EyeQ Phase Steps into a Percentage of the Eye Opening

Use Equation 1 to calculate the percentage of the horizontal eye opening when you use the EyeQ feature.

Equation 1.

\[
\text{\% horizontal eye opening} = (\text{NBER} \times 3.125) \pm 3\%
\]

where, NBER is the number of phase steps for which the target BER is met.

The horizontal eye opening shown in Figure 7 with 19 EyeQ phase steps that meet the BER target of 1E-15 is 19 * 3.125 ±3% = 56% to 62%.

The horizontal eye opening shown in Figure 8 with 23 EyeQ phase steps that meet the BER target of 1E-15 is 23 * 3.125 ±3% = 69% to 75%.
Conclusion

The EyeQ feature provides a unique way of estimating the horizontal eye opening at the receiver data sampling point, as well as performing remote in-system debugging. With the EyeQ feature you can achieve a good margin to meet stringent BER requirements at high data rates.

For a reference design of the EyeQ feature, refer to Stratix IV GX Board EyeQ Reference Design.

Document Revision History

Table 1 lists the revision history for this application note.

Table 1. Document Revision History

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<td>1.2</td>
<td>Updated to improve searchability</td>
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