

Introduction

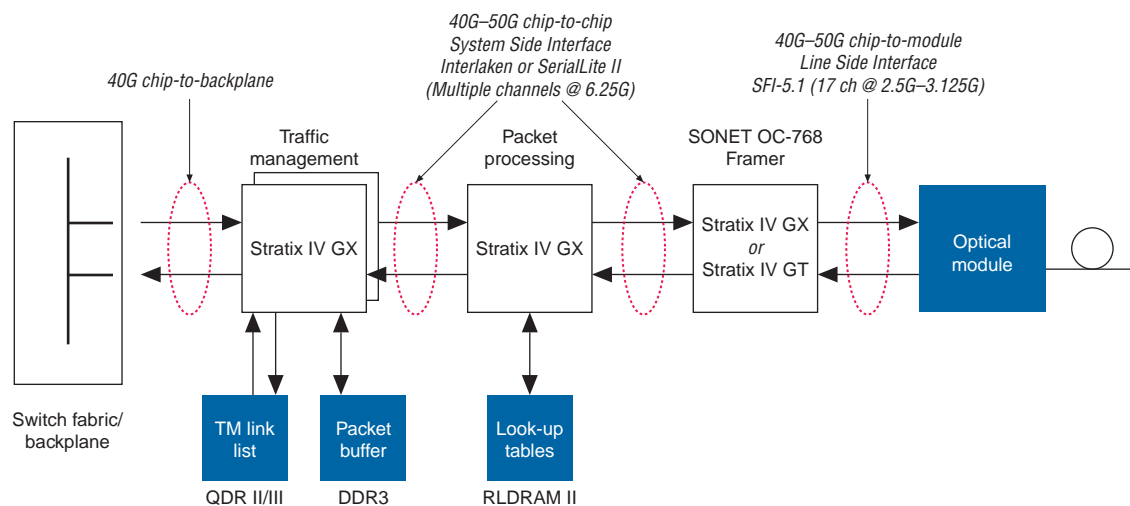
This application note describes how to implement an SFI-5.1 interface using Altera's 40 nm Stratix[®] IV GX and Stratix IV GT devices.

The SFI-5.1 is a chip-to-chip or chip-to-module protocol that targets 40 Gbps applications. The protocol allows up to 25% overhead for forward error correction (FEC) code for a maximum throughput of 50 Gbps.

Both Stratix IV GX and Stratix IV GT devices support SFI-5.1 interfaces using high-speed CDR-based transceivers.

Figure 1 shows a typical OC-768 packet over SONET (POS) line card application that uses a Stratix IV GX device to implement an OC-768 framer and FEC processor. The line-side interface to the 40G optical module uses SFI-5.1, while the system-side interface to the packet processor uses either the industry-standard Interlaken or the proprietary SerialLite II protocol.

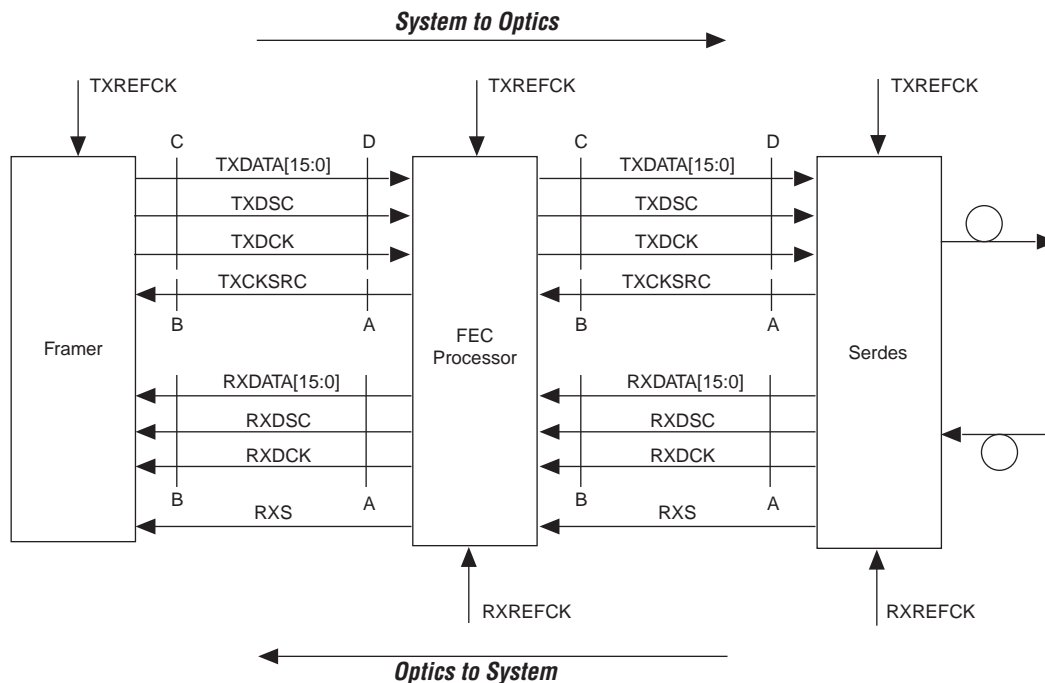
Figure 1. OC-768 Packet Over SONET (POS) Line Card



SFI-5.1 Protocol Reference Model

Figure 2 shows a general SFI-5.1 interface reference model as specified in the SFI-5 implementation agreement by the Optical Internetworking Forum (OIF).

Figure 2. SFI-5.1 Reference Model ⁽¹⁾



Note to Figure 2:

(1) From *Serdes Framer Interface Level 5 (SFI-5): Implementation Agreement for 40Gb/s Interface for Physical Layer Devices*. Optical Internetworking Forum, OIF-SFI5-01.02, January 2002. (www.oiforum.com)

As shown in Figure 2, an SFI-5.1 link supports the following signals:

- Interface Data Signals
 - 16 data channels (TXDATA[15:0] or RXDATA[15:0]), each configured at a data rate between 2.488 Gbps and 3.125 Gbps
 - One deskew channel (TXDSC or RXDSC) configured at the same data rate as the 16 data channels
- Interface Clock Signals
 - One timing reference data clock (TXDCK or RXDCK) signal at one-fourth the data rate
 - Optional transmit clock source (TXCKSRC) signal. The SFI-5 specification optionally allows the sink device in the system-to-optics direction to generate a TXCKSRC signal at a frequency of one-fourth the data rate. If the sink device provides the TXCKSRC signal to the source device, the source device must use this signal as the input reference clock for the TXDATA, TXDSC, and TXDCK signals. Otherwise, the source device must use TXREFCK as the input reference clock for these signals.

- Input Reference Clock Signals
 - Transmitter Reference Clock (TXREFCK)—Input reference clock for the SFI-5.1 interface in the system-to-optics direction at a frequency of one-fourth the data rate
 - Receiver Reference Clock (RXREFCK)—Input reference clock for the SFI-5.1 interface in the optics-to-system direction at a frequency of one-fourth the data rate



Although the SFI-5.1 specification mandates the TXDCK, RXDCK, TXCKSRC, TXREFCK, and RXREFCK signals at a frequency of one-fourth the data rate, these clock signals are typically implemented at a frequency of one-eighth or one-sixteenth the data rate.

- Other Interface Signals
 - Asynchronous Receiver Status (RXS) signal—The SFI-5.1 specification mandates the source device in the optics-to-system direction to generate this receiver status signal. It is optional for the sink device to use this signal.

This application note divides the implementation of an SFI-5.1 link in Stratix IV FPGAs into the following three sections:

- [“Implementing the SFI-5.1 Interface Data Signals”](#)
TXDATA[15:0]/RXDATA[15:0] and TXDSC/RXDSC
- [“Implementing the SFI-5.1 Interface Clock Signals” on page 15](#)
TXDCK/RXDCK and TXCKSRC
- [“Implementing the SFI-5.1 Asynchronous Receiver Status Signal” on page 16](#)
RXS

Implementing the SFI-5.1 Interface Data Signals

The 17 interface data signals (TXDATA[15:0]/RXDATA[15:0] and TXDSC/RXDSC) in the SFI-5.1 link support data rates between 2.488 Gbps and 3.125 Gbps. These 17 interface data signals must be implemented using the CDR-based transceiver channels in Stratix IV GX and Stratix IV GT devices.

The SFI-5 implementation agreement mandates all SFI-5.1 links to be electrically compliant with the OIF-SxI-5 specification, which specifies the maximum transmitter lane-to-lane skew across the 16 data channels and one deskew channel to be 2 UI. To meet the transmitter lane-to-lane skew specification of 2 UI, all 17 transmitter channels must be bonded using the xN clock network. This requires all 17 channels in an SFI-5.1 link to be placed across three adjacent transceiver blocks on the same side (left or right) of the device.



For more information about the xN clock network, refer to the [Stratix IV Transceiver Clocking](#) chapter in volume 2 of the *Stratix IV Device Handbook*.

Each of the following Stratix IV GX and Stratix IV GT devices supports up to two SFI-5.1 links, one on each of the left and right sides of the device:

- Stratix IV GX—EP4SGX180KF40, EP4SGX230KF40, EP4SGX290KF40, EP4SGX360KF40, EP4SGX530KF40, EP4SGX290KF43, EP4SGX360KF43, EP4SGX530KF43, EP4SGX290NF45, EP4SGX360NF45, EP4SGX530NF45
- All Stratix IV GT devices

Recommended Transceiver Configuration for 17 Interface Data Signals

To implement the 17 interface data signals in an SFI-5.1 link with optimum FPGA clock resource utilization, Altera recommends the following transceiver configuration:

- All 17 transmitter channels configured in Basic (PMA Direct) xN mode
- Five of the 17 receiver channels configured in Basic (PMA Direct) x1 mode
- The remaining 12 receiver channels configured in Basic x1 mode with low latency PCS datapath

This implementation requires creating three different ALTGX instances, as follows.

Instance 1: 17 Transmitter Channels in Basic (PMA Direct) xN Mode

Use the ALTGX MegaWizard™ Plug-In Manager to instantiate a 17-channel Basic (PMA Direct) transmitter-only configuration instance (Figure 3).

Figure 3. Instance 1 of the Recommended SFI-5.1 Implementation

As shown in Figure 3, select the following options on the **General** tab:

- Which protocol will you be using?: **Basic (PMA Direct)**
- Which subprotocol will you be using?: **XN**
- What is the operation mode?: **Transmitter only**
- What is the number of channels?: **17**
- What is the deserializer block width?: **Double**
- What is the channel width?: **16**
- What is the effective data rate?: Enter a number from 2488 to 3125, depending on your system requirements
- What is the input clock frequency?: Select from the drop-down list (typically one-eighth or one-sixteenth of the data rate)

If any of the optional dynamic reconfiguration features are enabled, select the following option on the **Reconfig** tab:

- What is the starting channel number? 0

In the other tabs of the ALTGX MegaWizard Plug-In Manager for Instance 1, select the optional transceiver ports you require.

Instance 2: Five Receiver Channels in Basic (PMA Direct) x1 Mode

Use the ALTGX MegaWizard Plug-In Manager to instantiate a 5-channel Basic (PMA Direct) receiver-only configuration (Figure 4).

Figure 4. Instance 2 of the Recommended SFI-5.1 Implementation

As shown in Figure 4, select the following options on the **General** tab:

- Which protocol will you be using?: **Basic (PMA Direct)**
- Which subprotocol will you be using?: **None**
- What is the operation mode?: **Receiver only**
- What is the number of channels?: **5**
- What is the deserializer block width?: **Double**
- What is the channel width?: **16**
- What is the effective data rate?: Enter a number from 2488 to 3125, depending on your system requirements

- What is the input clock frequency?: Select from the drop-down list (typically one-eighth or one-sixteenth of the data rate)

Select the following option on the **Reconfig** tab:

- What is the starting channel number?: 72

In the other tabs of the ALTGX MegaWizard Plug-In Manager for Instance 2, select the optional transceiver ports you require.

Instance 3: 12 Receiver Channels in Basic x1 Mode with Low Latency PCS Datapath

Use the ALTGX MegaWizard Plug-In Manager to instantiate a 12-channel Basic receiver-only configuration (Figure 5).

Figure 5. Instance 3 of the Recommended SFI-5.1 Implementation

As shown in Figure 5, select the following options on the **General** tab:

- Which protocol will you be using?: **Basic**
- Which subprotocol will you be using?: **None**
- What is the operation mode?: **Receiver only**
- What is the number of channels?: **12**
- What is the deserializer block width?: **Double**

- What is the channel width?: **16**
- What is the effective data rate?: Enter a number from 2488 to 3125, depending on your system requirements
- What is the input clock frequency?: Select from the drop-down list (typically one-eighth or one-sixteenth of the data rate)

Select the following option on the **Reconfig** tab:

- What is the starting channel number?: **92**

Select the following option on the **Basic/8B10B** tab:

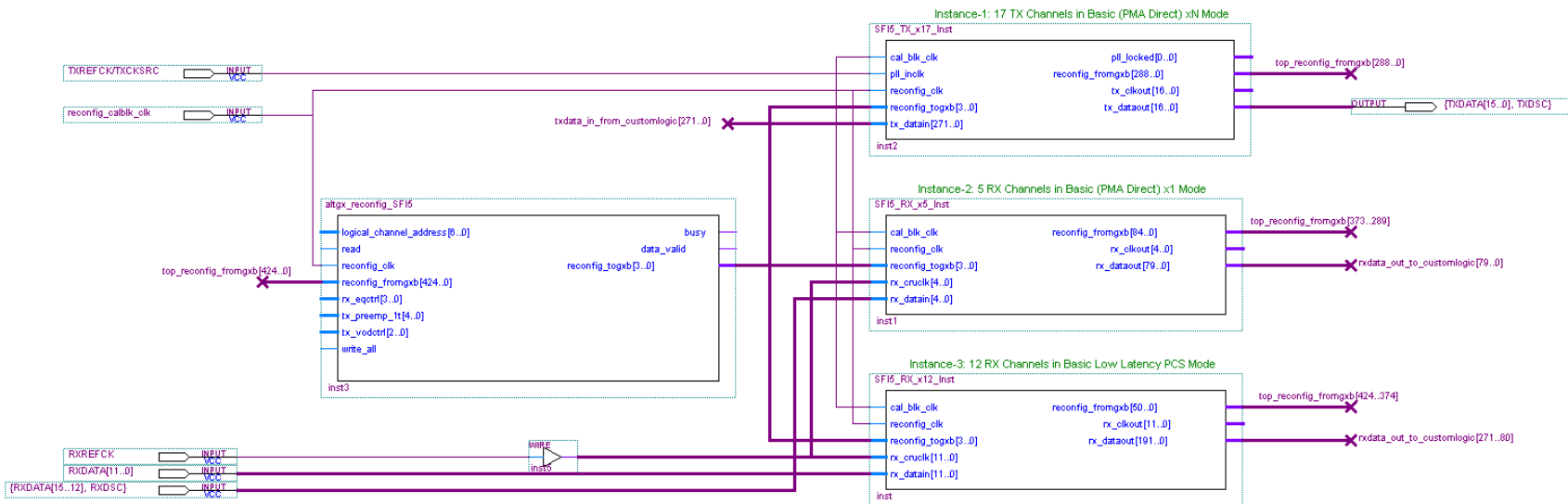
- **Enable Low Latency PCS mode**

In the other tabs of the ALTGX MegaWizard Plug-In Manager for Instance 3, select the optional transceiver ports you require.

Combining the Three Instances

Figure 6 shows a sample schematic of the recommended SFI-5.1 link implemented using these three instances.

Figure 6. Sample Schematic Diagram of the Recommended SFI-5.1 Link Implementation



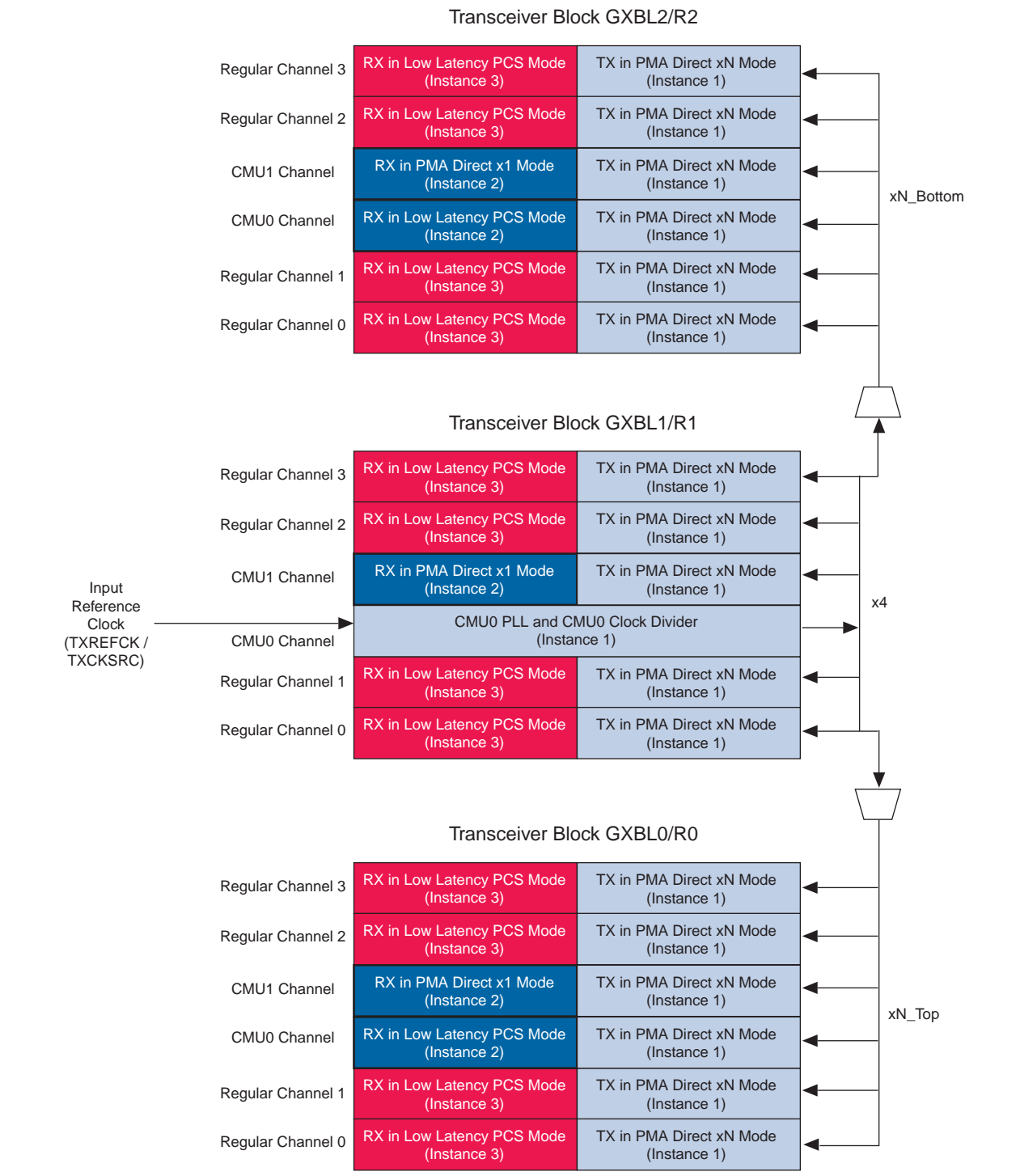
As shown in [Figure 6](#), the transmitter input reference clock `p11_inclk` in Instance 1 can be driven by `TXREFCK` or `TXCKSRC`, depending on your system implementation. The SFI-5 specification requires using `TXCKSRC` as the transmitter input reference clock if the source device in the optics-to-system direction provides this clock to the sink device. If `TXCKSRC` is not provided, the specification allows the sink device to use the `TXREFCK` clock as the input reference clock to the transmitter.

Transceiver Channel Placement for 17 Interface Data Signals

The 16 data channels, `TXDATA[15:0]` or `RXDATA[15:0]`, and one deskew channel, `TXDSC` or `RSDSC`, must be placed in three adjacent transceiver blocks on the same side of the device. To meet the 2 UI transmitter channel-channel skew across all 17 channels, you must use the `CMU0 PLL` in the middle transceiver block to generate the transmitter clocks.

Figure 7 shows the transceiver channel and CMU PLL placement requirements to implement an SFI-5.1 link in a Stratix IV GX or Stratix IV GT device with three transceiver blocks on the same side of the device. You can achieve the illustrated transceiver channel and CMU PLL placement by making the appropriate pin assignments in the Quartus® II software.

Figure 7. Transceiver Channel and CMU PLL Placement Requirements for SFI-5.1 Implementation



Lane-to-Lane Skew Consideration

The transmitter channel placement and clocking for the 16 data channels (TXDATA[15:0] or RXDATA[15:0]) and one deskew channel (TXDSC/RXDSC) shown in [Figure 8](#) ensures that the maximum transmitter lane-to-lane skew specification of 2 UI is met.

The interconnect between the source and the sink device may add up to 3 UI for a total of 5 UI lane-to-lane skew at the receiver input pins. Additionally, the SFI-5.1 receiver channel implementation shown in [Figure 8](#) could add up to 16 UI lane-to-lane skew. Implement the deskew controller in the FPGA fabric, allowing for both the interconnect skew and the skew added by the receiver channels.

FPGA Fabric-Transceiver Interface Clocking

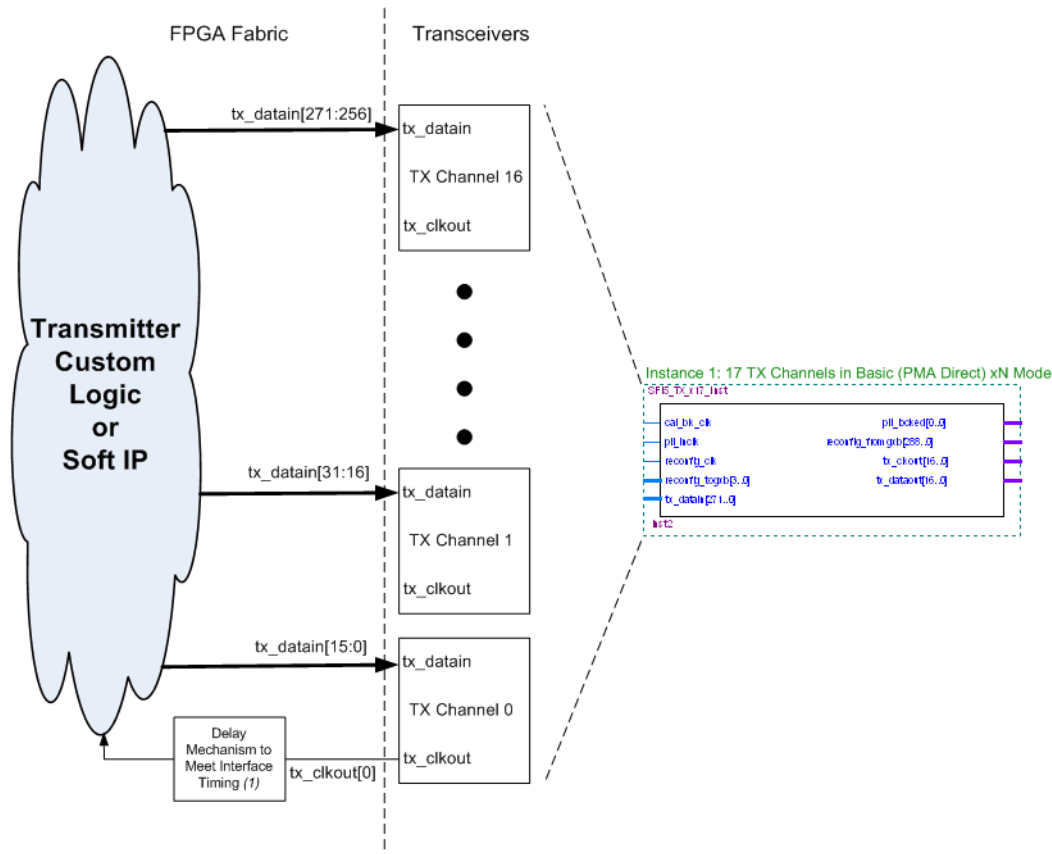
The following sections provide the recommended FPGA fabric-transceiver interface clocking for an SFI-5.1 link implementation:

- [“FPGA Fabric-Transmitter Interface Clocking”](#)
- [“FPGA Fabric-Receiver Interface Clocking”](#) on page 14

FPGA Fabric-Transmitter Interface Clocking

Figure 8 shows the FPGA fabric-transmitter interface clocking scheme recommended for SFI-5.1 implementation.

Figure 8. Recommended FPGA Fabric-Transmitter Interface Clocking in an SFI-5.1 Implementation




Note to Figure 8:

- (1) A certain amount of phase shift in the FPGA fabric-transmitter interface clock may be required in -3 and -4 speed grade Stratix IV GX devices to meet interface timing.

As shown in Figure 8, Instance 1 provides a tx_clkout signal on each of the 17 transmitter channels that form the SFI-5.1 link. You can choose any one of the 17 tx_clkout signals to clock the custom logic or soft IP that drives the parallel transmitter data into the tx_datain port. The example clocking scheme shown in Figure 8 uses tx_clkout[0] for this purpose.

To meet the interface timing requirements between the FPGA fabric and the transmitter channels, you may need to introduce some phase shift in the FPGA fabric-transmitter interface clock tx_clkout used to clock the custom logic or soft IP. This phase shift is required only in -3 and -4 speed grade Stratix IV GX devices above data rates of 2.88 Gbps and 2.56 Gbps, respectively.

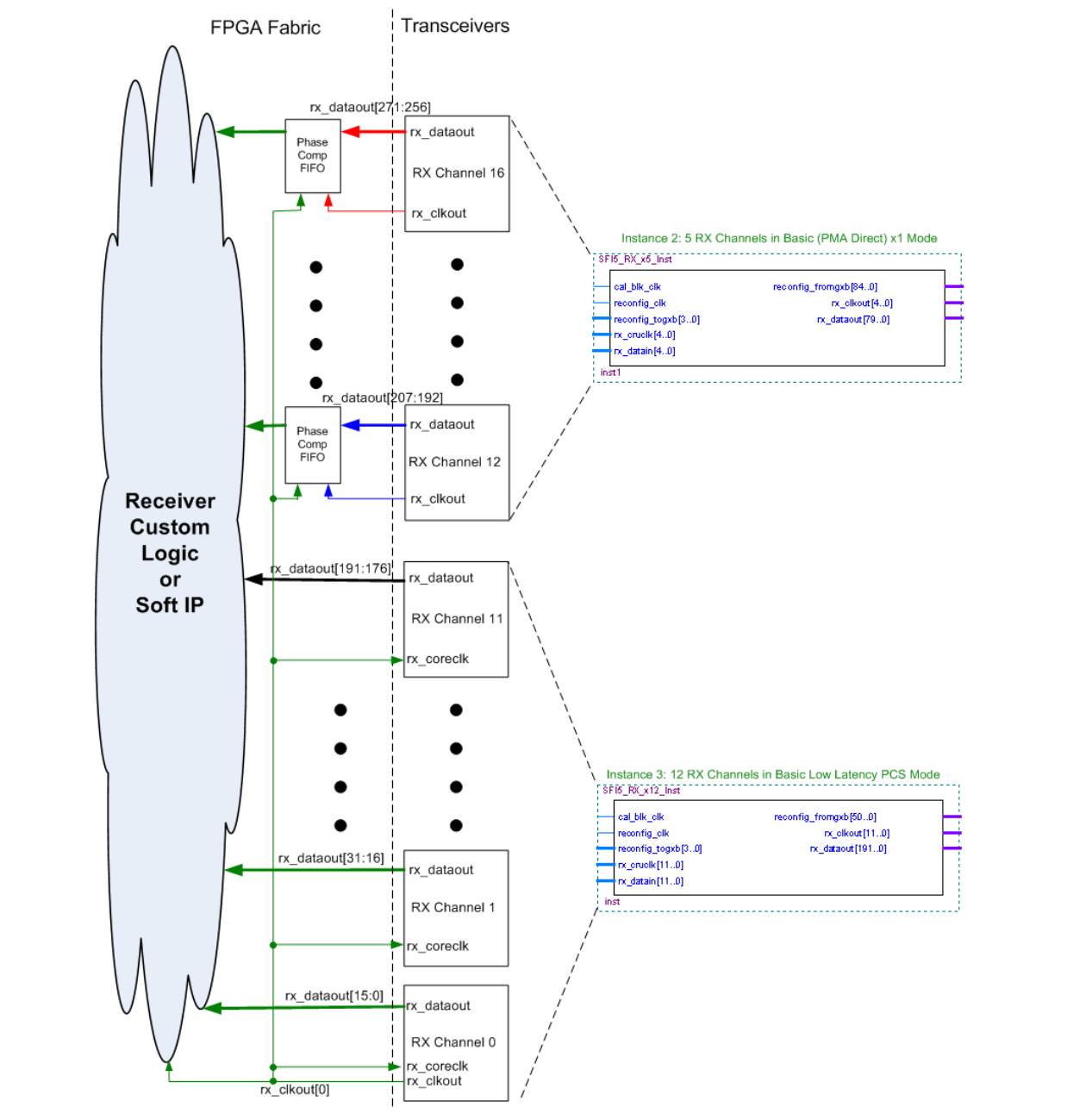
 For more details about implementing the required delay mechanism, refer to [AN 580: Achieving Timing Closure in Basic \(PMA Direct\) Functional Mode](#).

FPGA Fabric-Receiver Interface Clocking

Each of the 17 SFI-5.1 receiver channels instantiated using Instance 2 and Instance 3 provides a recovered clock `rx_clkout` signal to the FPGA fabric. Any of the 17 `rx_clkout` signals can be used to clock the receiver side custom logic or soft IP in the FPGA fabric. A phase compensation FIFO is required per channel to compensate for the phase difference between its own recovered clock and the one used to clock the custom logic or soft IP in the FPGA fabric.

Figure 9 shows the FPGA fabric-receiver interface clocking scheme recommended for SFI-5.1 link implementation.

Figure 9. Recommended FPGA Fabric-Receiver Interface Clocking in an SFI-5.1 Implementation



Five of the 17 SFI-5.1 receiver channels are configured in Basic (PMA Direct) mode using Instance 2. Because these five channels do not have a phase compensation FIFO in the receiver datapath, a phase compensation FIFO must be implemented in the FPGA fabric for each of these five channels, as shown in Figure 9.

The remaining 12 channels are configured in Basic mode with a low latency PCS datapath using Instance 3. The phase compensation FIFO in the receiver PCS of each of these 12 channels is used to compensate for the phase difference between its recovered clock and the one used to clock the custom logic or soft IP in the FPGA fabric. To achieve this, you must enable the `rx_coreclk` port in Instance 3 and drive each `rx_coreclk` port with the `rx_clkout` signal used to clock the custom logic or soft IP in the FPGA fabric, as shown in Figure 9. You must also make the following Quartus II assignments when using this recommended scheme for FPGA fabric-receiver interface clocking.

Table 1. Recommended FPGA Fabric-Transmitter Interface Clocking in an SFI-5.1 Implementation

Variable	Value
From	<code>rx_clkout</code> signal used to clock the receiver side custom logic or soft IP in the FPGA fabric
To	<code>rx_datain</code> pins of all 12 channels in Instance 3
Assignment Name	GXB 0 PPM Core Clock Setting
Assignment Value	On

Implementing the SFI-5.1 Interface Clock Signals

The SFI-5 protocol specifies that the source device in the system-to-optics direction generates a transmit data clock (TXDCK) signal that is frequency locked to the TXDATA[15:0] and TXDSC signals. The protocol also specifies that the source device in the optics-to-system direction generates a receive data clock (RXDCK) signal that is frequency locked to the RXDATA[15:0] and RXDSC signals. It does not specify any phase relationship between the TXDCK and TXDATA signals or the RXDCK and RXDATA signals.

Also, the SFI-5 protocol allows the sink device in the optics-to-system direction to optionally generate a transmit clock source (TXCKSRC) and forward it to the source device. If the sink device forwards the TXCKSRC signal to the source device, the source device must use it as the input reference clock for its transmitter PLL.



Although the SFI-5 protocol specifies the TXDCK, RXDCK, and TXCKSRC signals at a frequency of one-fourth the data rate, these clock signals are typically implemented at a frequency of one-eighth or one-sixteenth the data rate.

Altera recommends using LVDS I/Os located in the row I/O banks on the left or right side of the device for the TXDCK, RXDCK, and TXCKSRC signals. For an SFI-5.1 link in the system-to-optics direction, drive the LVDS row I/O assigned for TXDCK with the `tx_clkout[0]` signal from Instance 1. For an SFI-5.1 link in the optics-to-system direction, drive the LVDS row I/Os assigned for RXDCK and TXSRC with the `tx_clkout[0]` signal from Instance 1. The `tx_clkout[0]` signal operates at a frequency of one-sixteenth the data rate.

Implementing the SFI-5.1 Asynchronous Receiver Status Signal

The SFI-5 protocol specifies that the source device in the optics-to-system direction generates an asynchronous receiver status (RXS) signal. The source device asserts this signal to indicate to the sink device that the RXDCK and RXDATA signals are not derived from the optical receive signal.

Altera recommends using any user I/O pin in the row or column I/O banks and assigning the LVCMOS standard to it.

Summary

This application note discussed the Altera-recommended implementation of the SFI-5.1 link for 40 Gbps systems in Stratix IV GX and Stratix IV GT devices.

Referenced Document

This application note refers to the following document:

- *Serdes Framer Interface Level 5 (SFI-5): Implementation Agreement for 40Gb/s Interface for Physical Layer Devices*. Optical Internetworking Forum, OIF-SFI5-01.02, January 2002. (www.oiforum.com)

Document Revision History

Table 2 lists the revision history for this document.

Table 2. Document Revision History

Date	Version	Changes
March 2012	1.1	Updated "Starting Channel Number."
June 2009	1.0	Initial release.