AN 557: Stratix III-to-Stratix IV E Cross-Family Migration Guidelines

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Introduction

This application note provides guidelines in cross-family migration designs between the Altera® Stratix® III and Stratix IV E device family variant using the Quartus® II software. Use these guidelines for drop-in replacement of either device placed on a single PCB through your hardware design. Altera recommends using the following guidelines throughout your PCB design process to ensure a seamless migration of designs from Stratix III-to-Stratix IV E devices.

You can design your Stratix III FPGAs to take advantage of the higher performance, higher density, and lower power benefits of Stratix IV E FPGAs. With up-front planning that considers the different power supply voltages and available packages in both families, it is possible to design a PCB assembled with either a Stratix III or a Stratix IV E device in the same package.

Cross-family migration between Stratix III and Stratix IV E FPGAs allows you to design with Stratix III FPGAs today and move to Stratix IV E FPGAs in the future without changing the device pin-outs or the PCB layout.

Cross-Family Migration Overview

Cross-family migration is supported between the Stratix III and Stratix IV E device families, targeting device packages that are pin-to-pin compatible across the two families. This allows you to migrate an existing design already compiled for a Stratix III device to a Stratix IV E device with pin-out compatibility. A single PCB is designed to switch between a Stratix III and Stratix IV E device on the same board.

Supported Migration Device Packages

Table 1 lists the various migration paths supported between the Stratix III and Stratix IV E device packages.

Table 1. Stratix III-to-Stratix IV E Device Vertical Migration Package Options

Device		User I/Os, LVDS Count *(Note 1)*, *(2)*, *(3)*			
		F780 (29 mm)	F1152 (35 mm)	F1517 (40 mm)	F1760 (43 mm)
Stratix III	EP3SL50	488, 56	—	—	—
	EP3SL70	488, 56	—	—	—
	EP3SL110	488, 56	744, 88	—	—
	EP3SL150	488, 56	744, 88	—	—
	EP3SL200	488, 56 *(4)*	744, 88	976, 112	—
	EP3SL340	—	744, 88 *(5)*	976, 112	1,120, 132
	EP3SE50	488, 56	—	—	—
	EP3SE80	488, 56	744, 88	—	—
	EP3SE110	488, 56	744, 88	—	—
	EP3SE260	488, 56 *(4)*	744, 88	976, 112	—
Stratix IV E	EP4SE230	488, 56	—	—	—
	EP4SE360	488, 56 *(4)*	744, 88	—	—
	EP4SE530	—	744, 88 *(7)*	976, 112 *(7)*	976, 112 *(8)*
	EP4SE820 *(6)*	—	744, 88 *(7)*	976, 112 *(7)*	1,120, 132

Notes to Table 1:

(1) All devices are offered in flip chip ball-grid array (BGA) with 1.0-mm pitch.

(2) For each device package, the first number indicates the number of I/Os; the second number indicates the LVDS count. The user I/O count includes all general purpose I/Os, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the user I/O count.

(3) Device packages in the same column and marked under the same arrow sign have vertical migration capability.

(4) The 780-pin EP3SL200, EP3SE260, and EP4SE360 devices are only available in the 33-mm × 33-mm hybrid flip chip package.

(5) The 1152-pin EP3SL340 device is only available in the 40-mm × 40-mm hybrid flip chip package.

(6) Due to its large configuration file size, the EP4SE820 device is not currently supported by serial configuration devices. Altera recommends using the JTAG, passive serial (PS), or fast passive parallel (FPP) configuration schemes to allow vertical migration from the Stratix III device to a EP4SE820 device.

(7) The 1152-pin and 1517-pin EP4SE530 and EP4SE820 devices are only available in the 42.5-mm × 42.5-mm hybrid flip chip package.

(8) The 1760-pin EP4SE530 device has fewer user-available I/O pins when compared with the EP3SL340 device of the same package. For more information about the availability of I/O banks and user I/O pins, refer to the *Stratix III Device Pin-Outs* and *Stratix IV Device Pin-Outs*.

Differences Between Stratix III and Stratix IV E Devices

Similar to Stratix III devices, all device densities in the Stratix IV device family that are available in the same package are vertically migratable. Pin-outs for Stratix IV E devices are designed to allow design migrations between the Stratix III and Stratix IV E devices with a common PCB with minimal impact on the power supply design.

If you are designing a PCB for both Stratix III and Stratix IV E devices, you must consider the power supply requirements.

Table 2 lists the similarities and differences in power supplies between the Stratix III and Stratix IV E devices.

Table 2. Stratix III and Stratix IV E Power Supply Requirements

Power Pin	Description	Stratix III Device (V)	Stratix IV E Device (V)
VCCL *(1)*	Core voltage power supply	0.9 or 1.1	Combined 0.9
VCC *(1)*	Periphery circuitry power supply	1.1	
VCCIO [1..8] [A, B, C] *(2)*	I/O supply voltage for banks 1 through 8	1.2 to 3.3	1.2 to 3.0
VCCA_PLL [L[1:4], R[1:4], T[1:2], B[1:2]]	Analog power for PLLs [L[1:4], R[1:4], T[1:2], B[1:2]]	2.5	2.5
VCCD_PLL [L[1:4], R[1:4], T[1:2], B[1:2]]	Digital power for PLLs [L[1:4], R[1:4], T[1:2], B[1:2]]	1.1	0.9
VCCPT	Programmable power technology power supply	2.5	1.5
VCCAUX *(3)*	Programmable power technology second supply	Not required	2.5
VCCPGM *(2)*	Configuration pins power supply	1.8 to 3.3	1.8 to 3.0
VCCPD [1..8][A, B, C] *(2)*	I/O pre-driver power supply	2.5 to 3.3	2.5 to 3.0
VCCBAT	Battery back-up power supply for design security volatile key register	1.2 to 3.3	1.2 to 3.3
VCC_CLKIN [3, 4, 7, 8]	Differential clock input power supply for top and bottom I/O banks	2.5	2.5

Notes to Table 2:

(1) Stratix III devices have separate V_{CC} and V_{CCL} power supplies. Stratix IV E devices combine V_{CC} and V_{CCL} power supplies into a single 0.9-V V_{CC} power supply.

(2) All 3.3-V power supplies for Stratix III devices become 3.0-V power supplies for Stratix IV E devices.

(3) Some of the V_{CCPT} power pins in the Stratix III devices become V_{CCAUX} power pins in the Stratix IV E devices. For more information about the affected pins, refer to "V_{CCPT} and V_{CCAUX} Power Pins" on page 5.

The largest serial configuration device currently supports 128 MBits of configuration bitstream. The EP4SE820 device is not currently supported by the fast active serial (FAS) configuration scheme due to the unavailability of serial configuration devices that can support the large configuration file size.

Altera recommends using the JTAG, PS, or FPP configuration schemes to perform vertical migration from the Stratix III device to a EP4SE820 device.

For more information about the configuration schemes supported by Stratix IV E devices, refer to the *Configuration, Design Security, and Remote System Upgrades* chapter in volume 1 of the *Stratix IV Device Handbook*.

Board Design Considerations

Use the following guidelines if you are designing a board that accommodates Stratix III and Stratix IV E devices:

- Review the power pin connections for Stratix III and Stratix IV E devices to determine if the power supply requirements and the voltage inputs that share supplies.
- If necessary, re-design the voltage regulators and passive components on the board to handle the different supply voltage and current requirements.
- Take extra care when working with the keep-out area of the board if the Stratix III device is in a fineline BGA package and the Stratix IV E device is in a hybrid BGA package.
- Stratix IV E devices provide full support for 3.3-V LVTTL and LVCMOS I/O standards on their input and output levels if you are using 3.0-V V_{CCIO}.

For more information about the power supply requirements and pin connections, refer to the *Stratix III Device Family Pin Connection Guidelines* and *Stratix IV Device Family Pin Connection Guidelines*.

For more information about I/O standard specifications, refer to the *DC and Switching Characteristics* chapter in volume 4 of the *Stratix IV Device Handbook*.

Power Pin Connections

Altera recommends verifying that you have correctly connected all the power planes. You must identify any unique requirements for the power pins on your board or devices that can share the same power rail.

The following sections describe the supply voltage requirements for specific power pins in Stratix III and Stratix IV E devices.

V_{CC} and V_{CCL} Power Pins

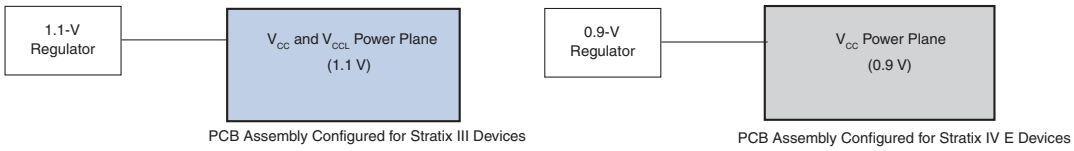
Stratix III devices have separate V_{CC} and V_{CCL} power supplies; Stratix IV E devices combine V_{CC} and V_{CCL} power supplies into a single V_{CC} power supply. Therefore, if you are migrating your design from a Stratix III to a Stratix IV E device, the V_{CC} and V_{CCL} power pins in the Stratix III device become the V_{CC} power pin in the Stratix IV E device.

Although Stratix III devices have separate V_{CC} and V_{CCL} power supplies, Altera recommends supplying a common voltage of 1.1 V to both V_{CC} and V_{CCL} power supplies for the Stratix III device if your design uses a single PCB to assemble both Stratix III and Stratix IV E devices. You must replace the 1.1-V power supply to both V_{CC} and V_{CCL} power pins for the Stratix III device with a 0.9-V power supply for the V_{CC} power pin if your design has the PCB assembled with the Stratix IV E device.

Because of the high current drawn, Altera does not recommend using isolated 1.1-V V_{CC} and 0.9-V V_{CCL} power supplies for Stratix III devices and connecting them to the 0.9-V V_{CC} power pin on the Stratix IV E device on the same board.

Figure 1 shows the recommended V_{CC} and V_{CCL} power supply requirements on the same board.

Figure 1. Recommended V_{CC} and V_{CCL} Power Supply Requirements on the Same Board *(Note 1)*



Note to Figure 1:

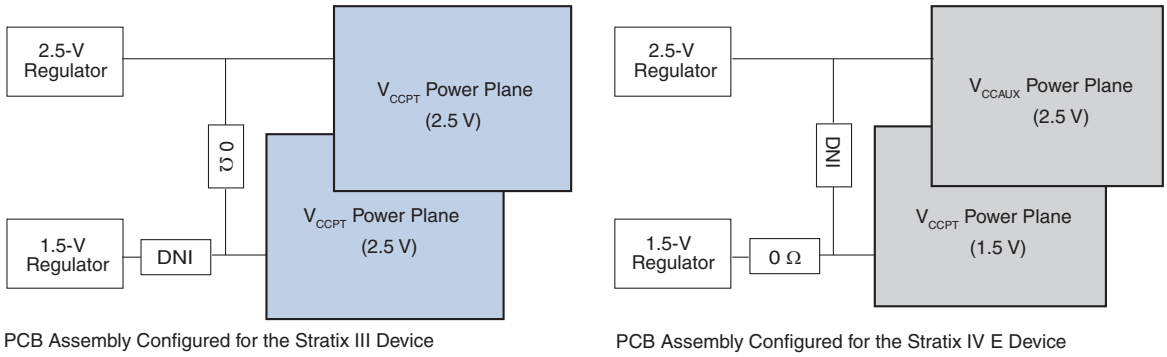
(1) If the Stratix III device design has a common plane for V_{CC} and V_{CCL} power plane (1.1 V), you must change the regulator output voltage for the Stratix IV E device (0.9 V).

V_{CCPT} and V_{CCAUX} Power Pins

To accommodate the Stratix IV E device on the same board as the Stratix III device, you must split the V_{CCPT} 2.5-V power supply for the Stratix III device into two separate power planes of 1.5 V and 2.5 V in the Stratix IV E device for the V_{CCPT} and V_{CCAUX} power supplies, respectively. When designing your board layout, you must isolate the V_{CCPT} and V_{CCAUX} power supplies for the Stratix IV E device and tie them together on the Stratix III device.

Figure 2 shows the V_{CCPT} and V_{CCAUX} power supply requirements on the same board.

Figure 2. V_{CCPT} and V_{CCAUX} Power Supply Requirements on the Same Board *(Note 1)*, *(2)*



Notes to Figure 2:

(1) V_{CCPT} and V_{CCAUX} are shown as separate power planes, but they can be islands on a single plane.

(2) This PCB layout shows two different methods of assembling the Stratix III and Stratix IV E devices on the same board. Alternative schemes are possible.

Table 3 through Table 6 list the pin names and functions of the VCCPT and VCCAUX power pins in Stratix III and Stratix IV E devices of the various packages.

Table 3 lists the pin names and functions of the VCCPT and VCCAUX power pins in an F780/H780 package for Stratix III and Stratix IV E devices.

Table 3. Pin Names and Functions of the VCCPT and VCCAUX Power Pins in an F780/H780 Package for Stratix III and Stratix IV E Devices

Pin Number	Stratix III Device		Stratix IV E Device	
	Pin Name/Function	Voltage (V)	Pin Name/Function	Voltage (V)
G23	VCCPT	2.5	VCCAUX	2.5
AC23	VCCPT	2.5	VCCAUX	2.5
AB6	VCCPT	2.5	VCCAUX	2.5
G6	VCCPT	2.5	VCCAUX	2.5
R24	VCCPT	2.5	VCCPT	1.5
AD15	VCCPT	2.5	VCCPT	1.5
P5	VCCPT	2.5	VCCPT	1.5
E14	VCCPT	2.5	VCCPT	1.5
M9	No Connect	—	VCCPT	1.5
U20	No Connect	—	VCCPT	1.5

Table 4 lists the pin names and functions of the VCCPT and VCCAUX power pins in an F1152/H1152 package for Stratix III and Stratix IV E devices.

Table 4. Pin Names and Functions of the VCCPT and VCCAUX Power Pins in an F1152/H1152 Package for Stratix III and Stratix IV E Devices

Pin Number	Stratix III Device		Stratix IV E Device	
	Pin Name/Function	Voltage (V)	Pin Name/Function	Voltage (V)
J27	VCCPT	2.5	VCCAUX	2.5
AG27	VCCPT	2.5	VCCAUX	2.5
AG7	VCCPT	2.5	VCCAUX	2.5
H8	VCCPT	2.5	VCCAUX	2.5
U29	VCCPT	2.5	VCCPT	1.5
AJ17	VCCPT	2.5	VCCPT	1.5
V6	VCCPT	2.5	VCCPT	1.5
F18	VCCPT	2.5	VCCPT	1.5
AC10	No Connect	—	VCCPT	1.5
M25	No Connect	—	VCCPT	1.5

Table 5 lists the pin names and functions of the VCCPT and VCCAUX power pins in an F1517/H1517 package for Stratix III and Stratix IV E devices.

Table 5. Pin Names and Functions of the VCCPT and VCCAUX Power Pins in an F1517/H1517 Package for Stratix III and Stratix IV E Devices

Pin Number	Stratix III Device		Stratix IV E Device	
	Pin Name/Function	Voltage (V)	Pin Name/Function	Voltage (V)
J32	VCCPT	2.5	VCCAUX	2.5
AL32	VCCPT	2.5	VCCAUX	2.5
AL8	VCCPT	2.5	VCCAUX	2.5
J8	VCCPT	2.5	VCCAUX	2.5
Y33	VCCPT	2.5	VCCPT	1.5
AL20	VCCPT	2.5	VCCPT	1.5
Y7	VCCPT	2.5	VCCPT	1.5
J20	VCCPT	2.5	VCCPT	1.5
T13	No Connect	—	VCCPT	1.5
AD27	No Connect	—	VCCPT	1.5

Table 6 lists the pin names and functions of the VCCPT and VCCAUX power pins in an F1760 package for Stratix III and Stratix IV E devices.

Table 6. Pin Names and Functions of the VCCPT and VCCAUX Power Pins in an F1760 Package for Stratix III and Stratix IV E Devices

Pin Number	Stratix III Device		Stratix IV E Device	
	Pin Name/Function	Voltage (V)	Pin Name/Function	Voltage (V)
L33	VCCPT	2.5	VCCAUX	2.5
AM34	VCCPT	2.5	VCCAUX	2.5
AN9	VCCPT	2.5	VCCAUX	2.5
K9	VCCPT	2.5	VCCAUX	2.5
AA33	VCCPT	2.5	VCCPT	1.5
AM22	VCCPT	2.5	VCCPT	1.5
AB11	VCCPT	2.5	VCCPT	1.5
L21	VCCPT	2.5	VCCPT	1.5
AB13	No Connect	—	VCCPT	1.5
AB30	No Connect	—	VCCPT	1.5

User I/O Pins

If you are migrating from the EP3SL340 device to the EP4SE530 device in the F1760 package, be aware that there are fewer user-available I/O pins in the F1760-pin EP4SE530 devices.

The number of I/O banks in the EP4SE530 device is similar to the EP3SL340 device in the F1760 package. However, the EP4SE530 device has 144 fewer user-available I/O pins than the EP3SL340 device. The unavailable I/O pins in the EP4SE530 device appear as "No Connect" in the pin-out files.

Table 7 compares the number of I/O pins in each bank of the EP3SL340 and EP4SE530 devices in the F1760 package. Both devices have 24 I/O banks, but 12 of these banks have fewer I/Os in the EP4SE530 device.

Table 7. Number of I/Os and I/O Banks in the F1760 Package for Stratix III and Stratix IV E Devices

Pin Function	EP3SL340		EP4SE530	
	I/O Bank	Number of I/Os	I/O Bank	Number of I/Os
I/O	1A	50	1A	50
I/O	1B	36	1B	24
I/O	1C	50	1C	42
I/O	2A	50	2A	50
I/O	2B	36	2B	24
I/O	2C	50	2C	42
I/O	3A	48	3A	48
I/O	3B	48	3B	48
I/O	3C	48	3C	32
I/O	4A	48	4A	48
I/O	4B	48	4B	48
I/O	4C	48	4C	32
I/O	5A	50	5A	50
I/O	5B	36	5B	24
I/O	5C	50	5C	42
I/O	6A	50	6A	50
I/O	6B	36	6B	24
I/O	6C	50	6C	42
I/O	7A	48	7A	48
I/O	7B	48	7B	48
I/O	7C	48	7C	32
I/O	8A	48	8A	48
I/O	8B	48	8B	48
I/O	8C	48	8C	32
Total User I/Os		1120		976

For more information about the availability of I/O banks, user I/O pins, and the DQ and DQS pins, refer to the *Stratix III Device Pin-Outs* and *Stratix IV Device Pin-Outs*.

DQ and DQS Pins

Designs with external memory interfaces using DQ and DQS pins require extra attention because the DQ and DQS pin assignments may be different in the Stratix IV E devices that have fewer I/O pins.

If you plan to migrate from a Stratix III device to a Stratix IV E device that has fewer user I/O pins, it is very important that you exclude the unavailable I/O pins in the Stratix IV E device from any external memory interfaces.

If you are planning to migrate from the EP3SL340 device to the EP4SE530 device in the F1760 package, you must pay attention to the external memory interface designs. The EP4SE530 device has 12 I/O banks with fewer I/O pins than the EP3SL340 device.

To ensure successful migration, Altera recommends planning your memory interface designs using the DQ and DQS pins capability of the Stratix IV E device (which has fewer I/Os). When designing your memory interface, consider each device before you make your final pin assignments. You must verify your design in the Quartus II software for each device before you finalize the pin assignments.

For more information about the number of DQ and DQS groups that are available in the Stratix III and Stratix IV E devices, refer to the *External Memory Interfaces* chapter in the *Stratix III Device Handbook* and *Stratix IV Device Handbook,* respectively.

You can assemble the PCBs that are designed to these guidelines with either Stratix III or Stratix IV E devices. Existing Stratix III device PCBs that are not designed to these guidelines cannot be assembled with Stratix IV E devices.

Quartus II Software Device Migration Flow

This section describes the Stratix III-to-Stratix IV E cross-family migration flow methodology in the Quartus II software.

To perform cross-family migration, perform the following steps:

1. Compile the user design targeted for a Stratix III device. Perform design synthesis and fitting.
2. Back-annotate the pin assignments.
3. Change the target device from Stratix III to **Stratix IV E** and incorporate the pin assignments from step 2.
4. Recompile the design for the Stratix IV E device.

The following sections describe the Quartus II software GUI migration flow of each step.

Compiling a Design for a Stratix III Device

As mentioned in Step 1 above, first compile your design targeting a Stratix III device. If you have an existing pre-compiled design in a different Quartus II software version, at a minimum, you must perform design synthesis and fitting again before you perform migration.

To compile the design, perform the following steps:

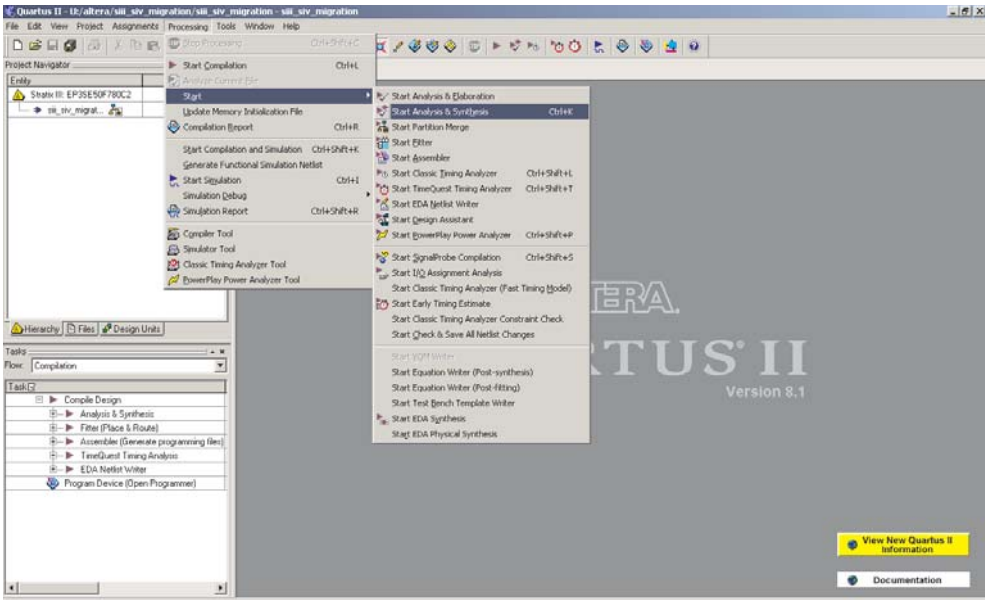
1. On the Processing menu, point to **Start** and click **Start Compilation** (Figure 3).

To only perform synthesis and fitting on your design, on the Processing menu, point to **Start** and click **Start Analysis & Synthesis**.

2. After you have successfully synthesized your design, on the Processing menu, point to **Start** and click **Start Fitter**.

Alternatively, you can perform compilation, synthesis, or fitting on your design by clicking on the Tasks window in the Quartus II software.

Figure 3. Design Compilation for a Stratix III Device

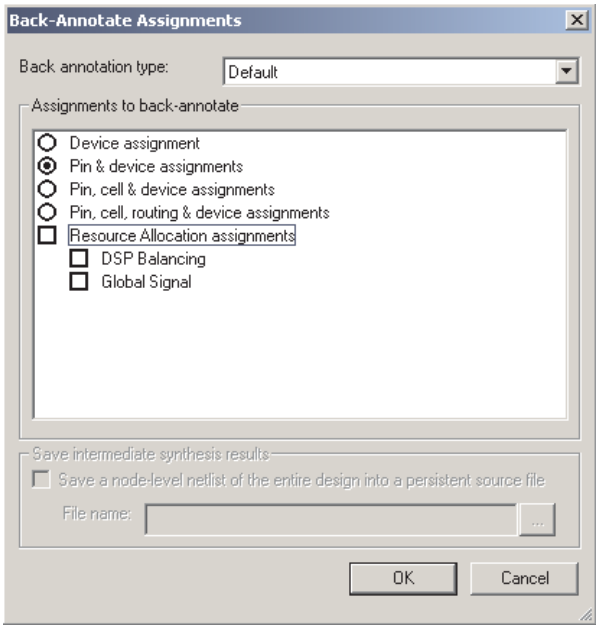


Back-Annotate Pin Assignments

To back-annotate your pin assignments, perform the following steps:

1. On the Assignments menu, click **Back-Annotate Pin Assignments**.
2. In the **Back Annotation Type** pull-down list, select **Default**.
3. In the **Back-Annotation Assignments** dialog box, select **Pin & device assignments** (Figure 4).
4. Click **OK**.

Figure 4. Selections in the Back-Annotation Assignments Dialog Box



Back-annotation results are not immediately visible in the Quartus II Settings File (**.qsf**). Changes are reflected after subsequent Quartus II software processing or after you have re-opened the design project.

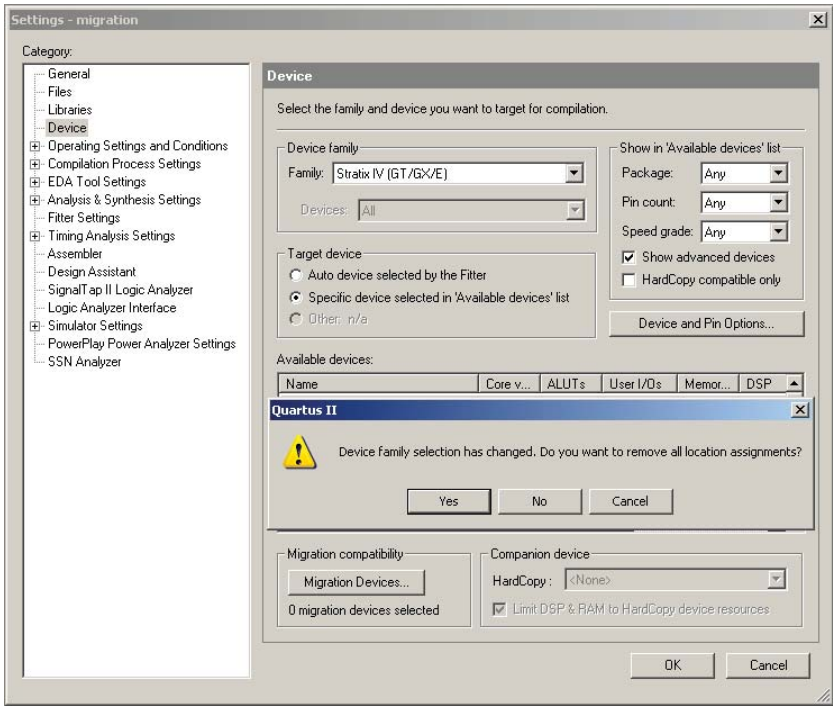
Migrating Your Design from a Stratix III to a Stratix IV E Device

You must select a target Stratix IV E device for compilation in the Quartus II software.

To change the targeted device family from Stratix III to Stratix IV E, perform the following steps:

1. On the Assignments menu, click **Device**.
2. In the **Settings** dialog box, select **Stratix IV (GT/GX/E)** in the **Device Family** pull-down list.
3. A **Removal of All Location Assignments** pop-up dialog box requesting clarification appears. Click **No** (Figure 5).

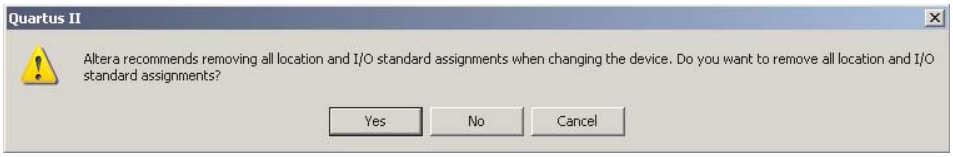
Figure 5. Settings and Removal of Location Assignments Dialog Box in the Quartus II Software



4. Under the **Available devices** list, select the necessary Stratix IV E device in the correct package, pin count, and speed grade that you intend to migrate to. You can filter the **Available devices** list to select the migration device under the **Show in 'Available devices' list** option.
5. After you have selected the necessary Stratix IV E device density for migration, a **Removal of All Location and I/O Standard Assignments** pop-up dialog box requesting confirmation appears. Click **No** (Figure 6).
6. Click **OK** to close the dialog box after selecting the device.

For more information about the supported cross-family migration devices in different packages, refer to Table 1 on page 2.

Figure 6. Removal of All Location and I/O Standard Assignments Dialog Box



Recompiling Your Design for a Stratix IV E Device

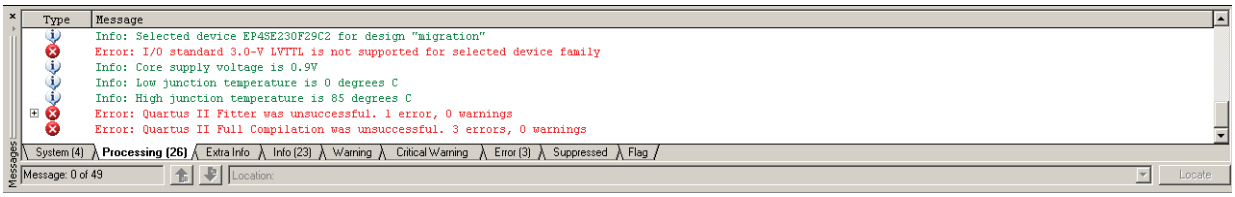
To recompile the design for the Stratix IV E device, perform the following step:

1. On the Processing menu, click **Start Compilation**.

During compilation, the Quartus II software issues I/O standard and I/O voltage incompatibility errors between the Stratix III and Stratix IV E devices. The Stratix IV E device does not support the 3.0-V LVTTL/LVCMOS I/O standard that you can use in a Stratix III device.

Figure 7 shows the Quartus II software error message if the I/O standard setting is not supported by the device family after you have completed cross-family migration.

Figure 7. I/O Standard Setting Error Message in the Quartus II software

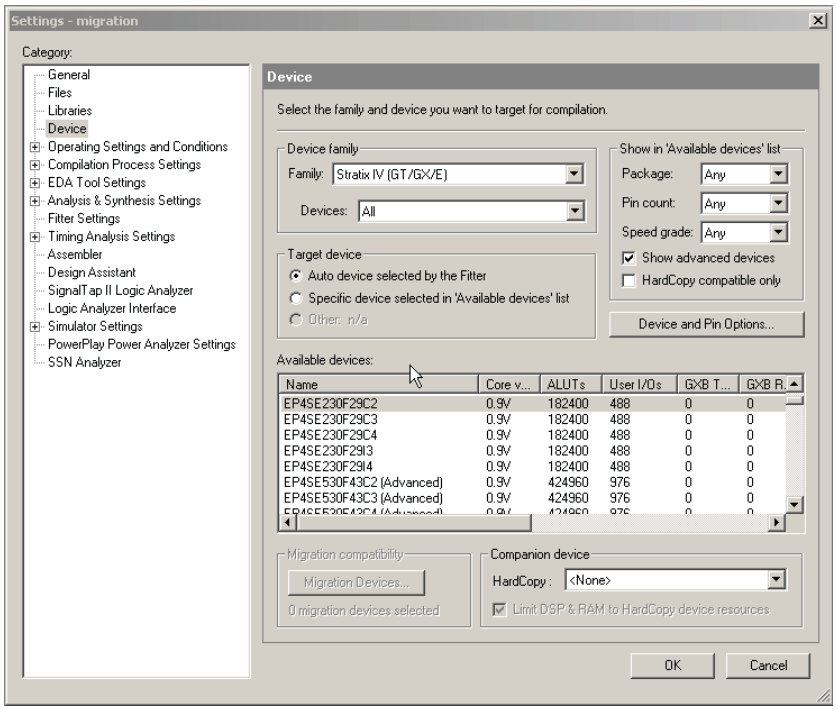


The Quartus II software default global I/O standard setting for new projects that target a Stratix III device is 2.5 V, unless you manually change this setting. If you use a global setting of **3.0-V LVTTL/LVCMOS** as your default I/O standard in your Stratix III device, you must change this setting to a global setting of **3.3-V LVTTL/LVCMOS** I/O standard in your Stratix IV E device. This accounts for the differences in the Stratix IV E device when compared with the Stratix III device.

To change the 3.0-V I/O standard setting in the Stratix III device to the 3.3-V I/O standard in the Stratix IV E device, perform the following steps:

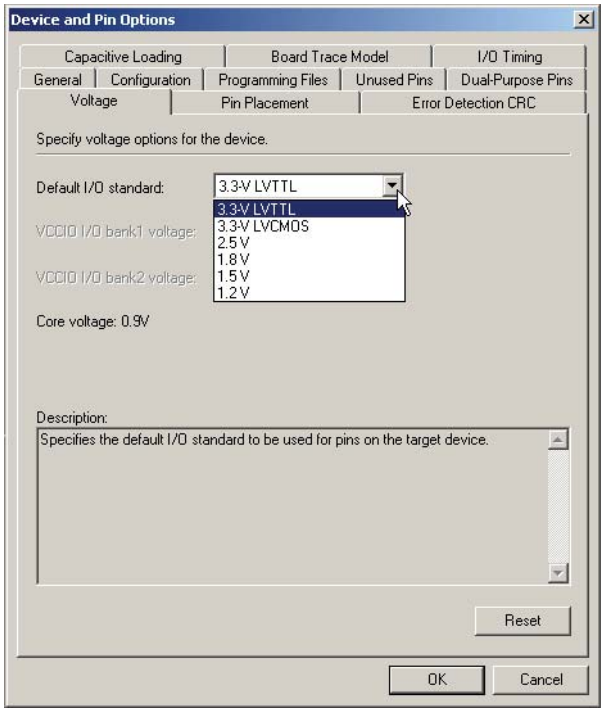
1. On the Assignments menu, click **Settings and Device and Pin Options** (Figure 8).

Figure 8. Settings Dialog Box in the Quartus II Software



2. In the **Device and Pin Options** dialog box, at the **Voltage** tab, select the **3.3-V LVTTL** or **3.3-V LVCMOS** I/O standard as the default I/O standard (Figure 9).

Figure 9. Voltage Tab Settings in the Device and Pin Options Dialog Box

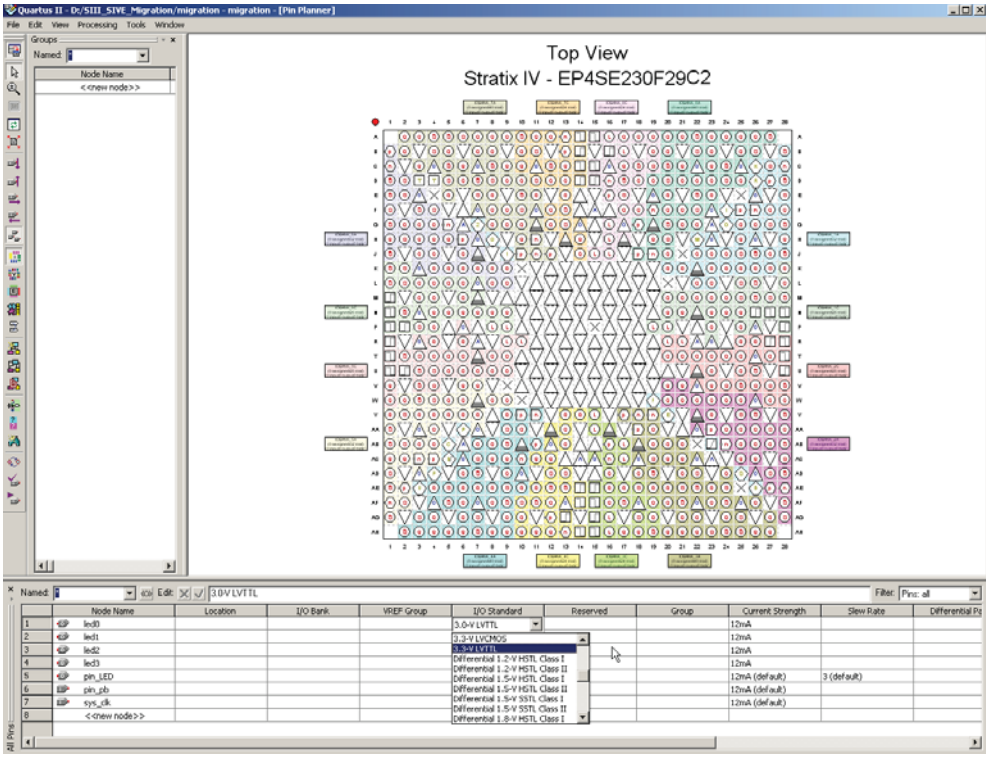


If you have previously assigned a 3.0-V LVTTL/LVCMOS I/O standard to individual pins in the Stratix III device, you must also individually assign a **3.3-V LVTTL/LVCMOS** I/O standard on the affected I/O pins in the Stratix IV E device.

To edit the I/O standard assignments using the Pin Planner in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **Pin Planner.**
2. Double-click the cell in the **I/O Standard** column that corresponds to the pin that you want to edit. Use the drop-down arrow to select the **3.3-V LVTTL/LVCMOS** I/O standard option (Figure 10).

Figure 10. I/O Standard Assignments in the Pin Planner View



For more information about creating or editing pin-related assignments in the Pin Planner, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Stratix III devices support the 3.3-V LVTTL or 3.3-V LVCMOS I/O standard using V_{CCIO} at 3.0 V. The 3.3-V LVTTL/LVCMOS output assignment in Stratix IV E devices results in a V_{CCIO} of 3.0 V for the bank that the output is located in. For Stratix III devices, the 3.3-V LVTTL/LVCMOS output assignment produces a V_{CCIO} of 3.3 V for the bank that the output is located in.

For more information about I/O standard specifications, refer to the *DC and Switching Characteristics* chapter in volume 4 of the *Stratix IV Device Handbook*.

Stratix III-to-Stratix IV E Cross-Family Migration Checklist

The following is a summary of the guidelines described in this application note. Use this checklist to help you follow these guidelines when you are designing your board for Stratix III-to-Stratix IV E cross-family migration.

	Done	N/A	Stratix III-to-Stratix IV E Cross-Family Migration Checklist (Part 1 of 2)
1	☐	☐	Review the Stratix III and Stratix IV E power pin connection guidelines to verify that all power planes are correctly connected and to determine the power supply requirements and voltage inputs that can share power rails for each device family.
2	☐	☐	The V_{CC} and V_{CCL} power supplies in Stratix III devices are combined into a single V_{CC} power supply in Stratix IV E devices.
3	☐	☐	The V_{CCPT} power supply of 2.5 V in Stratix III devices is split into two separate power supplies of 1.5 V and 2.5 V for V_{CCPT} and V_{CCAUX} in Stratix IV E devices, respectively.
4	☐	☐	Ensure the V_{CC} and V_{CCL} power supplies are connected together for Stratix III devices on the board if you designed a single PCB for both Stratix III and Stratix IV E devices.
5	☐	☐	All 1.1-V power supply voltages in Stratix III devices become 0.9-V power supply voltages in Stratix IV E devices.
6	☐	☐	All 3.3-V power supply voltages in Stratix III devices become 3.0-V power supply voltages in Stratix IV E devices.
7	☐	☐	If necessary, re-design the voltage regulators and passive components on the board to handle the different supply voltage and current requirements.
8	☐	☐	Create a keep-out area for the overhang of the hybrid BGA packages of the Stratix IV E device, especially if the Stratix III device is in the fineline BGA package.
9	☐	☐	Use the JTAG, PS, or FPP configuration schemes to allow vertical migration from the Stratix III device to a EP4SE820 device. Due to the unavailability of serial configuration devices that can support the large configuration file size, the EP4SE820 device is not currently supported by the FAS configuration scheme.
10	☐	☐	Be aware of the fewer user-available I/O pins in the migration of the 1760-pin EP3SL340 to the EP4SE530 device of the same package.
11	☐	☐	To ensure successful migration, Altera recommends designing the external memory interfaces using the DQ and DQS pins with the DQ and DQS pins capability of the Stratix IV E device (that have fewer I/O pins). If you plan cross-family migration from a Stratix III to a Stratix IV E device that has fewer user I/O pins, do not use the unavailable I/O pins in Stratix IV E device for external memory interface designs.
12	☐	☐	For information about the number of DQ and DQS groups that are available in the Stratix III and Stratix IV E devices, refer to the *External Memory Interfaces* chapter in the *Stratix III Device Handbook* and *Stratix IV Device Handbook*, respectively.
13	☐	☐	For information about the availability of I/O banks, user I/O pins, and DQ and DQS pins in Stratix III and Stratix IV E devices, refer to the *Stratix III Device Pin-Outs* and *Stratix IV Device Pin-Outs*.
14	☐	☐	Use the Quartus II software to compile and verify the designs for each device before finalizing your pin assignments.
15	☐	☐	Stratix IV E devices do not support the 3.0-V LVTTL/LVCMOS I/O standard that is supported in Stratix III devices. You must change this I/O standard in the Stratix III device to **3.3-V LVTTL/LVCMOS** I/O standard in the Stratix IV E device to account for the differences in the Stratix IV E device. You must also individually change the I/O standard to the **3.3-V LVTTL/LVCMOS** I/O standard on all I/O pins in the Stratix IV E device that you individually assigned as 3.0-V LVTTL/LVCMOS I/O standard in the Stratix III device.

	Done	N/A	Stratix III-to-Stratix IV E Cross-Family Migration Checklist (Part 2 of 2)
16	☐	☐	If you use 3.0-V V_{CCIO}, Stratix IV E devices provide full support for 3.3-V LVTTL/LVCMOS I/O standards on their input and output levels.
17	☐	☐	You cannot assemble existing Stratix III device PCBs that are not designed to these guidelines with Stratix IV E devices.

Conclusion

This application note provides guidelines and an easy-to-follow checklist on designing a single PCB that accommodates both Stratix III and Stratix IV E devices. By using these guidelines, cross-family migration between the Stratix III and Stratix IV E device family is not only possible, but you can also design your Stratix III FPGA to take advantage of the higher performance, higher density, and lower power benefits of the Stratix IV E FPGAs.

Document Revision History

Table 8 lists the revision history for this application note.

Table 8. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
September 2009, version 2.0	■ Updated Table 1 and Table 7. ■ Minor text changes.	—
March 2009, version 1.0	Initial Release.	—

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