# NAND Flash Memory Interface with Altera MAX Series

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You can use an Altera® MAX® II, MAX V, or MAX 10 device to implement a NAND Flash Memory Interface. You can use the design with both Samsung and AMD NAND Flash memories.

**Related Information**

- **Design Example for MAX II**
  Provides the MAX II design files for this application note (AN 500)
- **Design Example for MAX 10**
  Provides the MAX 10 design files for this application note (AN 500)
- **MAX II Device Design Guidelines**
  Provides information about MAX II devices design guidelines
- **Power Management in Portable Systems Using Altera Devices**
  Provides information about power management in portable systems using Altera devices

## NAND Flash Interface Using Altera Devices

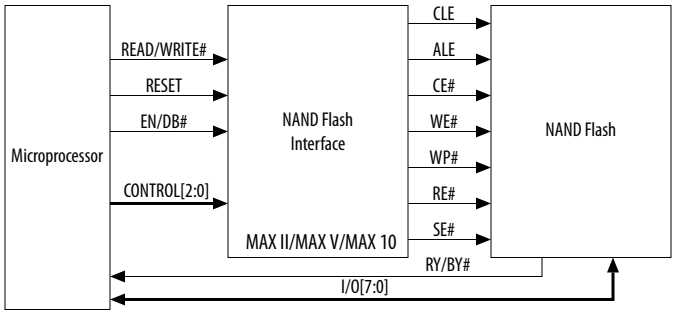
The commands from the system arrive at the inputs of the NAND Flash interface in coded form. Each operation performed is coded in a different format and issues through the 3-bit wide control bus.

Enabling or disabling (in the case of `ALE`, `CLE`, `SE`, and `WE`) is done separately with the help of enable/disable signal inputs. These commands are decoded correctly by the NAND Flash interface block (of the supported Altera devices) and translated as output enabling or disabling signals, which ensures the desired operation of the NAND Flash.

The actual operation performed by a NAND Flash is governed by the commands written into its command register through the I/O bus. The address of the data that is read or written, together with the data, are issued through the same bus.

**Figure 1: Interfacing Signals of the NAND Flash Device**

This figure shows host interfacing signals and NAND Flash device interfacing signals. The signals followed by a # are asserted when low.




## Signals

**Table 1: Interfacing Signals**

This table lists the interfacing signals.

| Signal | Size | Description |
|---|---|---|
| READ/WRITE# | 1-bit | Input from the microprocessor to distinguish between a write and a read operation.<br>• READ/WRITE# 0: Write operation.<br>• READ/WRITE# 1: Read operation |
| RESET | 1-bit | Input from the microprocessor to reset the NAND Flash device. |
| CONTROL[2:0] | 3-bit | 3-bit control bus. The microprocessor sends 3 bits of information to the NAND Flash interface (supported Altera devices) where it is suitably decoded. The appropriate interfacing signals are enabled or disabled depending on the condition of the EN/DB# input. |
| EN/DB# | 1-bit | Control bit used in conjunction with the control bits to perform the required operation.<br>• EN/DB# 1: Enables the interfacing signal selected by the control bits<br>• EN/DB# 0: Disables the interfacing signal selected by the control bits. |
| I/O[7:0] | 8-bit | Bidirectional 8-bit multiplexed bus used to send data/command/address to their respective registers in the NAND Flash device. The data read from the NAND Flash device is also available on these lines. |
| RY/BY# | 1-bit | Output from the NAND Flash device, indicating the status of the device.<br>• RY/BY# 0 : Device is still busy performing an operation.<br>• RY/BY# 1 : Device is ready to accept the next command. |

| Signal | Size | Description |
|---|---|---|
| CLE | 1-bit | Active high Command Latch Enable. Use to select the Command Register or the Data Register of the device. When high, the command on the I/O lines is latched into the command register on the rising edge of WE#.<br>**Note:** Data Register is selected by making the CLE and ALE signals low. The data on the I/O lines is latched into the Data Register on the rising edge of WE#. |
| ALE | 1-bit | Active high Address Latch Enable. Use to select the Address Register or the Data Register of the device. When high, the address on the I/O lines is latched into the address register on the rising edge of WE#. A low signal will cause the device to reset. This signal must remain high for the entire address sequence.<br>**Note:** Data Register is selected by making the CLE and ALE signals low. The data on the I/O lines is latched into the Data Register on the rising edge of WE#. |
| CE# | 1-bit | Active low Chip Enable. Use to choose between the active mode and the standby mode of the device.<br>• CE# 0 : Active mode selected.<br>• CE# 1 : Standby mode is selected if no operation is currently in progress.<br>The CE signal is ignored if a program or erase operation is in progress. |
| WE# | 1-bit | Active low Write Enable. Use to write command/address/data into their respective registers in the device. The information on the I/O lines is latched into the respective registers on the rising edge of WE#. |
| WP# | 1-bit | Active low Write Protect.<br>• WP# 0 : Device is write protected.<br>• WP# 1 : Device is not write protected. |
| RE# | 1-bit | Active low Read Enable. Use to read data/status to/from the device. The information is available on the I/O lines on the rising edge of RE#. |
| SE# | 1-bit | Active low Spare area Enable. Required only when an AMD device is used. Not required for a Samsung device.<br>• SE# 0 : 16 bytes of Spare area on each page is enabled.<br>• SE# 1 : Spare area is disabled. |

## Operations

Each operation performed is coded in a different format and issues through the 3-bit wide control bus.

**Table 2: Operations Performed by the Interface on Different Combinations of the Control Signals**

| Control Signal [2:0] | EN/DB# | Operation performed |
|---|---|---|
| 000 | — | Command Latch Enabled (CLE = 1) irrespective of the condition on EN/DB#. |
| 001 | — | Read Data / status / device depend on the command sent on the I/O lines. |
| 010 | — | Write Data / command /address depending on the command sent on the I/O lines. |
| 011 | 1 | ALE is asserted (high). |
| | 0 | ALE is disabled (low). |
| 100 | 1 | SE# is asserted (low). |
| | 0 | SE# is disabled (high). |
| | | **Note:** This operation is only applicable for AMD flash devices. This command enables/disables the 16 bytes of spare area on each page depending on the condition of the EN/DB# line. |
| 101 | 1 | WP# is asserted (low). |
| | 0 | WP# is disabled (high). |
| 110 | 1 | CE# is asserted (low). |
| | 0 | CE# is disabled (high). |
| 111 | 1 | The status of the flash device is sent on the RY/BY# line. |
| | 0 | RY/BY# line does not reflect the status of the flash device. |

## AMD and Samsung NAND Flash Devices Commands

**Table 3: AMD NAND Flash Device (Am30LV0064D) Commands**

This table lists the various commands supported by the AMD NAND Flash device (Am30LV0064D).

| Operation | Cycle 1 | Cycle 2 | Valid During Busy | Comment |
|---|---|---|---|---|
| Read data | 00h/01h | — | No | — |
| Gapless Read | 02h | — | No | Reads out data in a special high-performance mode to allow reading from multiple pages with only a 7 µs latency on the first page transfer.<br>Superset Command supported by the AMD NAND Flash device only. |
| Read Spare Area | 50h | — | No | — |
| Read ID | 90h | — | No | — |

| Operation | Cycle 1 | Cycle 2 | Valid During Busy | Comment |
|---|---|---|---|---|
| Read Status | 70h | — | Yes | — |
| Input Data | 80h | — | No | Programming data into the flash array is a two step process and requires two separate command sequences to be performed. The data to be programmed must be loaded into the data registers using the Input data command sequence. After the data is loaded the Page Program command is performed to transfer the information from the data registers to the flash array. |
| Page Program | 10h | — | No | Programming data into the flash array is a two step process and requires two separate command sequences to be performed. The data to be programmed must be loaded into the data registers using the Input data command sequence. After the data is loaded the Page Program command is performed to transfer the information from the data registers to the flash array. |
| Block Erase | 60h | D0h | No | A two command procedure. In the first command cycle the address of the block to be erased is issued to the device. In the second command cycle the flash device begins the erase operation when it encounters a rising edge on the WE# signal. |
| Erase Suspend | B0h | — | Yes | Allows time critical tasks to be performed. These tasks can only be performed on the block that is not being currently erased.<br>Superset Command supported by the AMD NAND Flash device only. |
| Erase Resume | D0h | — | No | Allows time critical tasks to be performed. These tasks can only be performed on the block that is not being currently erased.<br>Superset Command supported by the AMD NAND Flash device only. |
| Reset | FFh | — | Yes | — |

Programming of the Flash device occurs on a Page basis (512 bytes + 16 bytes of spare area), whereas the erasure takes place on a Block basis (8 K byte + 256 bytes).

### Table 4: Samsung NAND Flash Device (K9F4008W0A) Commands

This table lists the various commands supported by the Samsung NAND Flash device (K9F4008W0A).

| Operation | Cycle 1 | Cycle 2 | Valid During Busy | Comment |
|---|---|---|---|---|
| Read Data | 00h | — | No | — |
| Read ID | 90h | — | No | — |
| Read Status | 70h | — | Yes | — |
| Frame Program | 80h | 10h | No | Frame Program is a two command procedure: Loading of the data that has to be programmed starts with the Frame Program setup command (80h). The Frame Program confirm command (10h) initiates the programming process. |
| Block Erase | 60h | D0h | No | Block erase is also a two command procedure: The address of the block to be erased is loaded with the Erase setup command (60h). The Flash device initiates the internal erasing process when the Erase confirm command (D0h) is loaded. |
| Reset | FFh | — | Yes | — |

Programming of the flash device takes place on a Frame basis (32 bytes), whereas the erasure takes place on a block basis (4 K byte). The device also supports partial frame programming.

**Related Information**

- **Spansion NAND Flash Memory Page**
  Provides information about Spansion NAND flash memory
- **Samsung NAND Flash Device Information**
  Provides information about Samsung NAND flash device

# Implementation

These designs may be implemented using MAX II, MAX V, and MAX 10 devices. The provided design source codes target the MAX II (EPM240) and MAX 10 (10M08) respectively. These design source codes are compiled and can be programmed directly to the MAX devices.

**Table 5: Supported Flash Devices for the NAND Flash Interface Design**

This table lists the supported flash devices for the NAND Flash interface design.

| Name | Description |
|---|---|
| AMD NAND Flash device (Am30LV0064D) | • A 64-Mbit mass storage device suited for high density applications in which data is sequential and requires fast write capability.<br>• The initial page read access time is 7 µs with subsequent byte accesses of less than 50 ns. |

| Name | Description |
|---|---|
| Samsung NAND Flash device (K9F4008W0A) | • A 512 K × 8-bit storage device suited for applications that do not require the high performance levels or the capacity of larger density flash memories.<br>• Supports 32-byte Frame read operations with a random access time of 15 µs and a sequential access time of 120 ns. |

## Source Code

The design examples are implemented in Verilog HDL.

# Acknowledgments

Design example adapted for Altera MAX 10 FPGAs by:

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# Document Revision History

**Table 6: Document Revision History**

| Date | Version | Changes |
|---|---|---|
| September 2014 | 2014.09.22 | Added MAX 10 devices information. |
| December 2007 | V1.0 | Initial release |