Introduction

PCI Express technology is a serial interconnect link to support multiple market segments and emerging applications. PCI Express specifies a data rate of 2.5 gigabits per second (Gbps) for the serial link (based on the PCIe Base specification version 1.1). This protocol allows a point-to-point, scalable, and extensible I/O interconnect. The PCI Express physical interface is differential low voltage signaling with embedded clocking. Current PCIe specifications support scalable widths of ×1, ×2, ×4, ×8, ×16, and ×32. The Stratix® GX device family supports up to a maximum of 20 transceivers.

Stratix GX Settings for the PCI Express Protocol

Stratix GX transceiver options are set through the Altera® MegaWizard® Plug-In Manager. This application note goes through the altgxb megafunction settings that support PCI Express. The configuration settings that are system specific to PCI Express are also covered.

For more information on configuration settings, see the Stratix GX Transceiver User Guide.

The first two pages of the MegaWizard Plug-In Manager are for megafunction selection and will not be covered in this application note. The altgxb megafunction is the assumed selection.

Figure 1 shows the page 3 of the altgxb megafunction configuration.
The Basic protocol is used for PCI Express as it provides 8B/10B encoding across the required data rates in a single channel configuration.

The 8B/10B encoder/decoder in the hard intellectual property (IP) has an issue with performing polarity inversion or forced disparity mechanisms. If polarity inversion or forced disparity mechanisms are mandatory for a PCI Express design, Altera recommends bypassing the 8B/10B encoder/decoder in the Basic protocol and implementing the 8B/10B encoder/decoder in the FPGA core. In this case, the channel data width becomes 20 bits wide.

A typical PCI Express design utilizes a single duplex channel with a 20-bit data width. You can change the number of channels and data width to suit design needs. With a 20-bit data width interface, there are some clocking restrictions (refer to the Basic Mode chapter of Stratix GX User Guide) for the Stratix GX receiver side specifically with respect to receive phase compensation FIFO. As long as you can clock the FPGA fabric at 250 MHz (parallel clock frequency), you can also select a 10-bit transceiver data width.
The **Train Receiver PLL CRU clock from Transmitter PLL** option must be de-selected if the 125-MHz reference clock for Stratix GX devices is generated from a cascaded external PLL in the Stratix GX fabric. Using a 100-MHz PCI Express specified clock source and de-selecting avoids three cascaded PLLs (EPLL, TX PLL in GX, RX PLL in GX). If you provide a 125-MHz reference clock from a clock crystal that is compliant with PCI Express base version 1.0 and CEM version 1.1 jitter specifications, you have the choice of keeping the **Train Receiver PLL CRU clock from Transmitter PLL** option enabled or disabled. Figure 1 shows an example of a 125-MHz reference clock that is supplied from a clock crystal with low jitter where the **Train Receiver PLL CRU clock from Transmitter** option is enabled.

The **Select the bandwidth type on the transmitter PLL** option is a system specific setting. The default value for this option is **HIGH**. The PCI Express specification version 1.1 states that the transmitter PLL bandwidth should be between 1.5 MHz to 22 MHz, and the transmitter PLL can be set to **LOW** or **HIGH**. Regardless of whether a **LOW** or **HIGH** setting is selected, the total bandwidth of the transmitter PLL is approximately 3 MHz to 11 MHz in Stratix GX devices and does not cover the PCI Express specified bandwidth. If a **HIGH** setting is selected, the transmitter PLL tracks more jitter from the clock and rejects the noise of the power supplies, power distribution, and voltage controlled oscillator (VCO). For the Stratix GX development board, a **HIGH** setting yielded better jitter numbers. Altera recommends that you test with a **LOW** and **HIGH** setting and use which ever yields the best results (minimum jitter).

The **Select the acceptable PPM threshold between the Receiver PLL VCO and CRU clock** option has multiple choices to select, ranging from 125 PPM to 1000 PPM. The recommended setting is 1000 PPM. The PCI specification is ±300 PPM so that the worst case of 600 PPM difference can be handled by the 1000 PPM setting.

You can select all the reset signals that are part of the optional input ports depending on design considerations. In most cases, these signals are used by the external reset sequence state machine. The reset sequence is to keep the pointers in the phase compensation FIFO from moving when the PLLs are not yet locked.

For more information Stratix GX reset sequences, refer to the *Reset Control & Power Down* chapter of *Stratix GX Transceiver User Guide*.

All Stratix GX signals which are optional on page 3 of the MegaWizard Plug-In Manager are self explanatory. The lock time for the transmitter PLL signified by `pll_locked` going high can be found in the *Stratix GX Device Family* data sheet.
Loopback and self test are not mandatory to implement the PCI Express protocol. Although there are loopbacks that are identified in the PIPE interface of the PCI Express specification, the loopbacks and self test features shown in Figure 2 are left to your discretion. Constraints using the pseudo random binary sequence (PRBS) pattern exist when the 8B/10B encoder/decoder is enabled.

For more information on loopbacks and self test, see the Loopback Modes and Stratix GX Built-In Self Test (BIST) chapters of the Stratix GX Handbook.

Figure 3 shows the settings for the 8B/10B decoder and word aligner settings.
The 8B/10B decoder for the receiver is not selected. The word aligner is set to align to the K28.5 comma character and recognizes positive and negative disparity commas automatically as long as the \textit{rx\_enacdet} port is used and is set to high (1'b1 on \textit{rx\_enacdet}). If the \textit{rx\_enacdet} port is not used, the word aligner will not align to the comma. In basic mode with the 8B/10B encoder/decoder disabled, the \textit{rx\_enacdet} signal acts as an edge-sensitive signal. If \textit{rx\_enacdet} is high, it word aligns once. A second word align requires that you de-assert the signal first and then assert it to execute a second word align.

The run length setting is not used as the maximum run length when an 8B/10B coding scheme is set to 5.

Figure 4 shows page 6 of the \texttt{altgxbl} MegaWizard. The main setting on this page is the data rate.
Do not turn on the **Enable Stratix GX to Stratix GX DC coupling** option because it is not applicable for PCI Express.

You can use this option if and only if the Stratix GX device is DC coupled with another Stratix GX device.

Forced signal detection (**rx_force_signal_detect**) is enabled which effectively bypasses the signal detect circuit for support of lower $V_{ID}$. The signal detect circuit output is always forced high irrespective of the level of $V_{ID}$. The Quartus® II software version 4.2 automatically enables this option. An error occurs if it is not enabled while performing full compilation of the design. In BASIC functional mode, there is no output signal (**rx_signaldetect**) coming out from the signal detect block.
Altera does not have any specific recommendation on using the **Use equalizer control signal** option. You can use this feature as an optional port to dynamically change the equalization setting of the receiver channel. If a specific equalization value is needed, you can turn off the **Use equalizer control signal** option and statically set the **Select the equalize control setting** (quad based) list in the MegaWizard Plug-In Manager.

Altera recommends testing a given system to pick the optimal value of equalizer that yields the desired/optimal bit error rate (BER).

The **Select the bandwidth type on the receiver** option is system specific. The Quartus II software defaults to LOW. Altera recommends checking the jitter numbers with each allowed setting and then choose an optimal setting. PCI Express specifies a clock data recovery (CDR) bandwidth up to 22 MHz. The bandwidth of the receiver PLL is approximately 6 to 30 MHz. The receiver bandwidth type used for the Stratix GX development board with high-speed lab equipment is low, since it yielded the optimal results. The base setting on the data rate is set at 2,500 megabits per second (Mbps) for the PCI Express protocol.

Figure 4 shows page 7 of the **altgxb** MegaWizard. On this page, the optional ports for the receiver are set.
The optional input ports as the name goes are optional for user to use depending on the design expectations.

You should enable the `rx_locktorefclk` and `rx_locktodata` signals only when you want to use manual mode to lock in the CDR. In manual mode, the `rx_locktodata` signal has higher priority over `rx_locktorefclk`. You can use the `rx_locktorefclk` control signal for the receiver PLL to lock to the reference clock mode. You can use the `rx_locktodata` signal for the receiver PLL to lock to the incoming serial data mode.

Altera recommends using the `rx_clkout` port because it carries the recovered clock from the receiver channel to the FPGA core (read clock of the receiver phase compensation FIFO). This clock is used to clock a phase compensation FIFO to decouple the FPGA clock domain from the recovered clock domain.
The \textit{rx\_locked} signal is optional and indicates when the receiver PLL is locked to the reference clock. This signal can toggle when the VCO is locked to the incoming data, and is an active low signal.

Altera recommends using the \textit{rx\_freqlocked} port because this port indicates when the receiver is in lock to data mode.

See the \textit{Stratix GX Transceiver User Guide} for additional information.

The \textit{rx\_syncstatus} and \textit{rx\_patterndetect} ports are outputs of the word aligner and indicate when the word aligner has aligned to the word alignment pattern and when the pattern is detected in the current word boundary. Altera recommends the use of these ports for PCI Express operations as you can use the indicators to transition between states in a start up state machine, and to detect if the start of frame occurs in the expected time frame.

For more information on the operation of these ports, see the \textit{Stratix GX Transceiver User Guide}.

\textit{Figure 6} shows page 8 of the \texttt{altgxb} MegaWizard. This page sets the transmitter functionality.
The **Select the transmitter termination resistance** option has multiple choices (100 Ω, 120 Ω, or 150 Ω). For the PCI Express protocol, Altera recommends selecting 100 Ω.

Using dynamic VOD controls is not necessary for the PCI Express configuration, but you can use an optional port to dynamically alter the transmitter output characteristics. You should set the **Voltage output differential (VOD) control setting** option to 800 mV.

For more information on available settings, see the *Stratix GX Analog Description* chapter of the *Stratix GX User Guide*. 
If a specific $V_{OD}$ and/or pre-emphasis value is needed, turn off the **Use Voltage Output Differential (VOD) control signal** option and/or the **Use preemphasis control signal** option and statically set the Select the **Voltage Output Differential (VOD)** (block based) list in the MegaWizard Plug-In Manager. Based on the experiments conducted on the setup using PLD Applications XpressBridge board and the Intel Compliance Base board (total trace length of 4 inches), a pre-emphasis setting of two yielded optimal results. To get details of the system setup and board design (e.g., stack up, number of layers), contact PLD Applications at [www.plda.com](http://www.plda.com).

Figure 7 shows page 9 of the altgxb MegaWizard. This page allows you to select which output files you require. You cannot turn off the Variation file because it is required.

**Figure 7. Page 9 of the altgxb MegaWizard Plug-In Manager**
Stratix GX Issues with the PCI Express Protocol

Stratix GX devices (altgxb) are not compatible and are non-compliant with the following features. The features mentioned are classified into Physical and Physical Coding Sub-Layer (PCS).

**Physical Layer**

The physical layer features are as follows:

- **Spread-Spectrum Clocking with 0 to -0.5% Down Spread at 30- to 33-KHz Modulation**: Jitter increases
- **Power Budgeting and Power Down Modes**: Not implemented in the altgxb block
- **Electrical Idle State**: altgxb is not designed to perform this function
- **Receiver Wakeup Mechanism using Beacon**: No mechanism exists in the receive of altgxb
- **Receiver Detect Mechanism**: No mechanism exists to perform the receiver detect function
- **De-emphasis is not Complaint with PCIe Specification (High Voltage or High Temperature Corner Cases)**: Does not meet the specified 30 to 37%
- **Signal Detect Circuitry is not Complaint with the 175-mV Requirement**: The signal detect circuitry is not functioning properly so the circuit output is forced to always HIGH

**PCS**

The PCS features are as follows:

- **8B/10B Encoder/Decoder has no Polarity Inversion**: Current hard IP does not have this feature implemented. Need to implement the 8B/10B encoder/decoder block in the FPGA core
- **No Physical Status Signals like Receiver Electrical Idle, Transmitter Compliance, Transmitter Electrical Idle (No PIPE interface)**: There is no PIPE interface in the altgxb megafuction
- **No PCIe Specific Power Down Modes Implemented in Stratix GX PCS**

**Experiments**

This section illustrates the observations made on the XpressBridge board designed by PLD Applications. Contact PLD Applications at [www.plda.com](http://www.plda.com) for more information about the board (e.g., setup, equipment, observations, and eye diagrams under nominal conditions).

The eye diagrams shown in Figures 12 through 15 are captured by the PCI-SIG software that has the eye mask defined by PCI Express specification from the XpressBridge board with an approximate trace length of 4 inches. Also, the PLDA XpressBridge board and Intel Base Compliance board are shown in Figures 8 and 9.
**Figure 8. PLDA XpressBridge Board using Stratix GX Devices**

PCIe High-Speed Interface (4X) at 2.5 Gbps

PCI-X Interface
Figures 10 and 11 show the Intel Compliance Base board with the PLDA XpressBridge board using a PCI Express connector.
Figure 10. Intel Compliance & PLDA XpressBridge Board Using a PCI Express Connector (View 1)
Figures 12 through 15 show eye diagram results with a pre-emphasis setting of 0, 1, 2, and 3.
Figure 12. $V_{OD}$ setting = 800 mV, Pre-Emphasis setting = 0, Eye Result = PASS

Figure 13. $V_{OD}$ Setting = 800 mV, Pre-Emphasis Setting = 1, Eye Result= PASS

Figure 14. $V_{OD}$ Setting = 800 mV, Pre-Emphasis Setting = 2, Eye result= PASS
Figure 15. $V_{DD}$ Setting = 800 mV, Pre-Emphasis Setting = 3, Eye Result = PASS

Figure 16 shows the configuration space test summary report.
Conclusion

Stratix GX devices support most of the features of the PCI Express specification. The major parts that it is not complaint with are jitter numbers with SSC, de-emphasis specification (based on PCI Express Characterization report), and signal detect threshold.
Using Stratix GX Transceivers for PCI Express