Converting Memory from Asynchronous to Synchronous for Stratix & Stratix GX Designs

November 2002, ver. 2.0 Application Note 210

Introduction

The Stratix™ and Stratix GX device families provide a unique memory architecture called TriMatrix™ memory, consisting of dedicated memory blocks of three sizes. These blocks provide flexible and effective solutions for various memory applications. Table 1 lists the TriMatrix memory block types and their total memory bits.

Table 1. Stratix & Stratix GX TriMatrix Memory Blocks

Block Type	Total Memory Bits
M512 block	512 bits w/ parity (576)
M4K block	4 Kbits w/ parity (4,608)
M-RAM block	512 Kbits w/ parity (589,824)

For a detailed explanation of the TriMatrix memory architecture, refer to *AN 203: Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices*, the *Stratix Programmable Logic Device Family Data Sheet*, and the *Stratix GX FPGA Family Data Sheet*.

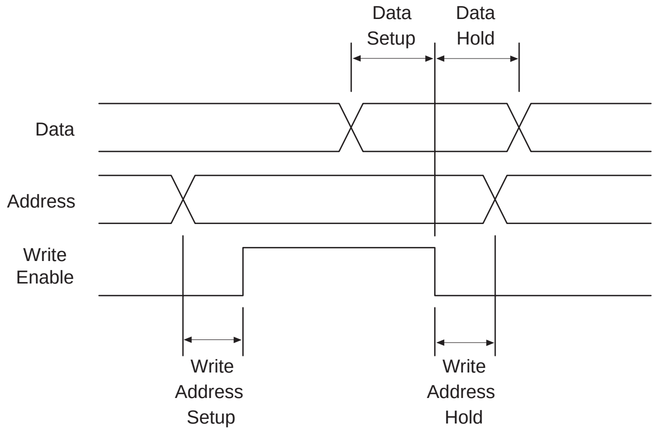
TriMatrix memory operates as fully synchronous true or simple dual-port memory capable of running at speeds of up to 312 MHz. The memory can operate in flow-through mode (inputs registered, outputs unregistered) or pipelined mode (inputs and outputs registered). The TriMatrix memory architecture does not support asynchronous memory. Therefore, you should convert asynchronous memory designs to synchronous before implementing them in Stratix and Stratix GX devices. This document illustrates the advantages of synchronous memory operation, including improved performance, and explains how to convert asynchronous memory designs to synchronous.

Synchronous vs. Asynchronous Memory

Several important differences exist between asynchronous and synchronous memory. Asynchronous memory requires that you create a write enable control circuit to generate a pulse every time a write operation occurs. You must consider write address setup and hold time and data setup and hold time on the rising and falling edge of the write enable pulse. The write enable must toggle on every write operation, as the address cannot change while the write enable is active. Figure 1 illustrates how asynchronous memory behaves.

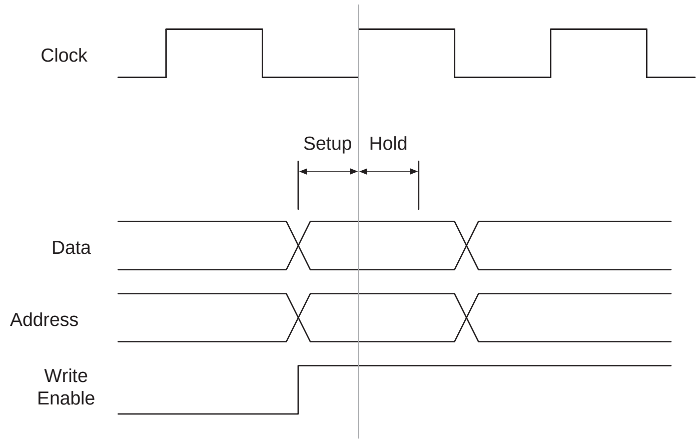
AN-210-2.0

Figure 1. Asynchronous Memory Behavior



Synchronous memory design offers several advantages over asynchronous memory design. Simpler timing requirements allow synchronous memory to operate at much higher frequencies, resulting in higher memory bandwidth. Synchronous operation is not prone to errors because signals are registered on clock edges, simplifying the design process. A write-enable control circuit is not required because the memory block controls the write strobe generation, saving on resource usage and simplifying the design. Additionally, synchronous memory consumes little standby power. Figure 2 illustrates synchronous memory behavior.

Figure 2. Synchronous Memory Behavior



In many designs, even if the memory is asynchronous, the modules the memory interfaces with are synchronous, making the conversion to synchronous memory design straightforward. Registers in the data path would move into the memory block, having a negligible effect on functionality.

Synchronous Memory Design

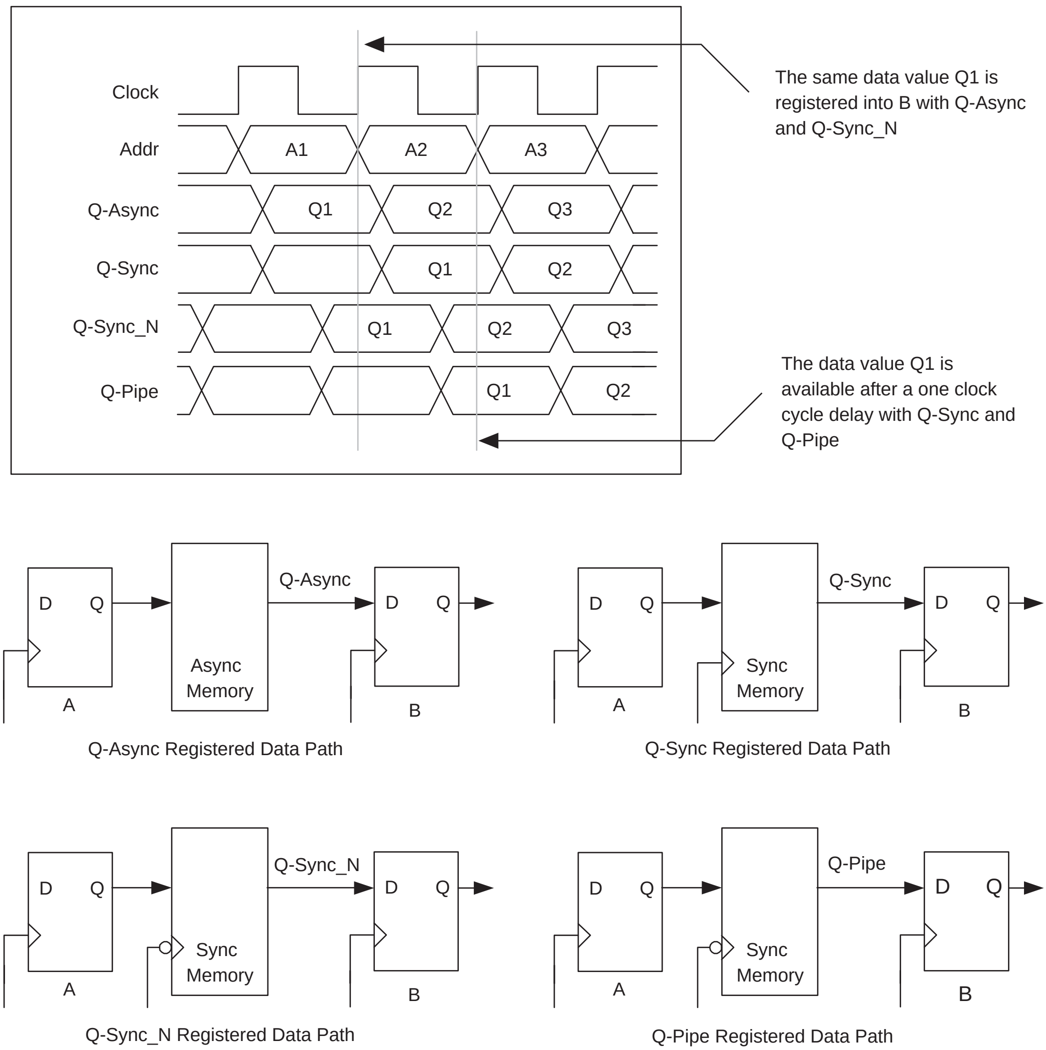
In synchronous memory operation, the TriMatrix™ memory architecture receives a system clock to control read and write operations. The TriMatrix memory block uses one or more system clocks to generate a self-timed intra-block write pulse strobe. This strobe writes to the memory without toggling the write enable (`WE`) signal. Since the intra-block pulse toggles, the address lines can change while the `WE` signal is active, allowing multiple writes to different addresses. The memory block can have a zero hold time, symplifying system design.

Synchronous memory can achieve the same or better performance as asynchronous memory if the data path is pipelined and the design is modified to compensate for the additional pipelined stages.

You can emulate the behavior of asynchronous memory by choosing an appropriate clock frequency such that the output of the Stratix or Stratix GX memory block behaves similarly to the output of the asynchronous memory. Figure 3 illustrates the Q output behavior of the memory block when it is asynchronous (Q-Async), clocked on the positive edge (Q-Sync), and clocked on the negative edge (Q-Sync_N).

If the asynchronous memory is in a registered data path as shown in Figure 3, you can make the memory synchronous by using the negative edge of the clock. The output data that is registered into B will have the same data Q1 whether it is asynchronous (Q-Async) or synchronous (Q-Sync_N).

Figure 3. Registered Data Path *Note (1)*



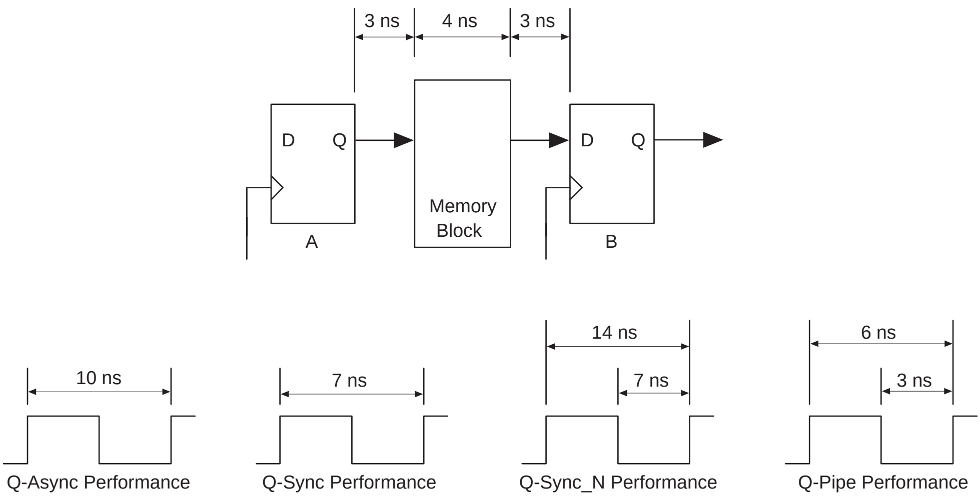
Note to Figure 3:

(1) Although Q-Async is not possible in the Stratix or Stratix GX memory block, Figure 3 illustrates this for comparison purposes.

A designer can use Q-Sync or Q-Pipe to capture the correct data Q1 after a one clock cycle delay. Using Q-Sync or Q-Pipe increases performance because the system clock is able to operate at a higher frequency compared with the Q-Sync_N implementation. For example, if the registered data path in Figure 4 is set with the parameters specified below, the maximum performance of the data path is 10 ns for Q-Async.

- Delay from A to the memory block = 3 ns
- Delay through the memory block = 4 ns
- Delay from the memory block to B = 3 ns

Figure 4. Registered Data Path Performance



If the asynchronous memory is replaced with a synchronous TriMatrix memory block with the same type of system clock, the maximum performance is 7 ns because of the addition of the input registers (Q-Sync). If negative-edge clocking is used, system performance decreases as delay from the negative edge of the clock (memory block) to the positive edge of the clock (register B) is 7 ns, effectively half a period. This results in overall performance of 14 ns (Q-Sync_N). If the memory block is pipelined to include output registers, the system clock performance becomes 6 ns, because the critical path is from the negative edge of the output register of the memory to the positive edge of register B.

Converting Existing Designs

When migrating designs to Stratix or Stratix GX devices, you must re-target the existing asynchronous memory components to the TriMatrix memory architecture. Conversion requires careful analysis and understanding of the memory operation, and some redesign.

Use the following procedure when converting existing asynchronous memory blocks:

- Recreate the memory function using the MegaWizard® Plug-In Manager in the Quartus II software (version 2.0 and later) to target the Stratix or Stratix GX device (Tools menu)
- Implement negative edge clocking for asynchronous memory components
- Remove the `WE` signal control circuit
- Verify registered data path behavior

For information regarding the different TriMatrix memory modes and using the MegaWizard Plug-In Manager to generate memory components, refer to *AN 203: Using TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices*.

You must connect the clock port of the new synchronous memory component to the clock that feeds the registered data path. Implement negative edge clocking by utilizing a `NOT` gate primitive to invert the clock feeding the memory component. You can remove the `WE` pulse generator circuit as it is not required for TriMatrix memory blocks.

Once you implement the design changes, verify the behavior of the data path. Using the Quartus II software or a third-party simulation tool, perform a timing simulation to verify the functionality of the memory block. Using the Quartus II or third party timing analyzer, check setup and hold times to ensure operation at the desired frequency. Many timing analyzers, including the Quartus II timing analyzer, automatically take positive or negative clocking of a register into account when computing the maximum frequency.

Verify the maximum frequency (f_{MAX}) of the clock feeding the registered data path. If there is a timing violation, or the desired performance is not achieved, further redesign is required. Adding pipelined stages and redesigning the system to accommodate the cycle latency associated with additional pipelining can increase performance.

Starting New Designs

When starting a new design that will utilize TriMatrix memory, consider the following:

- Specifications of the memory's performance and behavior
- Analysis of the data path

Determine the type of memory (single-port ROM, dual-port RAM, etc.) required for the application and the required performance of the memory block. Use the MegaWizard Plug-In Manager to create the appropriate memory function.

For more information on Stratix and Stratix GX memory megafunctions, see the Altera web site (**www.altera.com**).

Next, consider the performance required from the available memory block and system clocks. If the desired clock frequency is not available, use the PLLs in the Stratix or Stratix GX device to generate the required clock from one of the system clocks. Consider the number of pipelined stages required to achieve the desired performance. The rest of the design must compensate for the cycle latency.

The Stratix and Stratix GX device M-RAM blocks can replace external memory devices. Use the "Converting Existing Designs" section as a guideline for replacing asynchronous external memory. Since memory-access times will be much faster with on-chip memory, the TriMatrix memory blocks are able to emulate asynchronous memory in most cases.

Conclusion

Stratix and Stratix GX TriMatrix memory blocks must be synchronous. Their performance depends on the frequency of the clock source and the attributes of the data path. It is possible to migrate asynchronous memory designs to Stratix and Stratix GX devices without sacrificing performance or creating behavior changes in most cases. The benefits of synchronous memory designs, such as increased performance and simpler design process, make the TriMatrix memory block a flexible and effective solution for on-chip memory applications.

Revision History

The information contained in *AN 210: Converting Memory from Asynchronous to Synchronous for Stratix & Stratix GX Designs* version 2.0 supersedes information published in previous versions. The following change was made in *AN 210: Converting Memory from Asynchronous to Synchronous for Stratix & Stratix GX Designs* version 2.0: added Stratix GX devices throughout the document.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com