High-Speed Board Designs

November 2001, ver. 4.0 Application Note 75

Introduction

A successful high-speed printed circuit board (PCB) requires integration of the device(s), PCB(s), and other elements into the design. Altera® devices have fast I/O pins with fall times as low as 1 ns to 3 ns. Because a fast slew rate can contribute to noise generation, signal reflection, cross-talk, and ground bounce, designs must:

- Filter and evenly distribute power to all devices to reduce noise
- Use the recommended routing techniques for signals, including clock and differential signals
- Match impedance and evaluate termination schemes
- Terminate signal and transmission lines to diminish signal reflection
- Minimize cross-talk between parallel traces
- Reduce the effects of ground bounce

Power Filtering & Distribution

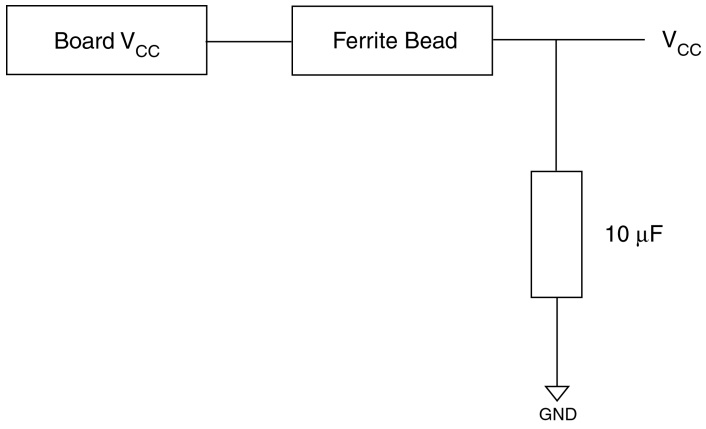
Clean, evenly distributed power to V_{CC} on all boards and devices can reduce system noise.

Filtering Noise

To diminish the low-frequency (< 1 kHz) noise caused by the power supply, filter the noise on the power lines at the point where the power connects to the PCB and to each device. Altera recommends placing a 100-µF electrolytic capacitor adjacent to the location where the power supply lines enter the PCB. If using a voltage regulator, place the capacitor immediately after the final stage that provides the V_{CC} signal to the device(s). Capacitors not only filter low-frequency noise from the power supply, but also supply extra current when many outputs switch simultaneously in a circuit.

Another way to filter power supply noise is to place a non-resonant surface-mount ferrite bead, big enough to handle the current, in series with power supply. Place a 10-µF to 100µF bypass capacitor next to the ferrite bead (see Figure 1). Proper terminations, layouts, and filtering in a design eliminate the need for the ferrite bead. In this case, use a 0 Ω resistor instead of the ferrite bead.

Figure 1. Filtering Noise with a Ferrite Bead



PCB elements add high-frequency noise to the power plane. To filter high-frequency noise at the device, Altera recommends placing decoupling capacitors as close as possible to each V_{CC} and ground pair.

Placing the power and ground planes in parallel and separated by dielectric material provides another level of bypass capacitance. These parallel planes reduce the power-related high-frequency noise, since this type of capacitance has no effective series resistance (ESR) and no lead inductance.

See the ***Operating Requirements for Altera Devices Data Sheet*** for more information on bypass capacitors.

Distributing Power

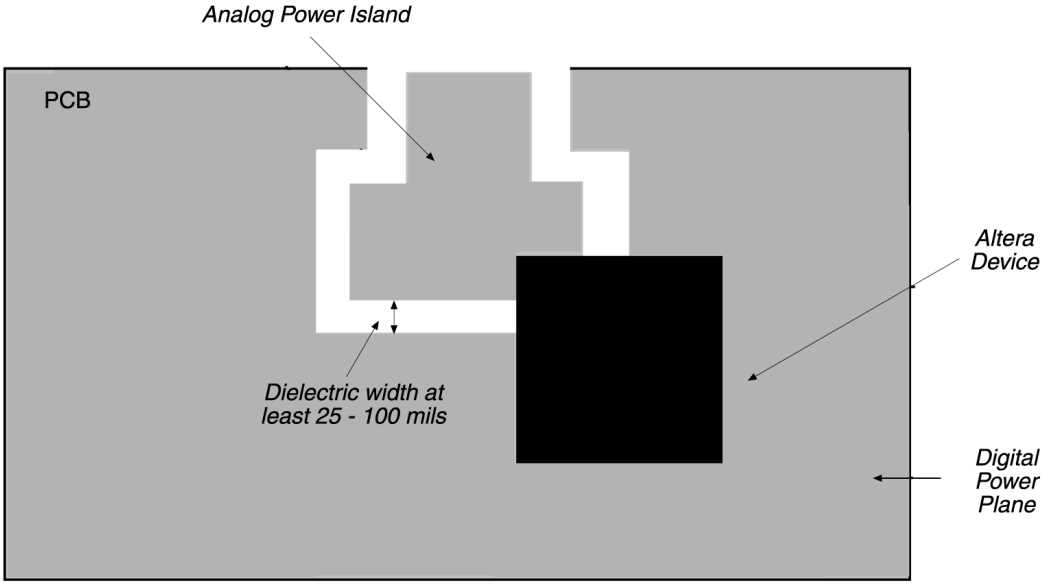
Power distribution also impacts system noise. Either a power bus network or power planes can distribute power throughout the PCB.

Usually used on two-layer PCBs, the least expensive way to distribute power is a power bus network, which consists of two or more wide metal traces that carry V_{CC} and ground to the devices. The density of the PCB limits the trace widths, which should be as wide as possible. Power buses have significant DC resistance; the last element on the bus may receive V_{CC} power degraded by as much as 0.5 V.

Altera recommends using power planes to distribute power. Used on multi-layer PCBs, power planes consist of two or more metal layers that carry V_{CC} and ground to the devices. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains V_{CC}, distributes it equally to all devices, and provides very high current-sink capability, noise protection, and shielding for the logic signals on the PCB. Sharing the same plane between analog and digital power supplies may be risky due to unwanted interaction of these two circuit types.

For fully digital systems without separate analog power and ground planes on the board, adding two new planes to the board may be prohibitively expensive. Instead, the board designer can create partitioned power islands (split plane). Figure 2 shows an example board layout with phase-locked loop (PLL) power islands.

Figure 2. Board Layout for General-Purpose PLL Power Islands



To reduce system noise from power distribution:

- For equal power distribution use separate power planes for the analog power supply.
- Avoid trace and multiple signal layers when routing the PLL power supply.
- Place a ground plane next to the PLL power supply plane.

- Place analog and digital components only over their respective ground plane.
- Use ferrite beads to isolate the PLL power supply from digital power supply.

Transmission Line & Signal Routing

After establishing the PCB power network, Altera recommends considering the layout of the devices and traces. Fast edge rates contribute to noise, cross-talk, and ground bounce in varying degrees, depending on the PCB construction material.

Each PCB substrate has a different relative dielectric constant (E_r) that compares the effect of an insulator on the capacitance of a conductor pair to the capacitance of the conductor pair in a vacuum. The substrate determines the length at which the signal traces must be handled as transmission lines.

Table 1 lists E_r values for various dielectric materials.

Table 1. Relative Dielectric Constants

Material	E_r
Air	1.0
PTFE/glass	2.2
Rogers RO 2800	2.9
CE/goreply	3.0
BT/goreply	3.3
GETEK	3.5
CE/glass	3.7
Silicon dioxide	3.9
BT/glass	4.0
Polymide/glass	4.1
FR-4/glass	4.1
Glass cloth	6.0
Alumina	9.0

The following equation shows how each material's E_r value determines the velocity (V_P) at which signals may flow. The constant (C) equals 3×10^8 m/s or 30 cm/ns:

$$V_P = \frac{C}{\sqrt{E_r}}$$

Calculate the propagation delay (t_{PD}) for a given length (l) with the following expression:

$$t_{PD} = \frac{l}{V_P}$$

When driving a line, view the circuit as either a lumped or distributed circuit depending on whether or not the signal edge rate (t_R) is greater than four times the t_{PD}:

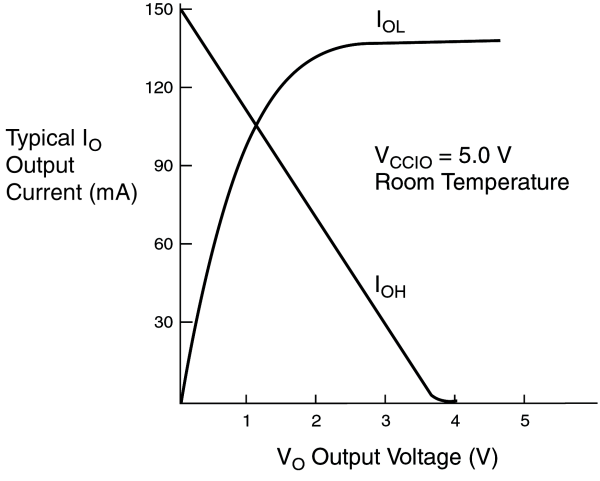
Lumped: $t_R > 4 \times t_{PD}$

Distributed: $t_R < 4 \times t_{PD}$

Model distributed circuits as transmission lines that exhibit ringing, overshoot, and undershoot. In contrast, model lumped circuits as having the same voltage across the line. Some lumped systems exhibit ringing, especially those with large inductance, such as point-to-point wired systems.

An Altera® device's signal edge rate at the rising edge is a function of device capacitance. Estimate this signal edge rate using the device's capacitive load. Altera device family data sheets include output drive characteristics graphs that show the voltage/current relationship of the output drives. Use these graphs to derive an equation for signal edge rate at the rising edge as a function of capacitance. Figure 3 shows the output drive characteristics for the MAX® 7000 device family that is also used to determine the signal edge rate.

Figure 3. Output Drive Characteristics of MAX 7000 Devices



The falling edge, represented by the I_{OL} curve, has a sharper edge rate and is more susceptible to transmission line effects. The curve is roughly linear when it goes from 10% to 90% of the maximum I_{OL}. The following equation approximates the value of I_{OL}:

$$I_{OL} = 0.06\ V_O$$

Solving the charging capacitor equation for time (t) yields the following equations:

$$\frac{\partial V}{\partial t} = \frac{I_O}{C}$$

$$\partial t = \frac{C}{I_O}(\partial V)$$

Substituting the equation above for I_{OL} yields the following equation:

$$\partial t = \frac{C}{(0.06\ V)}(\partial V)$$

Integrating and solving the integral from 10% to 90% yields the following signal edge rate (t_F) equation for the falling edge:

$$t_F = C\frac{1}{0.06} \times \ln(V)\Big|_{0.2}^{2.1} = 39.19 \times C$$

To calculate the output delay time, first determine the fall time of the specified load. To drive a 35-pF load, the fall time is:

$$t_F = 39.19 \times (35 \times 10^{-12})\ \text{seconds} = 1.37\ \text{ns}$$

Again, t_{PD} is the length (l) of the line divided by the velocity (V_P):

$$t_{PD} = \frac{l}{V_P}$$

By solving for l using the equation below, calculate the length at which the line must be treated as a transmission line:

$$l > \frac{t_R \times C_O}{4\sqrt{E_R}} = \frac{(1.37 \times 10^{-9})(3 \times 10^{8})}{4\sqrt{4.1}} = 5.07\ \text{cm}$$

For example, when using a MAX 7000 device to drive a 35-pF load through a glass cloth substrate line that is greater than 5.07 cm, treat the line as a transmission line. Estimation from the curves in Figures 3 shows I_{OL} to have a faster edge rate and, hence, to be prone to transmission line effects. However, if I_{OH} has the faster edge rate, it would be more susceptible, and its linear approximation would be used to calculate l.

In the example above, the MAX 7000 device has a normal slew rate and a V_{CCIO} of 5.0 V. If the slow slew rate logic option is turned on or I/O pins are connected to 3.3 V, the edge rate of the MAX 7000 device is slower. When V_{CCIO} is connected to 3.3 V, use the diagram of its output drive characteristics to calculate $\mathbf{t_F}$.

If the slow slew rate option is turned on, the new $\mathbf{t_F}$ increases. The new expression for $\mathbf{t_F}$ is:

$\mathbf{t_F} = (t_{OD3} - t_{OD2}) + \mathbf{t_F}$ [calculated from the above equation for a normal slew rate]

For example, if a device with a -10 speed grade is used where t_{OD3} = 5.5 ns and t_{OD2} = 1.5 ns, $(t_{OD3} - t_{OD2})$ = (5.5 – 1.5) ns = 4 ns, and the new $\mathbf{t_F}$ for a slow slew rate can be calculated as shown below:

4 ns + 1.37 ns = 5.37 ns

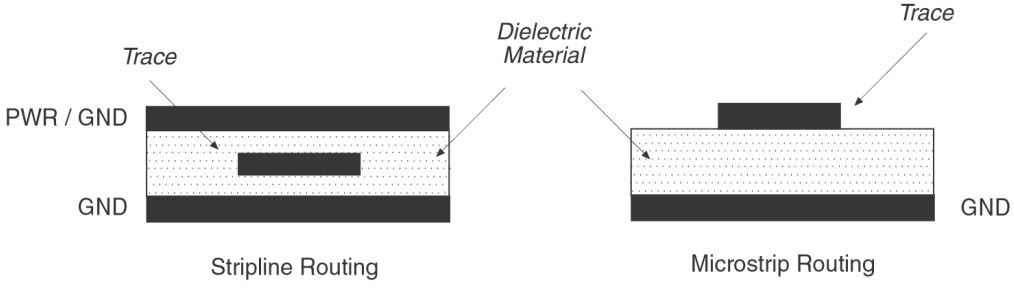
With the slow slew rate option turned on, the new length (*l*) used to determine a transmission line is 19.89 cm.

Consult the appropriate device data sheet to see if a slow slew rate control affects both the rising and falling edge rates of a device.

Signal Routing

Microstrip or stripline routing are ways to route signals on a PCB. Microstrip routing refers to a trace routed on an outside layer of the PCB separated by a dielectric from the reference plane (GND or V_{CC}). Stripline routing refers to a trace routed on an inside layer with two reference planes. See Figure 4.

Figure 4. Stripline & Microstrip Signal Routing



Clock Signal Routing

Considering routing techniques can help to maximize the quality of clock transmission lines. Use the following routing techniques for clock signals:

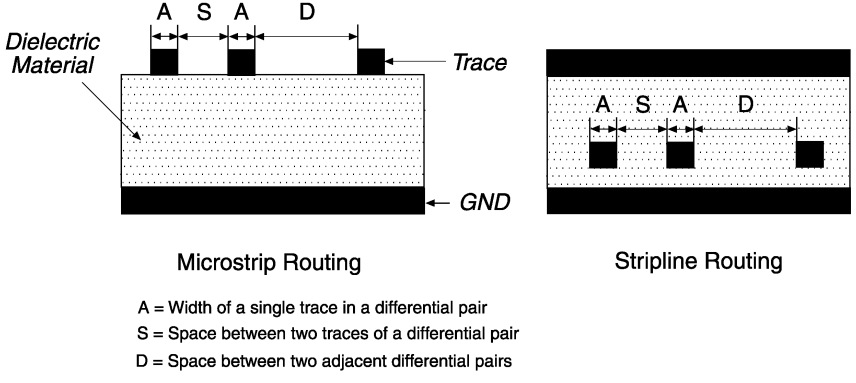
- Avoid using serpentine routing; clock traces should be as straight as possible.
- Avoid using multiple signal layers for clock signals.
- Avoid using vias in the clock transmission line, since vias can contribute impedance change and reflection.
- Route the clock trace on the microstrip (preferably top layer) to minimize the use of vias and delays, since air is the dielectric material. Air has the lowest dielectric constant ($E_r = 1$).
- Place a ground plane next to the outer layer to minimize noise. If using the inner layer for routing the clock trace, sandwich the layer by ground planes to reduce delay.
- Terminate clock signals properly.

Differential Signal Routing

For quality signal transmission, consider routing techniques of differential signals in PCB designs. Use the following techniques for differential signal routing:

- Make D > 2S to minimize crosstalk. See Figure 5.
- Route the two traces of a differential pair as close to each other as possible after they leave the device to ensure minimal reflection.
- Maintain a constant distance between the two traces of a differential pair over their entire length.
- Keep the electrical length between the two traces of a differential pair the same. This minimizes the skew and phase difference.
- To minimize impedance mismatch and inductance, avoid using vias.

Figure 5. Differential Signal Routing



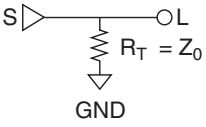
Impedance Matching & Termination Schemes

Mismatched impedance causes signals to reflect up and down the line, which in turn causes ringing at the load. To eliminate reflections, the impedance of the source (Z_S) must equal the impedance of the trace (Z_0), as well as the load (Z_L).

The load impedance is typically much higher than the line impedance, which is higher than the source impedance. On an unmatched transmission line, a signal reflects 100% at the load and approximately 80% at the source, bouncing back and forth until it dies out. To reduce signal reflection, match the impedance either at the load (Z_L) or at the source (Z_S) to the trace (Z_0) by adding an impedance in parallel with the load to reduce its input impedance.

The following examples of how parallel termination schemes diminish the first reflection by matching the load impedance to the line impedance. Altera recommends using either Thevenin or series-RC schemes. For the matching to be effective, terminate each load, because any impedance mismatch will result in a signal reflection.

Simple Parallel Termination



In a simple parallel termination scheme, the termination resistor (R_T) is equal to the line impedance. The placement of the termination resistor must be as close to the load as possible to be efficient. The current loading of this termination is highest at a high-output state. Estimate the current load (I_L) with the following equation:

$$I_L = \frac{V_O}{R_T}$$

Calculate the driving voltage (V_O) from the I_{OH} curve (refer to Figure 3). The equation for I_{OH} is:

$$I_{OH} = 0.15 - (0.038) \times V_O$$

$$V_O = \frac{(0.15 - I_{OH})}{0.038}$$

Calculate the current load for a 1.0 kΩ termination:

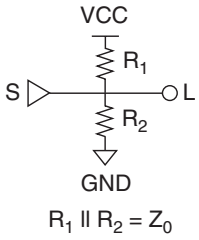
$$I_L = \frac{0.15 - I_{OH}}{0.038 \times 1,000} = \frac{0.15 - I_{OH}}{38}$$

When driving high, $I_L = I_{OH}$, therefore:

$$I_L = \frac{0.15}{39} = 3.85\text{mA}$$

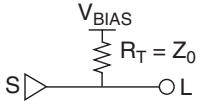
The current load should not exceed the DC operating conditions of a MAX 7000 device, which is 4 mA for I_{OH} and 12 mA for I_{OL}. In this case, the 3.85-mA current load is less than the maximum I_{OH} limit of 4 mA per output pin for MAX 7000 devices.

Thevenin Parallel Termination



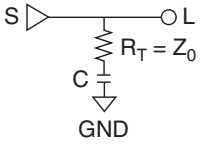
An alternative parallel termination scheme uses a Thevenin voltage divider. The terminating resistor is split between R_1 and R_2, which equals the line impedance when combined. Although this scheme reduces the current draw from the source device, it adds current drawn from the power supply because the resistors are tied between V_{CC} and ground.

Active Parallel Termination



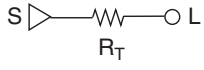
In an active parallel termination scheme, the terminating resistor ($R_T = Z_0$) is tied to a bias voltage (V_{BIAS}). The bias voltage is such that the output drivers are capable of drawing current from the high- and low-level signals. However, this scheme requires a separate voltage source that can sink and source currents to match the output transfer rates.

Series-RC Parallel Termination



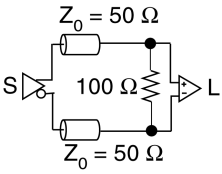
In a series-RC parallel termination scheme, a resistor and capacitor network is the terminating impedance. The terminating resistor (R_T) is equal to Z_0; the capacitor must be greater than 100 pF. The capacitor blocks low-frequency signals while passing high-frequency signals. Therefore, the DC loading effect of R_T does not have an impact on the driver.

Series Termination



A series termination scheme matches the impedance at the signal source instead of matching the impedance at each load. Because the output impedance of Altera devices is low, add a series impedance to match the signal source to the line impedance.

On an unmatched line, the source eventually reduces the reflections. Adding the series termination helps attenuate secondary reflections. The line impedance varies depending on the distribution of the load. Therefore, a single resistor value cannot apply to all conditions. Altera recommends using a 33-Ω series resistor to cover most impedances. This method requires only a single component at the source rather than multiple components at each load, but delays the signal path as it increases the RC time constant.



Differential Pair Termination

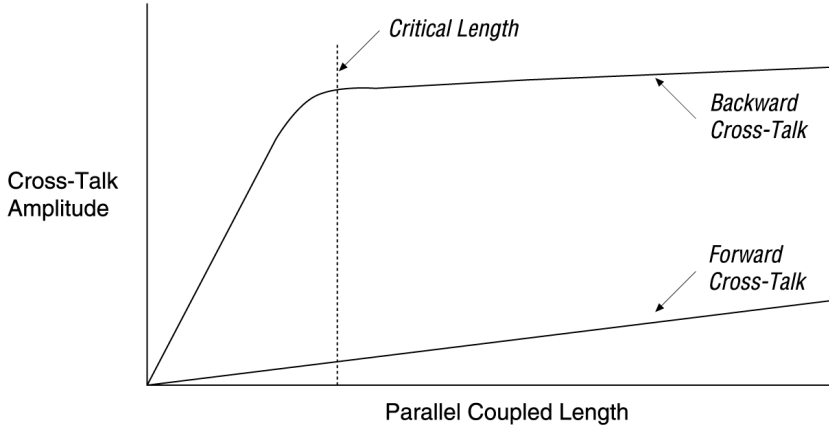
The differential signal I/O standard requires a termination resistor between the signals at the receiving device. The termination resistor should match the differential load impedance of the bus (typically 100 Ω).

See *Application Note 134 (Using Programmable I/O Standards in Mercury™ Devices)* for different types of differential termination schemes, such as LVDS, LVPECL, and PCML.

Cross-Talk

Cross-talk is the unwanted coupling of signals between parallel traces. Two types of cross-talk exist: forward (capacitive) and backward (inductive). Figure 6 illustrates the effect of each type of cross-talk as a function of the parallel length.

Figure 6. Cross-Talk as a Function of Parallel Length



Forward cross-talk has less effect than backward cross-talk. In forward cross-talk, two long running parallel traces have a mutual capacitance between them. A voltage change in one trace produces a capacitive effect on the other trace. This effect appears as a small positive pulse shaped like the derivative of the original voltage change.

Backward cross-talk occurs when the magnetic field from one trace induces a signal in a neighboring trace. In logic systems, the current flow through a trace is significant when the signals are switching or non-static. The magnetic fields created by switching currents induce the coupling transients.

Cross-talk increases when two or more traces run parallel to one another for some distance and also with decreased trace separation. As shown in Figure 7, the center-to-center separation between the two traces should be at least 4 times the trace width. Without disturbing the separation between two traces, lowering the distance between the trace and the ground plane to under 10 mils reduces the cross-talk.

Figure 7. Separation of Traces for Cross-Talk Prevention

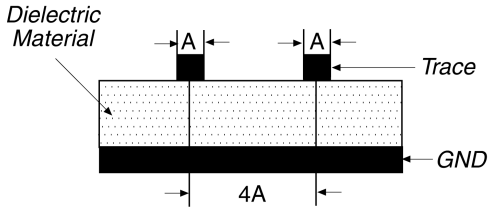
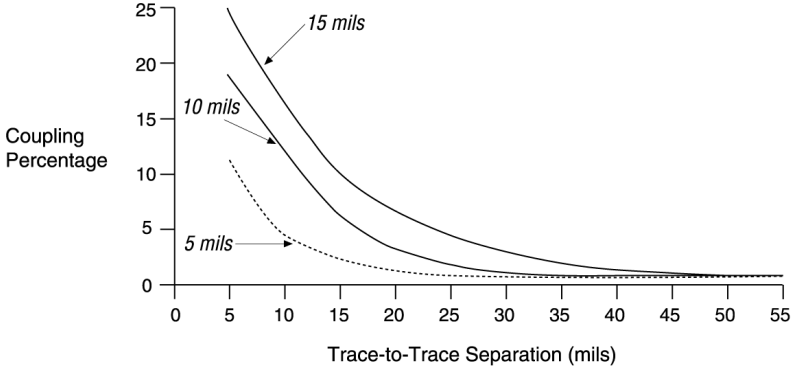


Figure 8 shows the effect of height over GND plane on trace-to-trace coupling. The dielectric material also plays an important role in reducing the cross-talk. Low dielectric material helps to reduce the thickness between the trace and ground plane.

Figure 8. Effect of Height over Ground Plane on Trace-to-Trace Coupling



Ground Bounce

As digital devices become faster, their output switching times decrease. Faster switching times cause higher transient currents in outputs as they discharge load capacitances. These higher currents, which are generated when multiple outputs of a device switch simultaneously from a logic high to a logic low, can cause a board-level phenomenon known as ground bounce.

Many factors contribute to ground bounce. Therefore, no standard test method predicts ground bounce magnitude for all possible PCB environments. Determine each condition's and each device's relative contributions to ground bounce by testing the device under these conditions. Load capacitance, socket inductance, and the number of switching outputs are the predominant conditions that influence the magnitude of ground bounce in programmable logic devices.

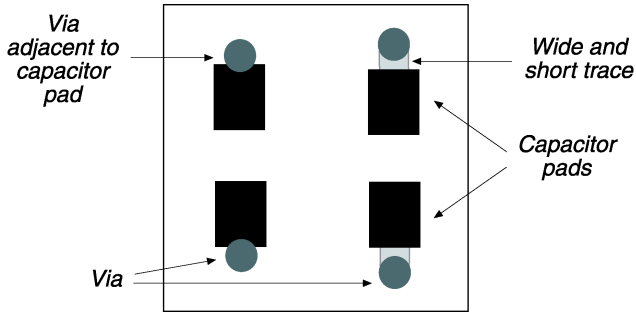
Design Recommendations

Altera recommends the following design methods to reduce ground bounce:

- Add the recommended decoupling capacitors for as many V_{CC}/GND pairs as possible.
- Place the decoupling capacitors as close as possible to the power and ground pins of the device.
- Add external buffers at the output of a counter to minimize the loading on Altera device pins.
- Configure the unused I/O pin as an output pin and then drive the output low. This configuration acts as a virtual ground. Connect this low driving output pin to `GNDINT` and/or the board's ground plane.
- For MAX 7000AE devices, any unused I/O pin may be driven to ground by programming the "programmable ground" bit (one per I/O cell). In doing so, the macrocell will not need to be sacrificed, but can still be used as a buried macrocell.
- When speed is not critical, turn on the slow slew rate logic option for APEX™ II, APEX™ 20K, Mercury™, Excalibur™, FLEX® 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000A, and MAX 7000 designs.
- Limit load capacitance by buffering loads with an external device, such as the 74244 IC bus driver, or by reducing the number of devices that drive the bus.
- Eliminate sockets whenever possible.
- Reduce the number of outputs that can switch simultaneously and/or distribute them evenly throughout the device.
- Move switching outputs close to a package ground pin.
- Create a programmable ground next to switching pins.
- Eliminate pull-up resistors or use pull-down resistors.
- Use multi-layer PCBs that provide separate V_{CC} and ground planes.
- Add 10- to 30-Ω resistors in series to each of the switching outputs to limit the current flow into each of the outputs.
- Create synchronous designs that will not be affected by momentarily switching pins.
- Assign I/O pins to minimize local bunching of output pins.

- Place the power and ground pins next to each other. The total inductance will be reduced by mutual inductance, since current flows in opposite directions in power and ground pins.
- Use a bigger via size to connect the capacitor pad to the power and ground plane to minimize the inductance in decoupling capacitors.
- Use the wide and short trace between the via and the capacitor pad or place the via adjacent to the capacitor pad. See Figure 9.

Figure 9. Suggested Via Location That Connects to Capacitor Pad



- Use surface mount capacitors to minimize the lead inductance.
- Use low effective series resistance (ESR) capacitors. The ESR should be < 400 mΩ.
- Each GND pin/via should be connected to the ground plane individually.
- To add extra capacitance on the board, Altera recommends placing a ground plane next to each power (V_{CC}) plane. This placement gives zero lead inductance and no ESR. The dielectric thickness between the two planes should be ~5 mils.

Search for "Slow Slew Rate" in the Quartus® II Software Help for more information about this logic option.

These design recommendations, many of which are described in detail on pages 17 and 18. in this application note, should help high-speed logic design for operating over a range of PCB conditions.

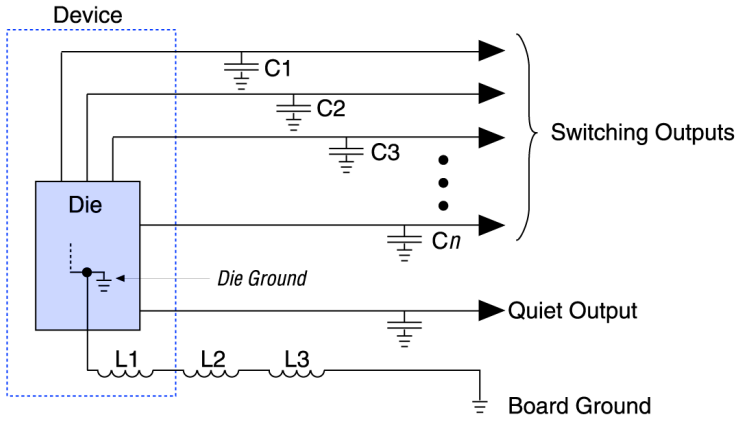
Analyzing Ground Bounce

Figure 10 shows a simple model for analyzing ground bounce. The external components driven by the device appear as capacitance loads to that device (C1 to C*n*). These capacitive loads store a charge determined by the following equation:

Charge (Q) = [voltage (V) × capacitance (C)]

Thus, the charge increases as the voltage and/or load capacitance increases.

Figure 10. Ground Bounce Model



A device's environment and ground path have intrinsic inductances (shown in Figure 10 as L1, L2, and L3). L1 is the inductance of the bond wire from the device's die to its package pin, and of the pin itself. L2 is the inductance of the connection mechanism between the device's ground pin and the PCB. This inductance is greatest when the device is connected to the PCB through a socket. L3 is the inductance of the PCB trace between the device and the PCB location where the power supply's reference ground is connected.

Ground bounce occurs when multiple outputs switch from high to low. The transition causes the charge stored in the load capacitances to flow into the device. The sudden rush of current (di/dt) exits the device through the inductances (L) to board ground, generating a voltage (V) determined by the equation $V = L \times (di/dt)$. This voltage difference between board ground and device ground causes the relative ground level for low or quiet outputs to temporarily rise or bounce. Although the rush of current is brief, the magnitude of the bounce can be large enough to trigger other devices on the PCB.

In synchronous designs, ground bounce is less often a problem because synchronous outputs have enough time to settle before the next clock edge. Also, synchronous circuits are not as likely to be falsely triggered by a voltage spike on a quiet output.

Capacitive loading on the switching outputs and quiet outputs affect ground bounce differently.

Switching Outputs

When the capacitive loading on the switching outputs increases, the amount of charge available for instantaneous switching increases, which in turn increases the magnitude of ground bounce. Depending on the device, ground bounce increases with capacitive loading until the loading is approximately 100 pF per device output. At this point, the device output buffers reach their maximum current-carrying capacity and inductive factors become dominant.

One method of reducing the capacitive load and, consequently, ground bounce is to connect the device's switching outputs to a bus driver integrated circuit (IC). The outputs of this IC drive the heavy capacitive loads, reducing the loading on the device and minimizing ground bounce for the device's quiet outputs.

Some bus applications use pull-up resistors to create a default high value for the bus. These resistors cause the load capacitances to charge up to the maximum voltage. Consequently, the driving device produces a higher level of ground bounce. Eliminate pull-up resistors in applications in which ground bounce is a concern, or design bus logic that uses pull-down resistors instead.

The number of switching outputs also affects ground bounce. As the number of switching outputs increases, the total charge stored also increases. The total charge is equal to the sum of the stored charges for each switching output. Therefore, the amount of current that must sink to ground increases as the number of switching outputs increases. Ground bounce can increase by as much as 40 to 50 mV for each additional output that is switching.

To counteract these effects, Altera devices provide multiple V_{CC} and GND pin pairs. Reduce ground bounce by moving switching outputs close to a ground pin and distributing simultaneously switching outputs throughout the device.

Besides placing switching pins next to a ground pin, create a programmable ground pin by creating an output pin in the design that drives only ground. By connecting this output pin to ground on the board, the device ground has another connection to the board ground, which helps reduce ground bounce.

Many Altera devices have slew rate options for the output drivers. Turning on the slow slew rate option for all or most of the drivers slows down the drivers, decreasing di/dt and reducing ground bounce.

To further reduce ground bounce, limit the number of outputs that can switch simultaneously in the design. For functions such as counters, use Gray coding as an alternative to standard sequential binary coding, because only one bit switches at a time.

In extreme cases, adding resistors (10 Ω to 30 Ω is usually adequate) in series to each of the switching outputs in a high-speed logic device can limit the current flow into each of the outputs and, thus, reduce ground bounce to an acceptable level.

Quiet Outputs

An increase in capacitive loading on quiet outputs acts as a low-pass filter and tends to dampen ground bounce. Capacitive loading on a quiet output can reduce ground bounce by as much as 200 to 300 mV. However, an increase in capacitive loading on a quiet output can increase the noise seen on other quiet outputs when the capacitive-loaded pin does switch.

Minimizing Lead Inductance

Socket usage and PCB trace length are two elements of L2, as shown in Figure 10. Sockets can cause ground bounce voltage to increase by as much as 100%. Eliminating sockets can often reduce the ground bounce on the PCB. The length of the PCB trace has a much smaller effect on ground bounce as compared to sockets. For PCBs with a ground plane, the voltage drop across the inductance (L3) of the PCB trace between the device and the PCB location where other devices in the system reference ground is negligible, because L3 is significantly less than L2. The inductance in a 3-inch trace increases ground bounce for a quiet output by approximately 100 mV. Therefore, keep trace length to a minimum. As traces become longer, transmission line effects may cause other noise problems.

Using multi-layer PCBs that provide separate V_{CC} and ground planes can also reduce the ground bounce caused by PCB trace inductance. Wire-wrapping the V_{CC} and ground supplies usually increases the amount of ground bounce. To reduce unwanted inductance, use low-inductance bypass capacitors between the V_{CC} supply pins and the board ground plane, as close to the package supply pins as possible. Altera requires low ESR decoupling surface mount capacitors of 0.01 µF to 0.1 µF to be used in parallel to reduce ground bounce. Adding a 0.001 µF capacitor in parallel to these capacitors filters high frequency noise (>100 MHz).

Refer to the *Minimizing Ground Bounce & V_{CC} Sag* White Paper for more information about ground bounce.

References

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