Introduction

A critical element of system reliability is the capacity of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system’s ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device’s maximum allowed junction temperature. This application note discusses how to evaluate and manage power, and provides sample worksheets for performing a power evaluation.

Power Evaluation

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To evaluate the power usage in your system, use the following steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power for the device and package.
3. Compare the estimated and maximum power values.

Table 1 shows the variables used for estimating power consumption.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CCSTANDBY}$</td>
<td>mA</td>
</tr>
<tr>
<td>$K$</td>
<td>$\mu A/(MHz \times LE)$</td>
</tr>
<tr>
<td>$I_{MAX}$</td>
<td>MHz</td>
</tr>
<tr>
<td>$N$</td>
<td>LE</td>
</tr>
<tr>
<td>$I_{CCINT}$</td>
<td>mA</td>
</tr>
<tr>
<td>$P_{INT}$</td>
<td>mW</td>
</tr>
<tr>
<td>$MC_{TON}$</td>
<td>LE</td>
</tr>
<tr>
<td>$MC_{DEV}$</td>
<td>LE</td>
</tr>
<tr>
<td>$MC_{USED}$</td>
<td>LE</td>
</tr>
<tr>
<td>$P_{DCOUT}$</td>
<td>mW</td>
</tr>
</tbody>
</table>
Estimating Power Consumption

Use the following formula to compute the estimated power consumption ($P_{EST}$) of the application:

$$P_{EST} = P_{INT} + P_{IO}$$

Where:

- $P_{INT} = I_{CCINT} \times V_{CCINT}$
- $P_{IO} = P_{ACOUT} + P_{DCOUT}$

Therefore:

$$P_{EST} = (I_{CCINT} \times V_{CCINT}) + (P_{ACOUT} + P_{DCOUT})$$

The no-load power ($P_{INT}$) value can be obtained from the “Power Consumption” section in each device family data sheet. Because this value is “unloaded,” it is necessary to add the power dissipated by the I/O buffers—$P_{DCOUT}$ from steady-state outputs and the $P_{ACOUT}$ current from frequently switching outputs. $P_{DCOUT}$ depends on the number of steady-state outputs, the logic levels they drive, and the resistive load on each output, as shown in the following formula:

$$P_{DCOUT} = \sum_{n=1}^{d} P_{DCn}$$

Where:

- $d$ = Number of DC outputs
- $P_{DCn}$ = DC output power of output $n$
- $V_{n}$ = Voltage swing of output $n$
- $f_{n}$ = Switching frequency of output $n$
Table 2 shows the DC power dissipated by the output drivers of a device with $V_{CCIO}$ set at 5 V under typical types of loads. The DC power dissipated by the output driver does not equal the $V_{CC} \times I_{CCIO}$ value because most of the DC power is consumed by the load. If you are using a 2.5-V or 3.3-V device or a non-5.0-V $V_{CCIO}$, you can compute the power based on the device’s $I_{OH}$ and $I_{OL}$ figures shown in the device family data sheet.

<table>
<thead>
<tr>
<th>Load Driven</th>
<th>$P_{DCO}(\text{mW})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-K pull-up resistor for low outputs</td>
<td>0.49</td>
</tr>
<tr>
<td>1-K pull-down resistor for high outputs</td>
<td>5.04</td>
</tr>
<tr>
<td>Bipolar for low outputs</td>
<td>0.16</td>
</tr>
<tr>
<td>Bipolar for high outputs</td>
<td>0.0576</td>
</tr>
<tr>
<td>CMOS inputs</td>
<td>Negligible</td>
</tr>
</tbody>
</table>

$P_{ACOUT}$ depends on the capacitive load on each output and the frequency at which each output switches, as shown in the following formula:

$$P_{ACOUT} = \sum_{n=1}^{a} C_n V_n f_n \times V_{CCIO}$$

Where:
- $a$ = Number of AC outputs
- $C_n$ = Capacitive load on output $n$
- $V_n$ = Voltage swing of output $n$
- $f_n$ = Switching frequency of output $n$

The following equation shows the frequency of each output ($f_n$), in terms of the maximum clock frequency ($f_{MAX}$) of the design and the average ratio of I/O pins toggling at each clock ($\text{tog}_{IO}$):

$$f_n = (0.5) \times f_{MAX} \times \text{tog}_{IO}$$

Inserting the equation for $f_n$ into the $P_{ACOUT}$ equation and resolving the summation for an average capacitive load yields the following formula:

$$P_{ACOUT} = (0.5) \times \text{OUT} \times C_{AVE} \times V_{O} \times f_{MAX} \times \text{tog}_{IO} \times V_{CCIO}$$

Where: $\text{OUT}$ = Total number of output and bidirectional pins
Table 3 shows the \( V_{CCIO} \) and \( V_O \) values for Altera® devices.

<table>
<thead>
<tr>
<th>( V_{CCIO} ) (V)</th>
<th>( V_O ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0</td>
<td>3.8</td>
</tr>
<tr>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>2.5</td>
<td>2.5</td>
</tr>
</tbody>
</table>

For example, the following equation provides the power consumed by driving a capacitive load for applications with \( V_{CCIO} = 5 \) V:

\[
P_{ACOUT} = \left(0.5\right) \times OUT \times C_{AVE} \times 3.8 \, \text{V} \times f_{MAX} \times I_{OIO} \times 5.0 \, \text{V}
\]

**Calculating Maximum Power for the Device & Package**

The following formulas are used to calculate the maximum allowed power (\( P_{MAX} \)) for a device:

\[
P_{MAX} = \frac{T_J - T_A}{\theta_{JA}} \quad \text{or} \quad P_{MAX} = \frac{T_J - T_C}{\theta_{JC}}
\]

The maximum allowed power is dependent on the maximum allowed junction temperature (\( T_J \)) of the silicon, the ambient temperature of operation (\( T_A \)), and the package’s thermal resistance (\( \theta_{JA} \)) when configured in the system. The maximum junction temperature is specified in the Altera device family data sheets. The ambient temperature depends on the application. The worst-case \( P_{MAX} \) value is estimated using the formula with \( \theta_{JA} \), the junction-to-ambient thermal resistance. The \( \theta_{JA} \) value for Altera devices is provided for still air (with convection cooling only), and for a forced-air flow of 100 feet/second, 200 feet/second, and 400 feet/second. If heat-sinking is used to dissipate heat and \( \theta_{JA} \) for a heat sink is given, you should use the case temperature (\( T_C \)) and the junction-to-case thermal resistance (\( \theta_{JC} \)) to calculate \( P_{MAX} \) for a device. \( \theta_{JC} \) is a measure of the lowest possible thermal resistance.

For thermal resistance values (\( \theta_{JC} \) and \( \theta_{JA} \)) of Altera devices, refer to the *Altera Device Packaging Information Data Sheet*.
Comparing Maximum Allowed Power & Estimated Power

To avoid reliability problems, you should compare the values calculated for the maximum allowed power and estimated power. The estimated power should be the smaller of the two values. If the estimated power exceeds the maximum allowed power, refer to “Thermal Management” on page 10 for suggestions on how to reduce power requirements for a design. Figure 1 shows a sample worksheet for evaluating power.

Figure 1. Power Evaluation Worksheet (Part 1 of 2)

Design___________________________             Device_________________________

Estimating the Power Consumption of the Application

Internal Power Calculation for All Altera Devices

FLEX 10K, FLEX 8000 & FLEX 6000 Devices

Standby current (ICCSTANDBY)

ICCSTANDBY = mA

Coefficient for ICC calculation. See the appropriate device family data sheet for this value.

K = µA/(MHz × LE)

Maximum clock frequency (fMAX)

fMAX = MHz

Total number of logic elements (LEs) used in the device (N)

N = LE

Average ratio of logic cells toggling (toGLC) at each clock (typically 0.125)

toGLC =

Total internal current (ICCINT)

ICCINT = mA

ICCINT = ICC0 + K × fMAX × N × toGLC

Total internal power (PINT)

PINT = mW

PINT = VCC × ICCINT

MAX 9000, MAX 7000 & MAX 3000A Devices

Coefficients for ICC calculation. See the appropriate device family data sheet for these values.

Number of macrocells with the Turbo Bit™ on (MCTON)

MCTON = LE

Number of macrocells in the device (MCDEV)

MCDEV = LE

Number of macrocells in the design (MCUSED)

MCUSED = LE

Average ratio of logic cells toggling (toGLC) at each clock (typically 0.125)

toGLC =

Total internal current (ICCINT)

ICCINT = mA

ICCINT = (A × MCTON) + [B × (MCDEV − MCTON)] + (C × MCUSED × fMAX × toGLC)

Total internal power (PINT)

PINT = mW

PINT = VCC × ICCINT
External Power Calculation for All Altera Devices

Power consumed by the DC output load ($P_{DCOUT}$)

$$P_{DCOUT} = mW$$

Average capacitive load ($C_{AVE}$) at output pins

$$C_{AVE} = pF$$

Number of output/bidirectional pins in the design ($OUT$)

$$OUT =$$

Average ratio of I/O pins toggling ($to\!g_{IO}$) at each clock (typically 0.125)

$$to\!g_{IO} =$$

Power consumed by AC output load ($P_{ACOUT}$)

$$P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times V_{IO} \times f_{MAX} \times to\!g_{IO} \times V_{CCIO} \times 0.001$$

Total external power ($P_{IO}$)

$$P_{IO} = P_{DCOUT} + P_{ACOUT}$$

Total Power Calculation for All Altera Devices

Estimated total power ($P_{EST}$)

$$P_{EST} = mW$$

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device

$$\theta_{JA} = ^\circ C/W$$

Maximum junction temperature ($T_J$) as specified in the appropriate device family data sheet.

$$T_J = ^\circ C$$

Ambient temperature ($T_A$) of the design

$$T_A = ^\circ C$$

Maximum power ($P_{MAX}$) allowed for the device

$$P_{MAX} = \frac{(T_J - T_A)}{\theta_{JA}} W$$

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? Yes or No
Tables 4 and 5 show design parameters for the sample power evaluations shown in Figures 2 and 3. The design parameters are unique to the sample designs and are not found in device family data sheets.

**Table 4. Parameters for the Sample FLEX 10K Design**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>Number of outputs</td>
<td>150</td>
</tr>
<tr>
<td>Number of 1-KΩ pull-up resistors</td>
<td>Type of load</td>
<td>50</td>
</tr>
<tr>
<td>CMOS inputs</td>
<td>Type of load</td>
<td>100</td>
</tr>
<tr>
<td>(C_{AVE})</td>
<td>Average capacitance</td>
<td>35 pF</td>
</tr>
<tr>
<td>(N)</td>
<td>Number of logic elements used</td>
<td>2,747 LE</td>
</tr>
<tr>
<td>(f_{MAX})</td>
<td>Maximum operating frequency</td>
<td>20 MHz</td>
</tr>
<tr>
<td>(P_{DCOUT})</td>
<td>Static power consumed by outputs</td>
<td>((0.49 \text{ mW} \times 50) + (0 \text{ mW} \times 231) = 24.5 \text{ mW})</td>
</tr>
</tbody>
</table>

**Table 5. Parameters for the Sample MAX 9000 Design**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_{CTON})</td>
<td>139</td>
</tr>
<tr>
<td>(M_{CDEV})</td>
<td>560</td>
</tr>
<tr>
<td>(M_{USED})</td>
<td>500</td>
</tr>
<tr>
<td>(M_{CTOFF})</td>
<td>421</td>
</tr>
<tr>
<td>(f_{MAX})</td>
<td>40 MHz</td>
</tr>
<tr>
<td>OUT</td>
<td>211</td>
</tr>
<tr>
<td>Number of 1-KΩ pull-down resistors</td>
<td>10</td>
</tr>
<tr>
<td>CMOS inputs</td>
<td>201</td>
</tr>
<tr>
<td>(C_{AVE})</td>
<td>35 pF</td>
</tr>
<tr>
<td>(P_{DCOUT})</td>
<td>((5.04 \text{ mW} \times 10) + (0 \text{ mW} \times 201) = 50 \text{ mW})</td>
</tr>
</tbody>
</table>

Figures 2 and 3 provide power evaluations for sample designs implemented in FLEX® 10K and MAX® 9000 devices, respectively.
AN 74: Evaluating Power for Altera Devices

Figure 2. Sample Power Evaluation for a FLEX 10K Device (Part 1 of 2)


Estimating the Power Consumption of the Application

Internal Power Calculation
FLEX 10K, FLEX 8000 & FLEX 6000 Devices

- Standby current ($I_{CCSTANDBY}$)
  $I_{CCSTANDBY} = 0.500$ mA

- Coefficient for $I_{CC}$ calculation. See the appropriate device family data sheet for this value.
  $K = 45 \, \mu A/(MHz \times LE)$

- Maximum clock frequency ($f_{MAX}$)
  $f_{MAX} = 50$ MHz

- Total number of logic elements used in the device (N)
  $N = 2,747$ LE

- Average ratio of logic cells toggling ($t_{ogLC}$) at each clock (typically 0.125)
  $t_{ogLC} = 0.125$

- Total internal current ($I_{CCINT}$)
  $I_{CCINT} = I_{CCSTANDBY} + K \times f_{MAX} \times N \times t_{ogLC}$

- Total internal power ($P_{INT}$)
  $P_{INT} = V_{CC} \times I_{CCINT}$

External Power Calculation for All Altera Devices

- Power consumed by the DC output load ($P_{DCOUT}$)
  $P_{DCOUT} = P_{DCn}$

- Average capacitive load ($C_{AVE}$) at output pins
  $C_{AVE} = 35 \, pF$

- Number of output/bidirectional pins in the design (OUT)
  $OUT = 150$

- Average ratio of I/O pins toggling ($t_{ogIO}$) at each clock (typically 0.125)
  $t_{ogIO} = 0.125$

- Power consumed by AC output load ($P_{ACOUT}$)
  $P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times 3.3 \, V \times f_{MAX} \times t_{ogIO} \times 3.3 \, V \times 0.001$

- Total external power ($P_{IO}$)
  $P_{IO} = P_{DCOUT} + P_{ACOUT}$

Total Power Calculation for All Altera Devices

- Estimated total power ($P_{EST}$)
  $P_{EST} = P_{INT} + P_{IO}$

$P_{EST} = 2,764.9$ mW
AN 74: Evaluating Power for Altera Devices

Figure 2. Sample Power Evaluation for a FLEX 10K Device (Part 2 of 2)

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device
\[ \theta_{JA} = 8 \degree C/W \]

Maximum junction temperature (T\text{J}) as specified in the appropriate device family data sheet.
\[ T\text{J} = 85 \degree C \]

Ambient temperature (T\text{A}) of the design
\[ T\text{A} = 40 \degree C \]

Maximum power (P\text{MAX}) allowed for the device
\[ P\text{MAX} = \frac{(T\text{J} - T\text{A})}{\theta_{JA}} \]

P\text{MAX} = 5.625 W

Comparing Maximum Power Allowed & Estimated Power

Is P\text{EST} < P\text{MAX}? Yes or No

Figure 3. Sample Power Evaluation for a MAX 9000 Device (Part 1 of 2)

Calculating Maximum Allowed Power for the Device & Package

Design atm_pkt.tdf Device EPM9560ARC304-10

Estimating the Power Consumption of the Application

Internal Power Calculation

MAX 9000, MAX 7000 & MAX 3000A Devices

Coefficients for I\text{CC} calculation. See the appropriate device family data sheet for these values.

- A = 0.68 mA/LE
- B = 0.26 mA/LE
- C = 0.052 mA/(MHz \times LE)

Number of macrocells with the Turbo Bit on (MC\text{T\text{ON}})

Number of macrocells in the device (MC\text{DEV})

Number of macrocells in the design (MC\text{USED})

Maximum clock frequency (f\text{MAX})

Average ratio of logic cells toggling (tog\text{LC}) at each clock (typically 0.125)

Total internal current (I\text{CC\text{INT}})

\[ I\text{CC\text{INT}} = (A \times MC\text{T\text{ON}}) + [B \times (MC\text{DEV} - MC\text{T\text{ON}})] + (C \times MC\text{USED} \times f\text{MAX} \times tog\text{LC}) \]

Total internal power (P\text{INT})

\[ P\text{INT} = V\text{CC} \times I\text{CC\text{INT}} \]

P\text{INT} = 1,669.9 mW

External Power Calculation for All Altera Devices

Power consumed by the DC output load (P\text{DC\text{OUT}})

\[ P\text{DC\text{OUT}} = P\text{DCn} \]

Average capacitive load (C\text{AVE}) at output pins

Number of output/bidirectional pins in the design (OUT)

Average ratio of I/O pins toggling (tog\text{IO}) at each clock (typically 0.125)

Power consumed by AC output load (P\text{AC\text{OUT}})

C\text{AVE} = 35 pF

OUT = 211

tog\text{IO} = 0.125

P\text{AC\text{OUT}} = 350.79 mW
Use available low-power features of the device. By turning the Turbo Bit™ off, Classic™ devices and individual macrocells in MAX 9000, MAX 7000, and MAX 3000A devices can be configured for low-power operation, with only a nominal increase in propagation delays. Macrocells in MAX 9000, MAX 7000, or MAX 3000A devices that do not need to run in high-performance mode should be set to low-power mode.

Choose a different device package. A ceramic or higher-pin-count package can be used. Ceramic packages dissipate more heat than plastic packages. Also, packages with higher pin counts can dissipate more heat through the connections to the printed circuit board (PCB).

Use forced-air cooling and/or heat-sinking. Forced-air cooling improves the efficiency of convection cooling, which reduces the surface temperature of the device. A heat sink connected to a device significantly increases heat dissipation by radiating heat via the metal mass.
Slow the operation in portions of the circuit. I_{CC} is proportional to the frequency of operation. Slowing parts of a circuit lowers the I_{CC} and hence reduces the power. Altera devices provide global or array clock sources for all registers. Signals that do not require high-speed operation can use a slower array clock that significantly reduces the system power consumption.

Reduce the number of outputs. DC and AC current is required to support all I/O pins on the device. Reducing the number of I/O pins may reduce the current necessary for the device, and thereby reduce the power.

Reduce the amount of circuitry in the device. Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device. The same effect may be achieved by using a larger device, which also provides increased heat dissipation and maintains a single-device solution.

Choose a different device family. Some device families consume less power than others. For example, the MAX 7000 family provides more power-saving features than the MAX 5000 family. The Classic family provides power-saving features for low-density designs, and low-speed designs consume less power when implemented in FLEX devices.

Modify the design to reduce power. Identify areas in the design that can be revised to reduce the power requirements. Common solutions include reducing the number of switching nodes and/or required logic, and removing redundant or unnecessary signals. For assistance in locating less obvious changes, contact Altera Applications at (800) 800-EPLD.

Revision History

The information contained in Application Note 74 (Evaluating Power for Altera Devices) version 3.1 supersedes information published in previous versions. In version 3.1, the MAX device in Figure 3 was updated.
Operating Requirements for Altera Devices

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